

THCX422R10

USB 3.2 / V-by-One® HS Re-driver with Linear Equalization

General Description

The THCX422R10 is high performance bi-directional active re-driver for serial links with data rates up to 10Gbps.

The THCX422R10 feature a continuous time linear equalizer (CTLE) to provide a boost of up to +15.6dB at 5GHz and open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums.

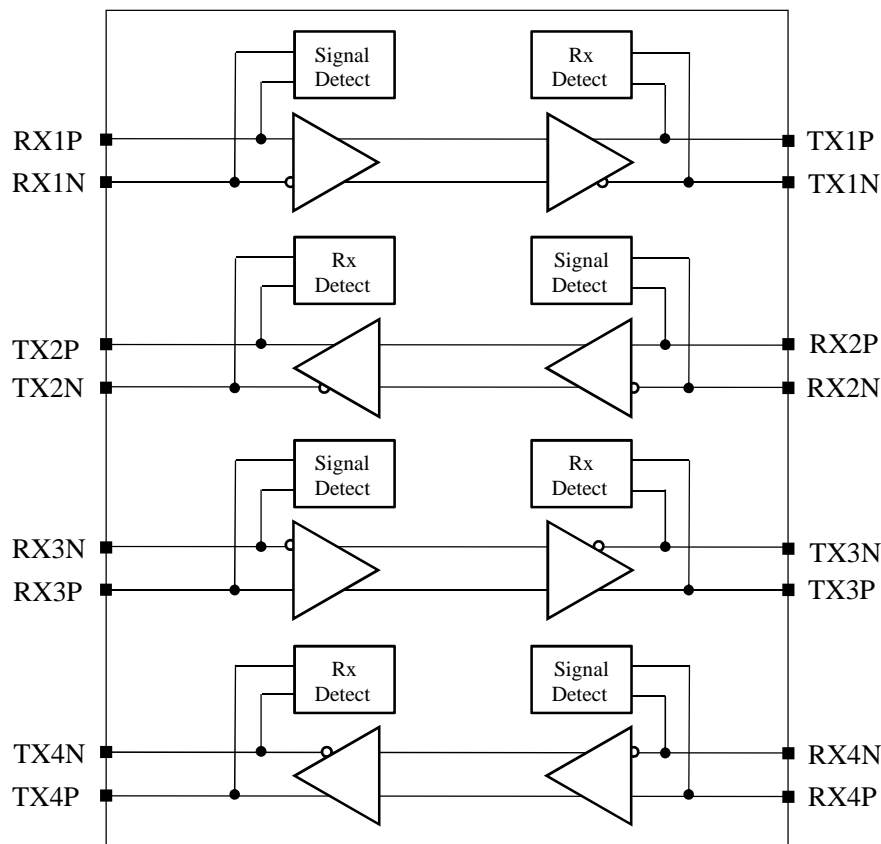
Features

- Signal Conditioning with Linear Equalizer
- Linear Equalization up to +15.6dB@5GHz
- Adjustable Voltage Output Swing Linear Range
- Adjustable Receiver Equalization and DC Gain
- Support USB 3.1 Gen2 and USB 3.2
 - Receiver and LFPS Detect
- Single Supply Voltage (3.3V)
- Package : QFN42 (3.5mm x 9.0mm)

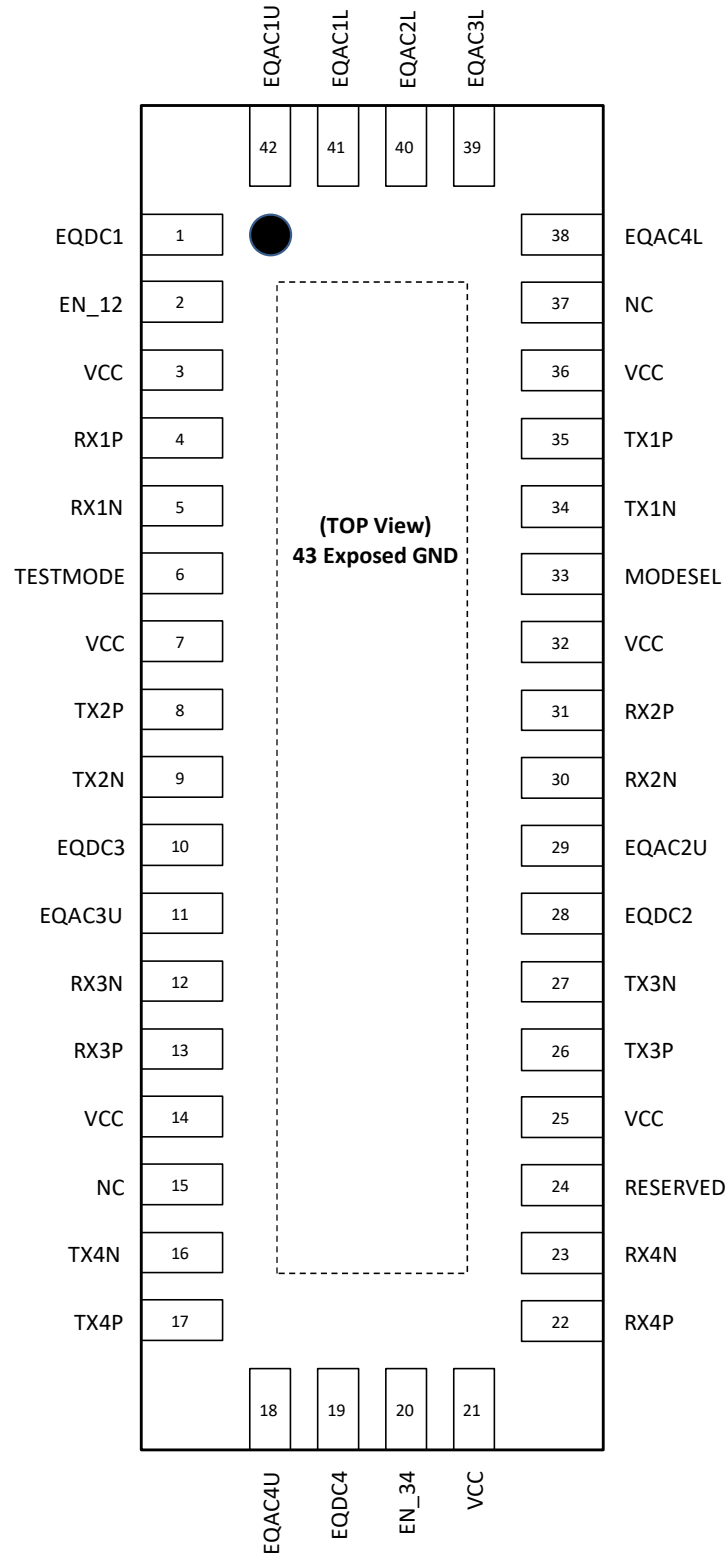
Applications

- USB 3.x
- Tablets, Laptops, Monitors, Phones
- USB Host and Devices
- Docking Stations
- Active Cable
- V-by-One® HS

Block Diagram



Pin Configuration





Pin Description

Pin Name	Pin No	Type	Description
RX1P,RX1N	4, 5	CI	High-Speed CML Signal Input (Channel1(=CH1))
TX1P,TX1N	35, 34	CO	High-Speed CML Signal Output (CH1)
RX2P,RX2N	31, 30	CI	High-Speed CML Signal Input (Channel2(=CH2))
TX2P,TX2N	8, 9	CO	High-Speed CML Signal Output (CH2)
RX3P,RX3N	13, 12	CI	High-Speed CML Signal Input (Channel3(=CH3))
TX3P,TX3N	26, 27	CO	High-Speed CML Signal Output (CH3)
RX4P,RX4N	22, 23	CI	High-Speed CML Signal Input (Channel4(=CH4))
TX4P,TX4N	17, 16	CO	High-Speed CML Signal Output (CH4)
EN_12	2	IPU	Channel Enable(CH1, CH2) With internal 480kΩ pull-up resistor 0 : Power Down 1 : Normal Operation
EN_34	20	IPU	Channel Enable(CH3, CH4) With internal 480kΩ pull-up resistor 0 : Power Down 1 : Normal Operation
EQAC1U	42	4LI	CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1L allows for up to 16 settings
EQAC1L	41	4LI	CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1U allows for up to 16 settings(default 1)
EQAC2U	29	4LI	CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2L allows for up to 16 settings
EQAC2L	40	4LI	CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2U allows for up to 16 settings(default 1)
EQAC3U	11	4LI	CH3 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC3L allows for up to 16 settings
EQAC3L	39	4LI	CH3 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC3U allows for up to 16 settings(default 1)
EQAC4U	18	4LI	CH4 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC4L allows for up to 16 settings
EQAC4L	38	4LI	CH4 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC4U allows for up to 16 settings(default 1)
EQDC1	1	4LI	CH1 Equalizer DC Gain setting
EQDC2	28	4LI	CH2 Equalizer DC Gain setting
EQDC3	10	4LI	CH3 Equalizer DC Gain setting
EQDC4	19	4LI	CH4 Equalizer DC Gain setting
MODESEL	33	4LI	Chip Operation Mode Select 1 : CH1/2, CH3/4 enable, RxDetect/SignalDetect enable F : CH1/2, CH3/4 enable, RxDetect enable, SignalDetect disable R : CH1/2, CH3/4 enable, RxDetect/SignalDetect disable 0 : CH1,3 enable, CH2,4 disable, RxDetect/SignalDetect disable
NC	15, 37	-	Non Connection pin. Must be open
RESERVED	24	I	Must be tied to VCC
TESTMODE	6	I	Test Mode Entry 1 : Normal Operation 0 : Test Mode
VCC	3, 7, 14, 21, 25, 32, 36	PWR	Power supply pin for on-chip regulator.
GND	43	GND	Exposed Pad Ground

CI: CML Input buffer, CO: CML Output buffer, I: LVCMOS Input buffer
 IPU: LVCMOS Input buffer. With internal 480kΩ pull-up resistor.
 4LI: 4-Level LVCMOS Input buffer. With internal 180kΩ pull-up resistor and 300kΩ pull-down resistor.
 0: Tie 0Ω to GND R: Tie 180kΩ to GND F: Leave Open 1: Tie 0Ω to VCC
 PWR: Power supply, GND: Ground



Functional Overview

The function that THCX422R10 has below item.

- 4ch Re-driver
- Signal Detection and Receiver Termination Detection designated for USB3.x
- Signal Conditioning with Linear Equalizer
- Single Supply Voltage (3.3V)

Operation Mode Settings

The operation mode setting is showed below.

Table 1 Operation Mode Setting

Pin Settings			Operation Mode
EN_12	EN_34	MODESEL	
1	1	0(*1)	CH1,3 Enable, CH2,4 Disable, RxDetect Disable, SignalDetect Disable
		R(*2)	CH1,2,3,4 Enable, RxDetect Disable, SignalDetect Disable
		F(*3)	CH1,2,3,4 Enable, RxDetect Enable, SignalDetect Disable
		1(*4)	CH1,2,3,4 Enable, RxDetect Enable, SignalDetect Enable
1	0	-	Forbidden
0	1	-	Forbidden
0	0	Ignore	Chip Power Down.

- *1 Tie 0Ω to GND
- *2 Tie 180kΩ to GND
- *3 Leave Open
- *4 Tie 0Ω to VCC

Detect Function

THCX422R10 has Input Signal Detect (SignalDetect) and Receiver Detect (RxDetect) functionality for USB3.x transmission.

Detect functionality must be disable when it is not USB3.x application.



Liner Equalizer Settings

Table 2 Equalization and -1dB Compression Point Linear Swing Settings

EQACnU*1	EQACnL*1	EQDCn*1	Equalizer Settings (dB) @1.5GHz / 2.5GHz / 5GHz	Output Linear Swing Settings (mVppd)	
				@100MHz	@5GHz
0	0	0	1.2 / 3.0 / 7.6	830	760
0	R		1.8 / 4.1 / 9.0		
R	0		2.0 / 4.4 / 10.2		
R	R		2.6 / 5.4 / 11.3		
F	0		2.7 / 5.8 / 12.3		
F	R		3.4 / 6.7 / 13.3		
1	0		3.6 / 7.1 / 13.9		
1	R		4.2 / 7.9 / 14.5		
0	0	R	1.9 / 3.5 / 7.7	830	760
0	R		2.5 / 4.4 / 9.2		
R	0		2.6 / 4.8 / 10.3		
R	R		3.2 / 5.7 / 11.4		
F	0		3.3 / 6.1 / 12.4		
F	R		3.9 / 7.0 / 13.4		
1	0		4.1 / 7.4 / 14.0		
1	R		4.6 / 8.2 / 14.6		
0	0	F	3.0 / 4.2 / 7.6	830	760
0	R		3.5 / 5.0 / 9.2		
R	0		3.6 / 5.4 / 10.2		
R	R		4.1 / 6.1 / 11.4		
F	0		4.2 / 6.5 / 12.3		
F	R		4.7 / 7.3 / 13.2		
1	0		4.8 / 7.7 / 13.9		
1	R		5.3 / 8.4 / 14.4		
0	0	1	6.4 / 6.8 / 8.6	830	760
0	R		6.6 / 7.3 / 9.8		
R	0		6.7 / 7.6 / 10.8		
R	R		7.0 / 8.1 / 11.8		
F	0		7.1 / 8.4 / 12.7		
F	R		7.4 / 9.0 / 13.5		
1	0		7.5 / 9.3 / 14.1		
1	R		7.8 / 9.8 / 14.7		
0	F	0	2.5 / 4.3 / 8.5	1200	1000
0	1		3.2 / 5.3 / 9.9		
R	F		3.4 / 5.6 / 11.0		
R	1		4.0 / 6.5 / 12.1		
F	F		4.0 / 6.9 / 13.2		
F	1		4.7 / 7.9 / 14.1		
1	F		4.9 / 8.2 / 14.8		
1	1		5.4 / 9.0 / 15.5		
0	F	R	3.2 / 4.8 / 8.6	1200	1000
0	1		3.8 / 5.7 / 10.0		
R	F		4.0 / 6.0 / 11.1		
R	1		4.5 / 6.9 / 12.3		
F	F		4.6 / 7.2 / 13.3		
F	1		5.2 / 8.1 / 14.2		
1	F		5.3 / 8.5 / 14.9		
1	1		5.9 / 9.2 / 15.6		

Average of all channels in typical condition

*1 n=1,2,3,4

EQACnU ^{*1}	EQACnL ^{*1}	EQDCn ^{*1}	Equalizer Settings (dB) @1.5GHz / 2.5GHz / 5GHz	Output Linear Swing Settings (mVppd)	
				@100MHz	@5GHz
0	F	F	4.3 / 5.5 / 8.7	1200	1000
0	1		4.8 / 6.3 / 10.0		
R	F		4.9 / 6.6 / 11.0		
R	1		5.4 / 7.3 / 12.2		
F	F		5.5 / 7.7 / 13.2		
F	1		5.9 / 8.5 / 14.1		
1	F		6.1 / 8.8 / 14.7		
1	1		6.5 / 9.5 / 15.4		
0	F	1	7.7 / 8.1 / 9.5	1200	1000
0	1		8.0 / 8.6 / 10.7		
R	F		8.1 / 8.8 / 11.6		
R	1		8.3 / 9.3 / 12.7		
F	F		8.4 / 9.6 / 13.5		
F	1		8.7 / 10.1 / 14.4		
1	F		8.8 / 10.4 / 15.0		
1	1		9.0 / 10.9 / 15.6		

Average of all channels in typical condition

*1 n=1,2,3,4

Table 3 Flat Gain Settings

EQDCn ^{*1}	Flat Gain Settings (dB) @Up to 300MHz	
	EQACn ^{*1} L=0/R	EQACn ^{*1} L=F/1
0	-2.6	-1.2
R	-1.7	-0.3
F	-0.2	1.3
1	3.8	5.2

Average of all channels in typical condition

*1 n=1,2,3,4

-1dB Compression Point is showed below. It means output voltage range that has linearity.

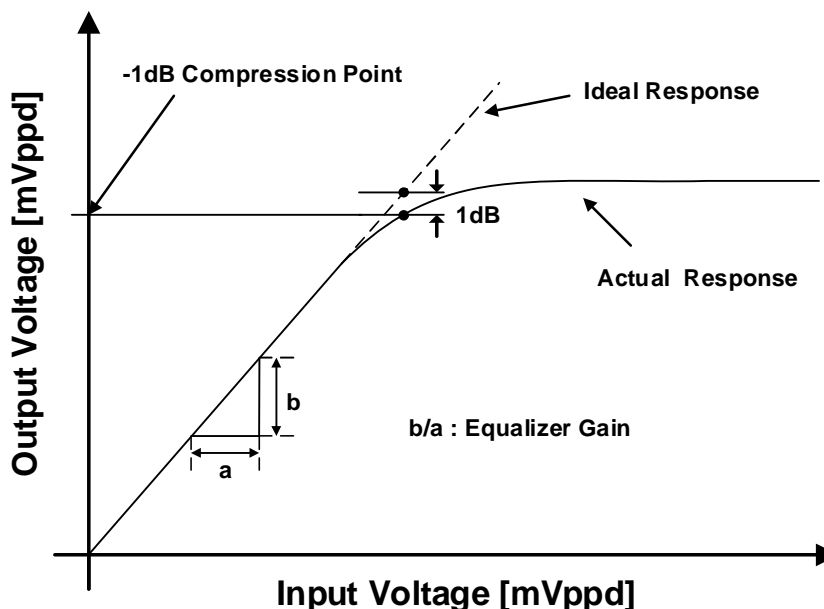


Figure 1. -1dB Compression Point

Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	-0.3	-	4.0	V
LVC MOS Input/Output Voltage	-0.3	-	VCC+0.3	V
4-Level LVC MOS Input Voltage	-0.3	-	VCC+0.3	V
CML Receiver Input Voltage	-0.3	-	VCC+0.3	V
CML Transmitter Output Voltage	-0.3	-	VCC+0.3	V
ESD Rating	HBM	-	±4	kV
	MM	-	±200	V
	CDM	-	±1000	V
Storage Temperature	-55	-	125	°C
Junction Temperature	-	-	125	°C
Reflow Peak Temperature/Time	-	-	260/10	°C/sec

Recommended Operating Conditions

Table 5 Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	3.0	3.3	3.6	V
Supply Ramp Requirement	0.1	-	50	ms
Operating Temperature	-40	-	85	°C

Equivalent CML Input Schematic Diagram

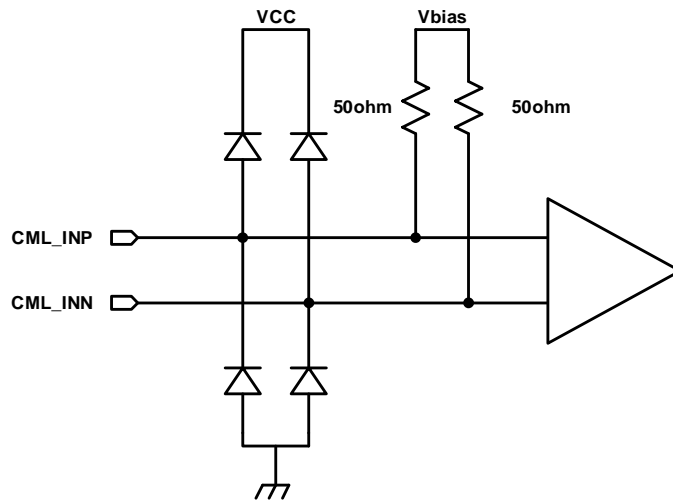


Figure 2. CML Input Schematic Diagram

Equivalent CML Output Schematic Diagram

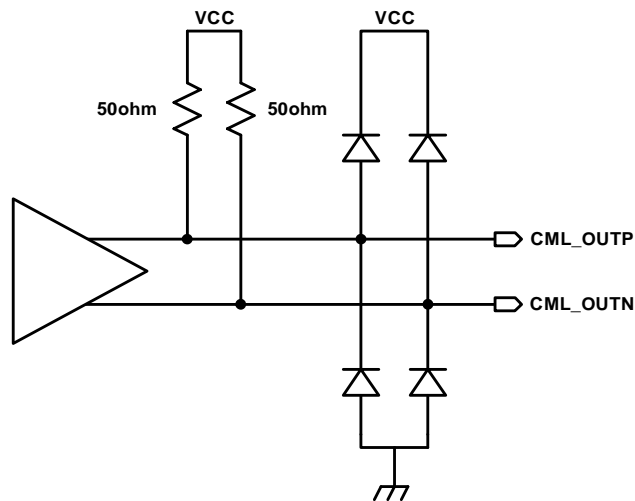


Figure 3. CML Output Schematic Diagram

Equivalent LVC MOS Input Schematic Diagram

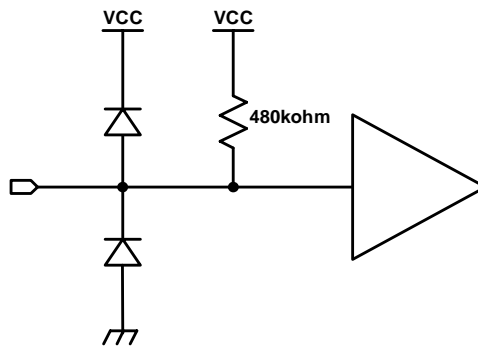


Figure 4. LVC MOS Input Schematics Diagram

Equivalent 4-Level LVC MOS Input Schematic Diagram

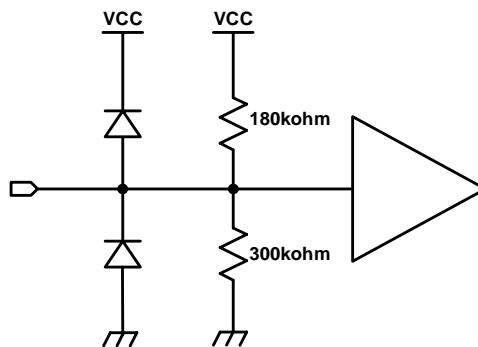


Figure 5. 4-Level Input Schematics Diagram



Electrical Specification

Supply Current

Table 6 Supply Current

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCW	Active Mode Supply Current	EQACn ¹ U=F/1	-	220	280	mA
		EQACn ¹ U=0/R	-	180	240	mA
ICCSL	Slumber Mode Supply Current	No Input signal	-	90	135	mA
ICCI	Unplug Mode Supply Current	No Output load	-	2.0	2.6	mA
ICCS	Power Down Supply Current	EN_12/34=0	-	270	550	uA

*1 n=1,2,3,4

LVC MOS DC Specification

Table 7 LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	-	2.0	-	VCC	V
VIL	Low Level Input Voltage	-	0	-	0.7	V

4-Level LVC MOS DC Specification

Table 8 4-Level LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{THL}	Low Level Input Voltage	0(*1)	0	-	VCC*0.25 - 0.3	V
V _{THR}	R-Level Input Voltage	R(*2)	VCC*0.25 + 0.3	-	VCC*0.5 - 0.3	V
V _{THF}	F-Level Input Voltage	F(*3)	VCC*0.5 + 0.3	-	VCC*0.75 - 0.3	V
V _{THH}	High Level Input Voltage	1(*4)	VCC*0.75 + 0.3	-	VCC	V
I _{IH_4L}	High level Input Leak Current	VIN=VCC	-100	-	100	uA
I _{IL_4L}	Low Level Input Leak Current	VIN=GND	-100	-	100	uA

*Must be tied for setting each level

*1 : Tie 0Ω to GND

*2 : Tie 180kΩ±5% to GND

*3 : Leave pin open

*4 : Tie 0Ω to VCC

Receiver DC/AC Specification

Table 9 Receiver DC/AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IN-DIFF-PP}	AC Coupled Differential Input Peak to Peak Signal	10Gbps PRBS9	-	-	1200	mV
R _{RX-DC}	Receiver DC Common Mode Impedance	-	-	30	-	Ω
R _{RX-DIFF-DC}	DC Differential Impedance	-	72	-	120	Ω
R _{RX-HIGH-IMP-DC-POS}	DC Input CM Input Impedance for V>0	-	25	-	-	kΩ
RL _{RX-DIFF}	Rx Differential Return Loss	0.05 to 5 GHz	-	-7	-	dB
RL _{RX-CM}	Rx Common Mode Return Loss	0.05 to 5 GHz	-	-6	-	dB

Transmitter DC / AC Specifications

Table 10 Transmitter DC / AC specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T _{TX-DJ-DD}	Deterministic Jitter	Loss=18dB@5GHz	-	0.25	-	U _{Ipp}
T _{TX-RJ-DD}	Random Jitter	-	-	0.5	-	ps RMS
T _{TX-RISE-FALL}	Tx Rise/Fall Time	20% to 80 %	-	40	-	ps
T _{RF-MISMATCH}	Tx Rise/Fall Mismatch	-	-	0.01	-	UI
RL _{TX-DIFF}	Tx Differential Return Loss ^{*1}	0.05 to 5 GHz	-	-10	-	dB
RL _{TX-CM}	Tx Common Mode Return Loss ^{*1}	0.05 to 5 GHz	-	-6	-	dB
R _{TX-DIFF-DC}	DC Differential Impedance	-	72	-	120	Ω
V _{TX-RCV-DETECT}	The Amount of Voltage Change Allowed during Receiver Detection	-	-	-	0.6	V
V _{TX-DC-CM}	Transmitter DC Common-mode Voltage	-	-	V _{CC} -0.8	-	V
V _{TX-CM-AC-PP_ACTIVE}	Transmitter AC Common-mode Voltage Active	-	-	-	100	mV _{pp}
V _{TX-IDLE-DIFF-AC-pp}	Electrical Idle Differential Peak-Peak Output Voltage	-	0	-	10	mV
V _{TX-IDLE-DIFF-DC}	DC Electrical Idle Differential Output Voltage	-	0	-	10	mV
C _{TX-PARASITIC}	Tx Input Capacitance	-	-	-	1.1	pF
T _{EN}	Power On to EN_12/34 High Delay	-	0	-	-	ns
T _{ACTIVE}	EN_12/34 High to Active Delay	-	-	-	200	us
T _{PROPAGATION}	Differential Propagation Delay	-	-	150	-	ps

*1 Confirmed evaluation board.

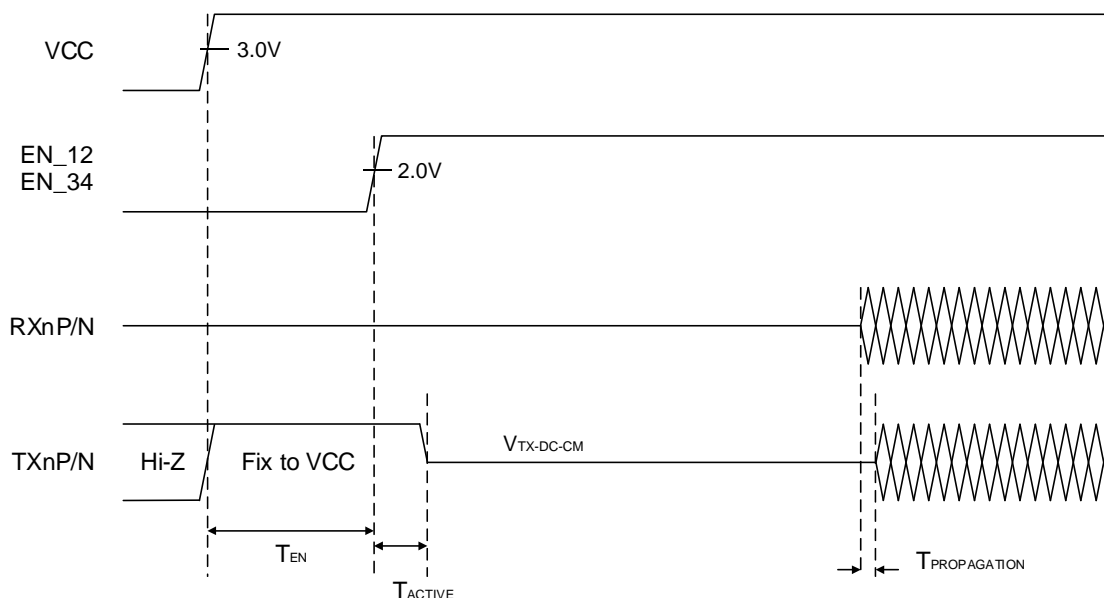
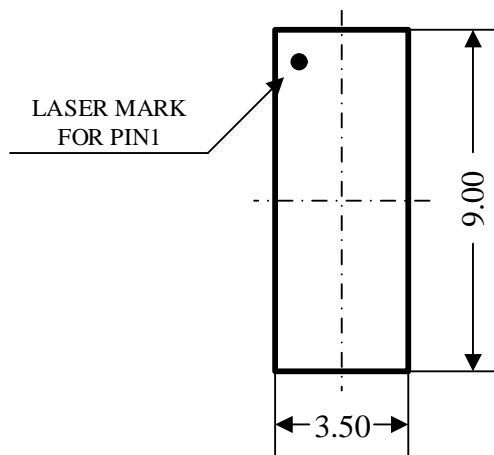


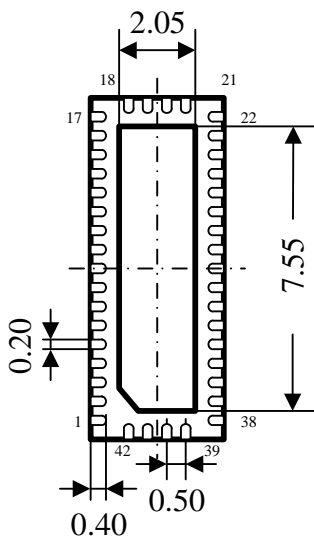
Figure 6. Power on Sequence (SignalDetect Disable/ RxDetect Disable)

Package

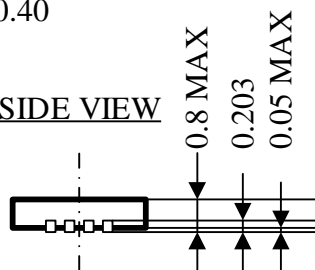
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Unit: mm

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7. Please note that this product is not designed to be radiation-proof.
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