

THCX222R10

High Performance Re-driver with Linear Equalization

General Description

THCX222R10 is a high performance bi-directional active re-driver for serial links with data rates up to 10Gbps.

THCX222R10 features a continuous time linear equalizer (CTLE) to provide a boost up to +15.6dB at 5 GHz. It opens an input eye completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums.

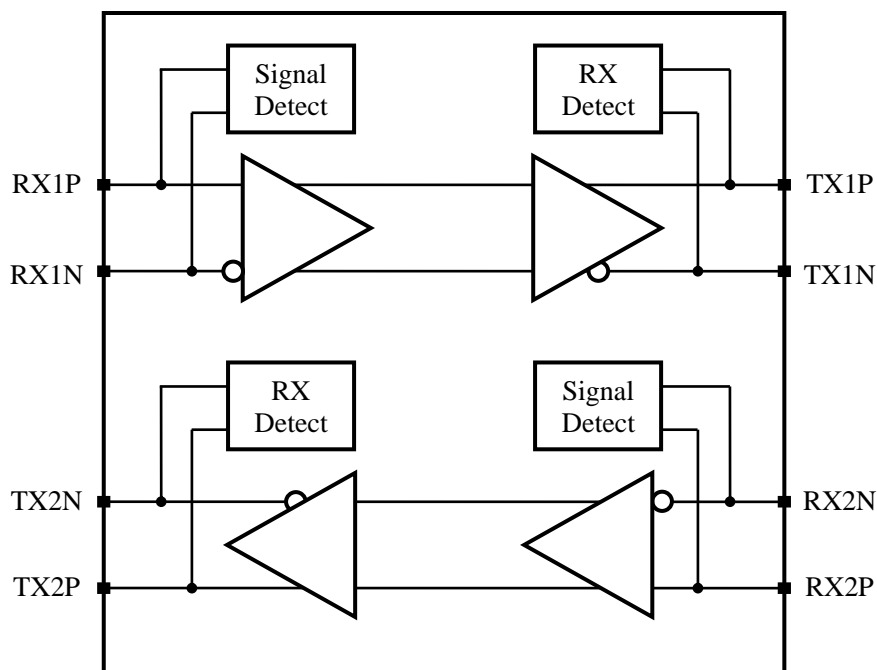
Features

- Signal Conditioning with Linear Equalizer
- Linear Equalization up to +15.6dB@5GHz
- Adjustable Voltage Output Swing Linear Range
- Adjustable Receiver Equalization and DC Gain
- Support USB 3.1 Gen2 and USB 3.2
 - Receiver and LFPS Detect
- Single Supply Voltage (3.3V)
- Package : QFN30 (2.5mm x 4.5mm)

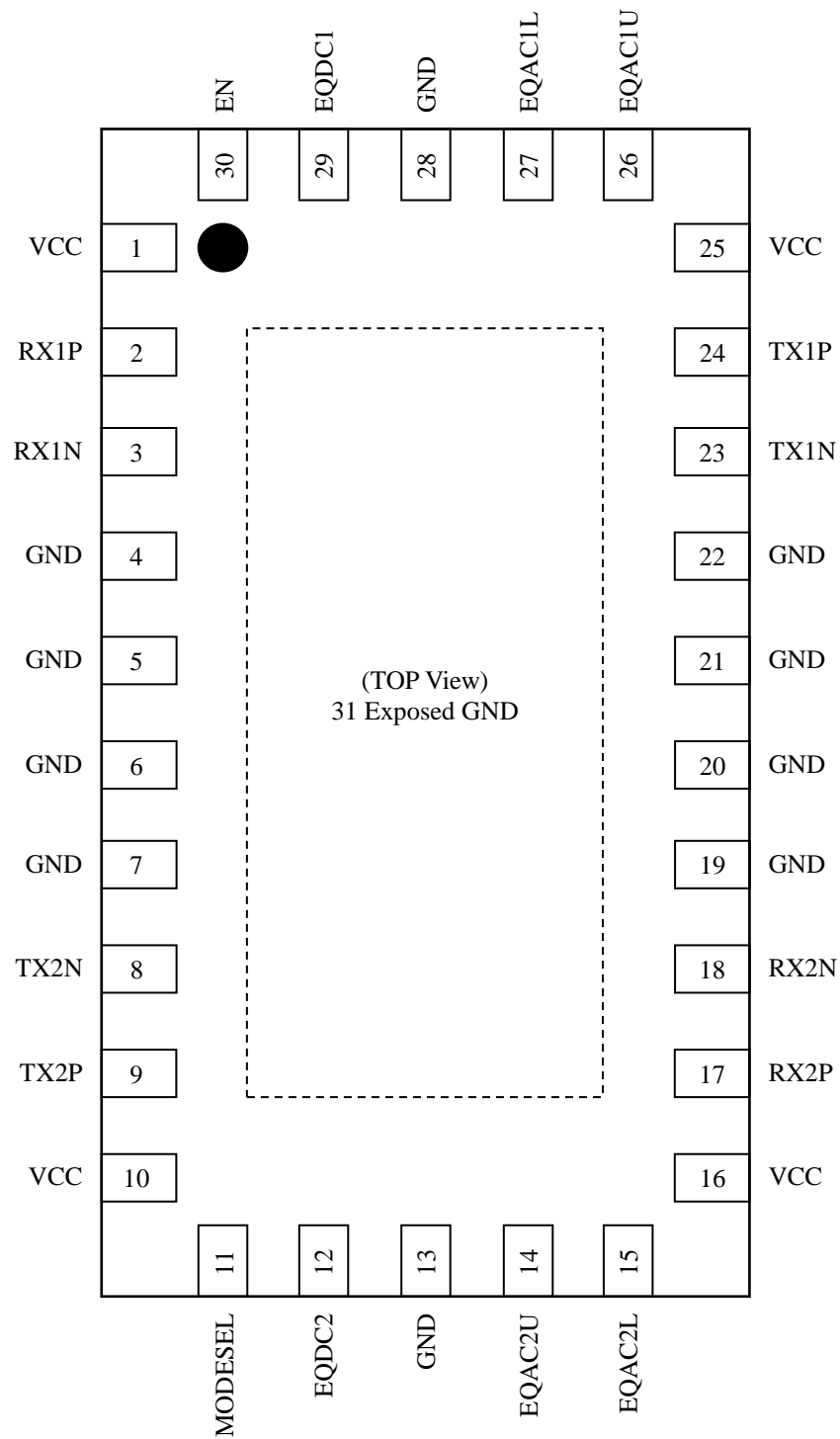
Applications

- USB 3.x
- USB Host and Devices
- Docking Stations
- Active Cable
- V-by-One® HS
- CML Interface

Block Diagram



Pin Configuration





Pin Description

Pin Name	Pin No	Type	Description
RX1P	2	CI	Super-Speed CML Signal Input of Channel1(CH1)
RX1N	3	CI	Super-Speed CML Signal Input of CH1
TX1P	24	CO	Super-Speed CML Signal Output of CH1
TX1N	23	CO	Super-Speed CML Signal Output of CH1
RX2P	17	CI	Super-Speed CML Signal Input of Channel2(CH2)
RX2N	18	CI	Super-Speed CML Signal Input of CH2
TX2P	9	CO	Super-Speed CML Signal Output of CH2
TX2N	8	CO	Super-Speed CML Signal Output of CH2
EN	30	I	Channel Enable. With internal 300kΩ Pull-up Resistor. 0 : Power Down 1 : Normal Operation
EQAC1U	26	4LI (*1)	CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1L allows for up to 16 settings.
EQAC1L	27	4LI (*1)	CH1 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC1U allows for up to 16 settings.
EQAC2U	14	4LI (*1)	CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2L allows for up to 16 settings.
EQAC2L	15	4LI (*1)	CH2 Rx Equalizer Peak Gain & High Linear Mode setting This pin along with EQAC2U allows for up to 16 settings.
EQDC1	29	4LI (*1)	CH1 Equalizer DC Gain Setting
EQDC2	12	4LI (*1)	CH2 Equalizer DC Gain Setting
MODESEL	11	4LI (*1)	Chip Operation Mode Select, if EN=1 0 : CH1/2 enable, RxDetect/SignalDetect enable R : CH1/2 enable, RxDetect enable, SignalDetect disable F : CH1/2 enable, RxDetect/SignalDetect disable 1 : CH1 enable, CH2 disable, RxDetect/SignalDetect disable
VCC	1, 10, 16, 25	PWR	Power Supply Pin for On-chip Regulator.
GND	4,5,6,7,13, 19,20,21, 22,28,31	GND	Ground. Must be tied to the PCB ground plane through an array of vias. Pin#31 is exposed pad ground.

CI: CML Input Buffer, CO: CML Output Buffer
 I: LVCMOS Input Buffer, 4LI: 4-Level LVCMOS Input Buffer,
 PWR: Power Supply, GND: Ground

*1 : 4-Level Input Buffer. With internal 180kΩ pull-up resistor and 300kΩ pull-down resistor.

Operation Mode Settings

Table 1. Operation Mode Setting

Pin Settings		Operation Mode
EN	MODESEL	
1	0(*1)	CH1/2 Enable, RxDetect Enable, SignalDetect Enable
	R(*2)	CH1/2 Enable, RxDetect Enable, SignalDetect Disable
	F(*3)	CH1/2 Enable, RxDetect Disable, SignalDetect Disable
	1(*4)	CH1 Enable, CH2 Disable, RxDetect Disable, SignalDetect Disable
0	Ignore	Chip Power Down.

*1 Tie 0Ω to GND

*2 Tie 180kΩ±5% to GND

*3 Leave pin Open

*4 Tie 0Ω to VCC

Detect Function

THCX222R10 has Input Signal Detect (SignalDetect) and Receiver Detect (RxDetect) functionality for USB3.x transmission.

Detect functionality must be disabled when it is not USB3.x application.



Liner Equalizer Settings

Table 2. Equalization and -1dB Compression Point Linear Swing Settings

EQACnU*1	EQACnL*1	EQDCn*1	Equalizer Settings (dB) @1.5GHz / 2.5GHz / 5GHz	Output Linear Swing Settings (mVppd)	
				@100MHz	@5GHz
0	0	0	1.2 / 3.0 / 7.6	830	760
0	R		1.8 / 4.1 / 9.0		
R	0		2.0 / 4.4 / 10.2		
R	R		2.6 / 5.4 / 11.3		
F	0		2.7 / 5.8 / 12.3		
F	R		3.4 / 6.7 / 13.3		
1	0		3.6 / 7.1 / 13.9		
1	R		4.2 / 7.9 / 14.5		
0	0	R	1.9 / 3.5 / 7.7	830	760
0	R		2.5 / 4.4 / 9.2		
R	0		2.6 / 4.8 / 10.3		
R	R		3.2 / 5.7 / 11.4		
F	0		3.3 / 6.1 / 12.4		
F	R		3.9 / 7.0 / 13.4		
1	0		4.1 / 7.4 / 14.0		
1	R		4.6 / 8.2 / 14.6		
0	0	F	3.0 / 4.2 / 7.6	830	760
0	R		3.5 / 5.0 / 9.2		
R	0		3.6 / 5.4 / 10.2		
R	R		4.1 / 6.1 / 11.4		
F	0		4.2 / 6.5 / 12.3		
F	R		4.7 / 7.3 / 13.2		
1	0		4.8 / 7.7 / 13.9		
1	R		5.3 / 8.4 / 14.4		
0	0	1	6.4 / 6.8 / 8.6	830	760
0	R		6.6 / 7.3 / 9.8		
R	0		6.7 / 7.6 / 10.8		
R	R		7.0 / 8.1 / 11.8		
F	0		7.1 / 8.4 / 12.7		
F	R		7.4 / 9.0 / 13.5		
1	0		7.5 / 9.3 / 14.1		
1	R		7.8 / 9.8 / 14.7		
0	F	0	2.5 / 4.3 / 8.5	1200	1000
0	1		3.2 / 5.3 / 9.9		
R	F		3.4 / 5.6 / 11.0		
R	1		4.0 / 6.5 / 12.1		
F	F		4.0 / 6.9 / 13.2		
F	1		4.7 / 7.9 / 14.1		
1	F		4.9 / 8.2 / 14.8		
1	1		5.4 / 9.0 / 15.5		
0	F	R	3.2 / 4.8 / 8.6	1200	1000
0	1		3.8 / 5.7 / 10.0		
R	F		4.0 / 6.0 / 11.1		
R	1		4.5 / 6.9 / 12.3		
F	F		4.6 / 7.2 / 13.3		
F	1		5.2 / 8.1 / 14.2		
1	F		5.3 / 8.5 / 14.9		
1	1		5.9 / 9.2 / 15.6		

Average of all channels in typical condition

*1 n=1,2

EQACnU ^{*1}	EQACnL ^{*1}	EQDCn ^{*1}	Equalizer Settings (dB) @1.5GHz / 2.5GHz / 5GHz	Output Linear Swing Settings (mVppd)	
				@100MHz	@5GHz
0	F	F	4.3 / 5.5 / 8.7	1200	1000
0	1		4.8 / 6.3 / 10.0		
R	F		4.9 / 6.6 / 11.0		
R	1		5.4 / 7.3 / 12.2		
F	F		5.5 / 7.7 / 13.2		
F	1		5.9 / 8.5 / 14.1		
1	F		6.1 / 8.8 / 14.7		
1	1		6.5 / 9.5 / 15.4		
0	F	1	7.7 / 8.1 / 9.5	1200	1000
0	1		8.0 / 8.6 / 10.7		
R	F		8.1 / 8.8 / 11.6		
R	1		8.3 / 9.3 / 12.7		
F	F		8.4 / 9.6 / 13.5		
F	1		8.7 / 10.1 / 14.4		
1	F		8.8 / 10.4 / 15.0		
1	1		9.0 / 10.9 / 15.6		

Average of all channels in typical condition

*1 n=1,2

Table 3. Flat Gain Settings

EQDCn ^{*1}	Flat Gain Settings (dB)@Up to 300MHz	
	EQACn ^{*1} U=0/R	EQACn ^{*1} U=F/1
0	-2.6	-1.2
R	-1.7	-0.3
F	-0.2	1.3
1	3.8	5.2

Average of all channels in typical condition

*1 n=1,2

-1dB Compression Point is showed below. It means output voltage range that has linearity.

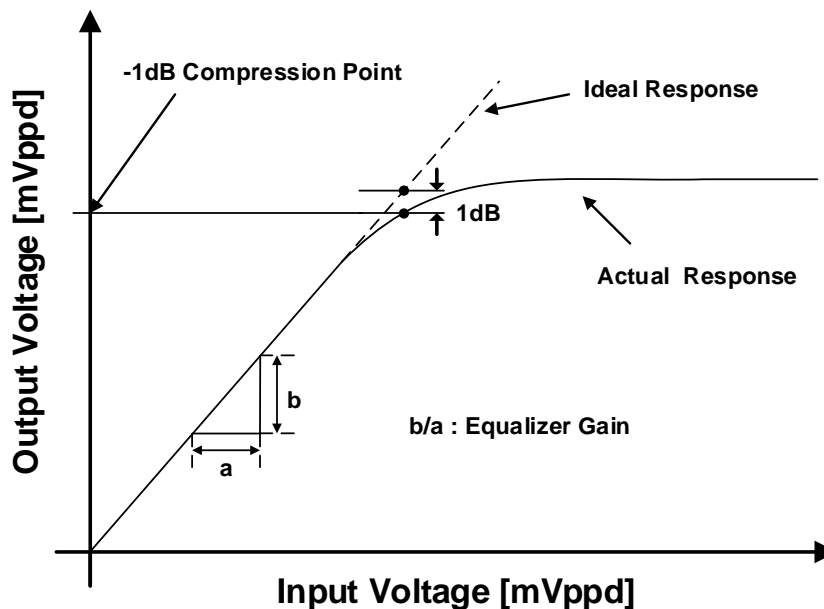


Figure 1. -1dB Compression Point

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	-0.3	-	4.0	V
LVC MOS Input/Output Voltage	-0.3	-	VCC+0.3	V
4-Level LVC MOS Input Voltage	-0.3	-	VCC+0.3	V
CML Receiver Input Voltage	-0.3	-	VCC+0.3	V
CML Transmitter Output Voltage	-0.3	-	VCC+0.3	V
ESD Rating	HBM	-	±4	kV
	MM	-	±200	V
	CDM	-	±1000	V
Storage Temperature	-55	-	125	°C
Junction Temperature	-	-	125	°C
Reflow Peak Temperature/Time	-	-	260/10	°C/sec

Recommended Operating Conditions

Table 5. Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	3.0	3.3	3.6	V
Supply Ramp Requirement	0.1	-	50	ms
Operating Temperature	-40	-	85	°C

Equivalent CML Input Schematic Diagram

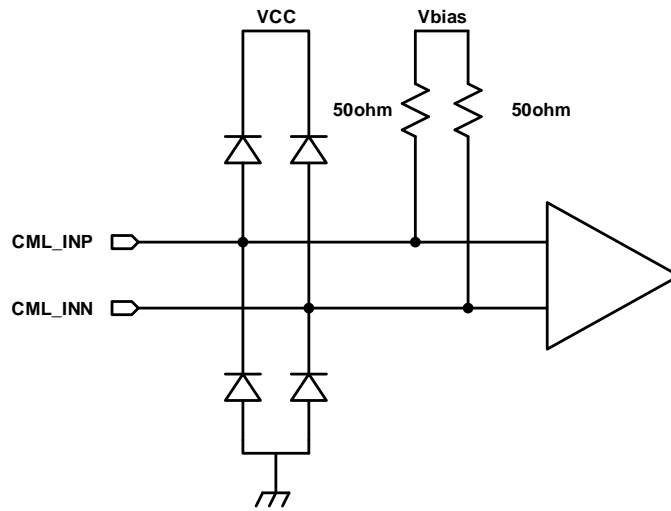


Figure 2. CML Input Schematic Diagram

Equivalent CML Output Schematic Diagram

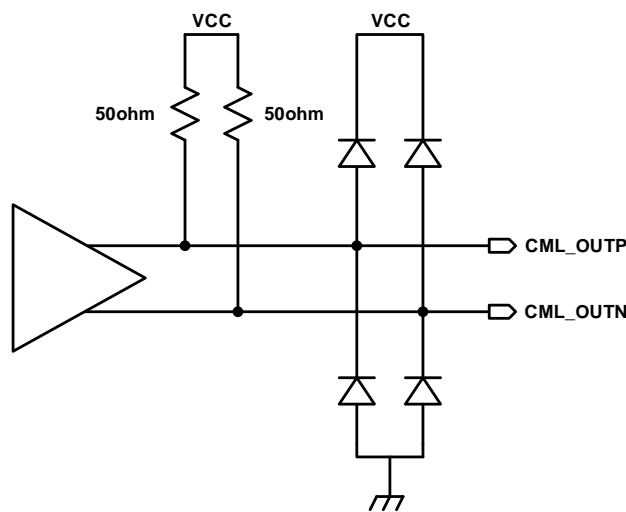


Figure 3. CML Output Schematic Diagram

Equivalent LVC MOS Input Schematic Diagram

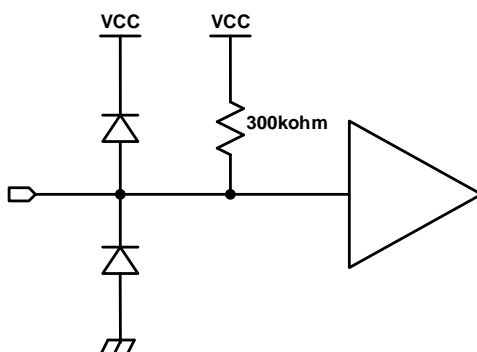


Figure 4. LVC MOS Input Schematics Diagram

Equivalent 4-Level LVC MOS Input Schematic Diagram

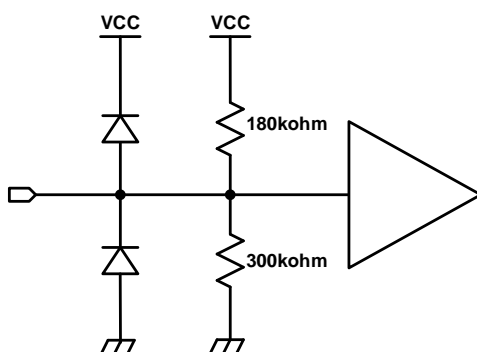


Figure 5. 4-Level Input Schematics Diagram



Electrical Specification

Supply Current

Table 6. Supply Current

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCW	Active Mode Supply Current	EQACn ¹ U=F/1	-	84	150	mA
		EQACn ¹ U=0/R	-	69	123	mA
ICCSL	Slumber Mode Supply Current	-	-	45	65	mA
ICCI	Unplug Mode Supply Current	-	-	1.2	2.9	mA
ICCS	Power Down Supply Current	-	-	120	180	uA

*1 n=1,2

LVC MOS DC Specification

Table 7. LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	-	2.0	-	VCC	V
VIL	Low Level Input Voltage	-	0	-	0.7	V

4-Level LVC MOS DC Specification

Table 8. 4-Level LVC MOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{THL}	Low Level Input Voltage	0(*1)	0	-	VCC*0.25 - 0.3	V
V _{THR}	R-Level Input Voltage	R(*2)	VCC*0.25 + 0.3	-	VCC*0.5 - 0.3	V
V _{THF}	F-Level Input Voltage	F(*3)	VCC*0.5 + 0.3	-	VCC*0.75 - 0.3	V
V _{THH}	High Level Input Voltage	1(*4)	VCC*0.75 + 0.3	-	VCC	V
I _{IH_4L}	High level Input Leak Current	VIN=VCC	-100	-	100	uA
I _{IL_4L}	Low Level Input Leak Current	VIN=GND	-100	-	100	uA

*Must be tied for setting each level

*1 : Tie 0Ω to GND

*2 : Tie 180kΩ±5% to GND

*3 : Leave pin open

*4 : Tie 0Ω to VCC

Receiver DC/AC Specification

Table 9. Receiver DC/AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IN-DIFF-PP}	AC Coupled Differential Input Peak to Peak Signal	10Gbps PRBS9	-	-	1200	mV
R _{RX-DC}	Receiver DC Common Mode Impedance	-	-	30	-	Ω
R _{RX-DIFF-DC}	DC Differential Impedance	-	72	100	120	Ω
R _{RX-HIGH-IMP-DC-POS}	DC Input Common Mode Input Impedance for V>0	-	25	-	-	kΩ
R _{LRX-DIFF}	Rx Differential Return Loss	0.05 to 5 GHz	-	-7	-	dB
R _{LRX-CM}	Rx Common Mode Return Loss	0.05 to 5 GHz	-	-6	-	dB

Transmitter DC / AC Specifications

Table 10. Transmitter DC / AC specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T _{TX-DJ-DD}	Deterministic Jitter	Loss=18dB@5GHz	-	0.25	-	UIpp
T _{TX-RJ-DD}	Random Jitter	-	-	0.5	-	ps RMS
T _{TX-RISE-FALL}	Tx Rise/Fall Time	20% to 80 %	-	40	-	ps
T _{RF-MISMATCH}	Tx Rise/Fall Mismatch	-	-	0.01	-	UI
R _{LTX-DIFF}	Tx Differential Return Loss ^{*1}	0.05 to 5 GHz	-	-10	-	dB
R _{LTX-CM}	Tx Common Mode Return Loss ^{*1}	0.05 to 5 GHz	-	-6	-	dB
R _{TX-DIFF-DC}	DC Differential Impedance	-	72	100	120	Ω
V _{TX-RCV-DETECT}	The Amount of Voltage Change Allowed during Receiver Detection	-	-	-	0.6	V
V _{TX-DC-CM}	Transmitter DC Common Mode Voltage	-	-	1.9	-	V
V _{TX-CM-AC-PP_ACTIVE}	Transmitter AC Common Mode Voltage Active	-	-	-	100	mVpp
V _{TX-IDLE-DIFF-AC-pp}	Electrical Idle Differential Peak-Peak Output Voltage	-	0	-	10	mV
V _{TX-IDLE-DIFF-DC}	DC Electrical Idle Differential Output Voltage	-	0	-	10	mV
C _{TX-PARASITIC}	Tx Input Capacitance	-	-	-	1.1	pF
T _{EN}	Power On to EN High Delay	-	0	-	-	ns
T _{ACTIVE}	EN High to Active Delay	-	-	-	200	us
T _{PROPAGATION}	Differential Propagation Delay	-	-	150	-	ps

*1 Confirmed evaluation board.

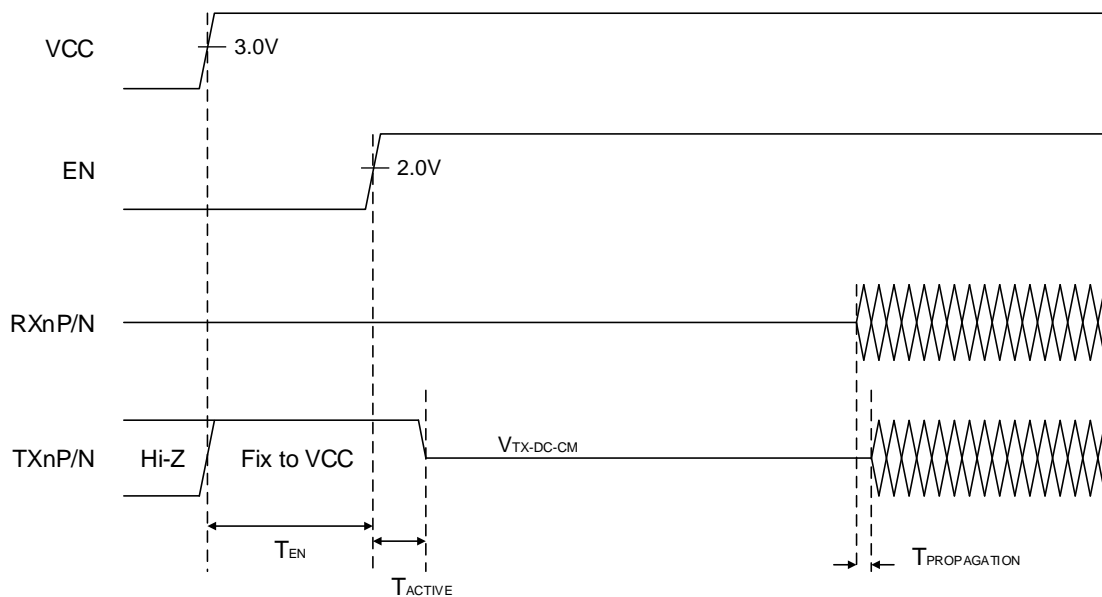
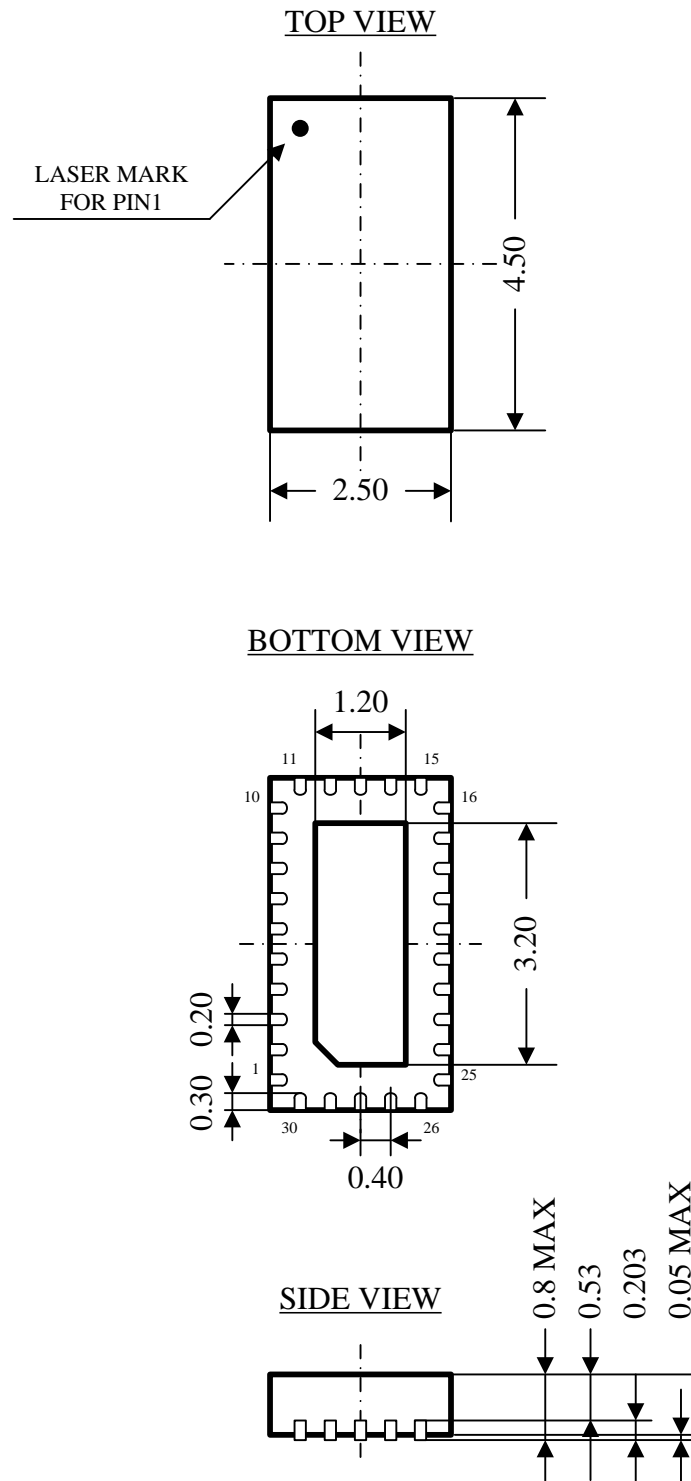


Figure 6. Power on Sequence (SignalDetect Disable/ RxDetect Disable)

n=1,2

Package



Unit: mm

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THine Electronics, Inc.

sales@thine.co.jp

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