V-by-One® HS plus Standard

Version 1.01

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1. Introduction

1.1. Objectives

This document constitutes the standard for the video by one high speed plus(V-by-One® HS plus).

- ✔ V-by-One® HS plus targets a high speed data transmission of video signals based on the internal connection of equipment.
- ✔ V-by-One® HS plus pursues easier usage and lower power consumption compared with the current internal connection.
- ✔ V-by-One® HS plus supports up to 8Gbps data rate.
- ✔ V-by-One® HS plus supports scrambling and Clock Data Recovery (CDR) to reduce EMI.
- ✔ V-by-One® HS plus supports CDR to solve the skew problem between the clock and data.

1.2. Technical Overview

With V-by-One® HS plus proprietary encoding/decoding scheme and CDR architecture, V-by-One® HS plus technology enables the transmission up to 40bit Pixel Data, up to 24bit Control Data (CTL), Hsync, Vsync, and Data Enable (DE) by some differential pair cables with minimal external components.

As shown in Figure 1, V-by-One® HS plus link includes data lanes, Hot Plug Detect signal (HTPDN), and CDR Lock signal (LOCKN). The number of data lanes is depended on the pixel rate and color depth (refer to Table 5). HTPDN connection between the transmitter and receiver can be omitted as an application option. V-by-One® HS plus technology implements the transmitter emphasis and receiver equalizer.

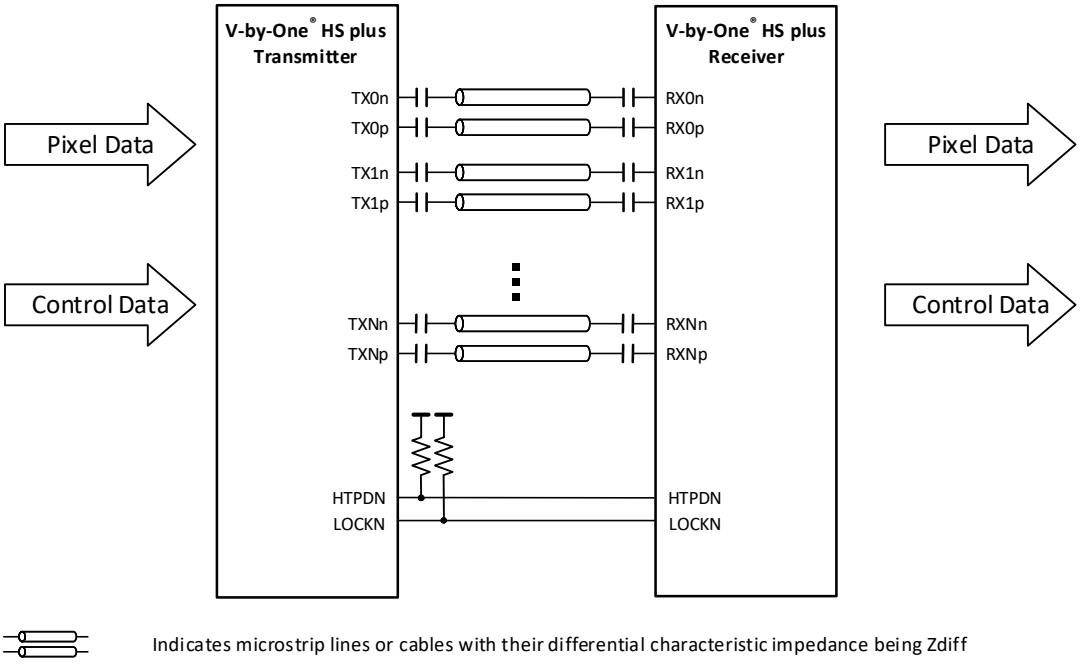

Figure 1 V-by-One® HS plus Link System Diagram

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1.2.1. Transmitter

V-by-One® HS plus transmitter consists of packer, scrambler, encoder, serializer, and transmitter link monitor (refer to Figure 5). The transmitter link monitor constantly checks LOCKN and HTPDN signals. If the LOCKN signal is high, the transmitter executes the CDR training. The transmitter sends the CDR training pattern during the CDR training mode. When CDR is locked, the transmitter shifts from the CDR training mode to the normal mode, and then it starts to transmit input data from user logic.

1.2.2. Receiver

V-by-One® HS plus receiver consists of unpacker, de-scrambler, decoder, de-serializer, and receiver link monitor. The receiver synchronizes the pixel clock by referring to the CDR training pattern in the CDR training mode. After shifting from the CDR training mode to the normal mode, the receiver aligns byte and pixel header position using ALN training pattern. About ALN training, refer to Chapter 2.2.5.2.

1.2.3. Transmission Mode Setting

V-by-One® HS plus transmission mode is defined as below.

$$\mathrm{FR}\left(\begin{matrix}\mathrm{HS}\\ \mathrm{HSP}\end{matrix}\right)\_\mathrm{COL}\left(\begin{matrix}06\\ 08\\ 10\\ 12\end{matrix}\right)\_\mathrm{ENC}\left(\begin{matrix}\mathrm{SE}\\ \mathrm{EE}\end{matrix}\right)\_\mathrm{RCH}\left(\begin{matrix}\mathrm{SR}\\ \mathrm{MR}\\ \mathrm{LR}\end{matrix}\right)$$

1.2.3.1. Frequency Range (FR)

FR(HSP) and FR(HS) mean the frequency range.

Table 1 Frequency Range Definition

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
FR(HS)	V-by-One® HS mode	-	0.6	-	4.0	Gbps
FR(HSP)	V-by-One® HS plus mode	-	0.6	-	8.0	Gbps

1.2.3.2. Color Depth (COL)

COL(06), COL(08), COL(10), and COL(12) stand for color depth.

Table 2 Color Depth Definition

Symbol	Parameter	Conditions	Color Depth	Unit
COL(06)	6bit / color	-	18	bit
COL(08)	8bit / color	-	24	bit
COL(10)	10bit / color	-	30	bit
COL(12)	12bit / color	-	36	bit

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1.2.3.3. Encoding (ENC)

ENC(SE) and ENC(EE) mean the encoding scheme. ENC(SE) is 8b/10b encoding scheme. It is the same as V-by-One® HS. ENC(EE) is higher efficiency encoding scheme than 8b/10b (option for future use).

Table 3 Encoding Definition

Symbol	Parameter	Conditions
ENC(SE)	Standard Encoding (8b/10b)	-
ENC(EE)	Enhanced Encoding (T.B.D.)	option for future use

1.2.3.4. Reach (RCH)

RCH(SR), RCH(MR) and RCH(LR) mean channel loss. V-by-One® HS plus has three different PHY specification corresponding to each of RCH(SR), RCH(MR) and RCH(LR) (refer to Chapter 3).

Table 4 Reach Definition

Symbol	Parameter	Conditions
RCH(SR)	Short Reach	-
RCH(MR)	Middle Reach	
RCH(LR)	Long Reach	-

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1.2.4. Data Lane

Transmission rate is able to be set up to 8Gbps depended on video pixel clock rate and color depth.

1.2.4.1. Recommended Data Lane

Table 5 Example of Video Data Format vs. Number of Lane

Resolution	Refresh Rate (pixel clock)	Color Depth [bit]	Number of Data Lanes*1		Packer Clock*2 [MHz/lane]	
			FR(HSP)	FR(HS)	FR(HSP)	FR(HS)
Full HD (1920 x 1080p)	120Hz (297MHz)	24/30/36	2	4	148.5	74.25
	240Hz (594MHz)	24/30/36	4	8	148.5	74.25
Cinema Full HD (2560 x 1080p)	120Hz (370MHz)	24/30/36*3	2	4	185	92.5
	240Hz (740MHz)	24/30/36*3	4	8	185	92.5
4K2K (3840 x 2160p)	60Hz (594MHz)	24/30/36	4	8	148.5	74.25
	120Hz (1188MHz)	24/30/36	8	16	148.5	74.25
	144Hz (1425.6MHz)	24/30/36*3	8	16	178.2	89.1
	165Hz (1633.5MHz)	24/30/36	16	32	102.1	51.05
	240Hz (2376MHz)	24/30/36	16	32	148.5	74.25
5K UHD TV (5120 x 2160p)	60Hz (740MHz)	24/30/36*3	4	8	185	92.5
	120Hz (1480MHz)	24/30/36*3	8	16	185	92.5
8K4K (7680 x 4320p)	60Hz (2376MHz)	24/30/36	16	32	148.5	74.25
	120Hz (4752MHz)	24/30/36	32	64	148.5	74.25
10K QUHD TV (10240 x 4320p)	60Hz (2160MHz)	24/30/36*3	16	32	185	92.5
	120Hz (5620MHz)	24/30/36*3	32	64	185	92.5

*1 other lane numbers could be chosen; however, for the interoperability, the above numbers are STRONGLY recommended.

*2 refer to Chapter 1.2.4.2 about a definition of packer clock.

*3 ENC(EE) mode would be adequate for 36bit color depth.

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1.2.4.2. Data Lane Consideration

This chapter is informative only. It shows the procedure to select the minimum and maximum number of lanes necessary for the target application

$$\mathrm{FR}\begin{pmatrix}\mathrm{HS}\\ \mathrm{HSP}\end{pmatrix}\_\mathrm{COL}\begin{pmatrix}06\\ 08\\ 10\\ 12\end{pmatrix}\_\mathrm{ENC}\begin{pmatrix}\mathrm{SE}\\ \mathrm{EE}\end{pmatrix}\_\mathrm{RCH}\begin{pmatrix}\mathrm{SR}\\ \mathrm{MR}\\ \mathrm{LR}\end{pmatrix}$$

As a 1st step, [Color Encoding] is decided in the following procedure. [Color Mode] is chosen from 06, 08, 10 or 12 depending upon color depth. [Encoding] is chosen from ENC(SE) or ENC(EE) depending upon display size and aspect ratio. ENC(EE) is suitable for cinema display size. When these parameters are chosen, [Color Encoding] is decided according to Table 6.

Table 6 Color/Encoding Factor [Color Encoding]

Symbol		Encoding		Unit
		ENC(SE)	ENC(EE)	
Color	COL(06)	30	T.B.D.	bit
	COL(08)	30	T.B.D.	bit
	COL(10)	40	T.B.D.	bit
	COL(12)	50	T.B.D.	bit

As a 2nd step, [encoded total bit rate] is calculated in the following procedure. Total bit rate which is physically transmitted on V-by-One® HS plus line can be estimated. Multiplying [pixel clock] of the target application by encoded data amount per pixel results into [encoded total bit rate] of V-by-One® HS plus transmission.

$$[\text{encoded total bit rate}](\text{bps}) = [\text{Color Encoding}](\text{bit}) \times [\text{pixel clock}](\text{Hz})$$

As a result, [encoded bit rate per lane] and [packer clock] are calculated in the following procedure. [encoded bit rate per lane] can be calculated as [total bit rate] over [number of data lanes]. [number of data lanes] should be chosen properly so that [encoded bit rate per lane] is above 0.6Gbps and below 8Gbps.

$$[\text{encoded bit rate per lane}](\text{bps/lane}) = \frac{[\text{encoded total bit rate}](\text{bps})}{[\text{number of data lanes}]}$$

$$= \frac{[\text{Color Encoding }](\text{bit}) \times [\text{pixel clock}](\text{Hz})}{[\text{number of data lanes}]}$$

[packer clock] is defined as follows,

$$\frac{[\text{pixel clock}](\text{Hz})}{[\text{number of data lanes}]} = [\text{packer clock}](\text{Hz/lane})$$

Therefore,

$$[\text{encoded bit rate per lane}](\text{bps/lane}) = [\text{Color Encoding}](\text{bit}) \times [\text{packer clock}](\text{Hz/lane})$$

[packer clock] should be selected appropriately for signal handling in applications.

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In FR(HSP) mode, [encoded bit rate per lane] should be above 0.6Gbps and below 8.0Gbps.

$$0.6\text{Gbps} \leq [\text{encoded bit rate per lane}](\text{bps/lane}) \leq 8.0\text{Gbps}$$

In FR(HS) mode, [encoded bit rate per lane] should be above 0.6Gbps and below 4.0Gbps.

$$0.6\text{Gbps} \leq [\text{encoded bit rate per lane}](\text{bps/lane}) \leq 4.0\text{Gbps}$$

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1.2.5. Hot Plug Detect Signal (HTPDN)

HTPDN indicates the connecting condition between the transmitter and receiver. HTPDN of the transmitter side is high when the receiver is not active or not connected. Then the transmitter can enter into the power down mode. HTPDN is set to low by the receiver when the receiver is active and connected with the transmitter, and then the transmitter must start up and transmit CDR training pattern for link training. HTPDN is the open drain output at the receiver side. Pull-up resistor is needed at the transmitter side (refer to Figure 1).

In RCH(SR) mode, HTPDN connection between the transmitter and receiver may be omitted as an application option. In this case shown on Figure 2, HTPDN at the transmitter side is fixed low.

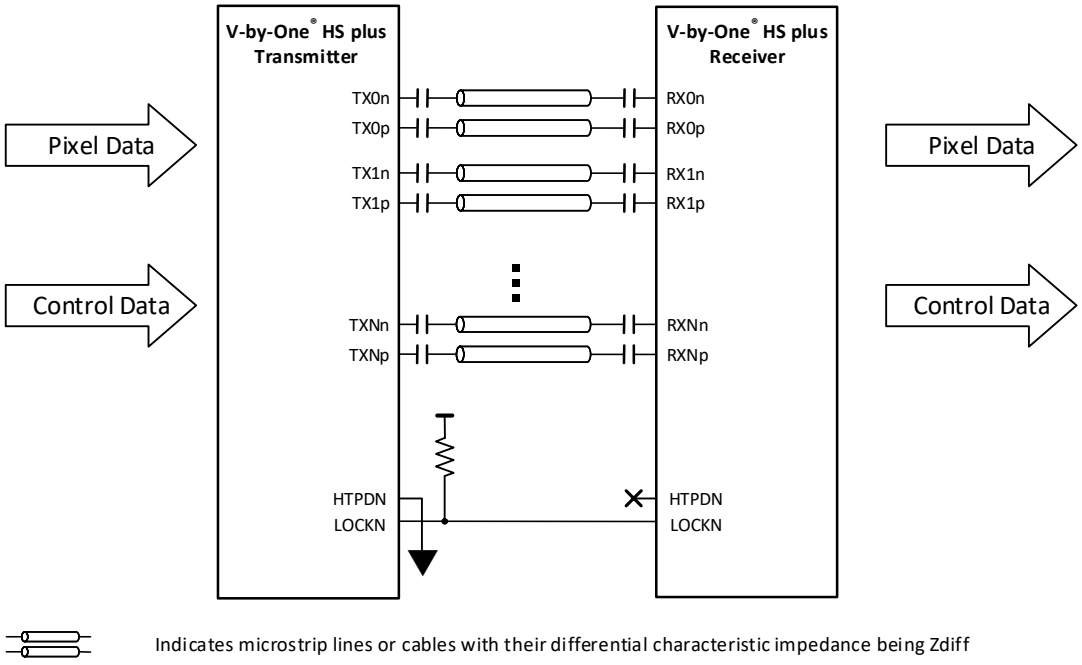

Figure 2 V-by-One® HS plus Link System without HTPDN Connection Schematic Diagram

1.2.6. LOCKN Signal

LOCKN indicates whether the CDR is in the lock state or not. LOCKN at the transmitter input is set to high by a pull-up resistor when the receiver is not active or at the CDR training state. LOCKN is set to low by the receiver when CDR lock is done. Then the CDR training mode finishes, and the transmitter shifts to the normal mode. LOCKN is the open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered after the HTPDN is pulled into low by the receiver.

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5. Connector and Cable

This chapter shows guideline of connector and cable to connect the V-by-One® HS plus transmitter (e.g. Video processing unit) and receiver (e.g. Panel module).

5.1. Pin Assignments

5.1.1. SSGSS Pin Assignment

In terms of pin assignment, SSGSS means “Signal-Signal-Ground-Signal-Signal” assignment.

Some systems might require a lot of user option, power supply pins and V-by-One® HS plus lanes at the same time.

Reduced ground format is applied to such a case. Compared with SSGGSS format signal integrity gets worse in general; therefore, user must pay attention to achieve transmission quality between transmitter and receiver, incorporated in PCB design, and connector/harness selection.

The power supply should be constructed by another dedicated cable separated from V-by-One® HS plus high speed lanes when system needs to transmit large current capacity between transmitter side and receiver side.

Note:

Some cable like Flexible Printed Circuits (FPC) may not have the symmetric conductor layout. This means that if users connect the cable at reverse direction, i.e. Rx plug is connected to transmitter’s receptacle and Tx plug to receiver’s receptacle, the correct connection cannot be achieved. Users must pay attention to the cable direction.

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5.1.1.1. FR(HSP) mode for 4K120Hz

Table 36 shows the 31 pin assignment in FR(HSP) mode for 4K120Hz. In this mode, it can be assigned 4 optional pins in the cable. On the other hand, the power supply should be connected by using another cable to support large current capacity.

Table 36 SSGSS(31pin) Pin Assignment in FR(HSP) mode for 4K120Hz

Pin No (TX)	31pins	Pin No (RX)
31	(Option)	1
30	(Option)	2
29	(Option)	3
28	(Option)	4
27	LOCKN	5
26	HTPDN	6
25	GND	7
24	Rx0n	8
23	Rx0p	9
22	GND	10
21	Rx1n	11
20	Rx1p	12
19	GND	13
18	Rx2n	14
17	Rx2p	15
16	GND	16
15	Rx3n	17
14	Rx3p	18
13	GND	19
12	Rx4n	20
11	Rx4p	21
10	GND	22
9	Rx5n	23
8	Rx5p	24
7	GND	25
6	Rx6n	26
5	Rx6p	27
4	GND	28
3	Rx7n	29
2	Rx7p	30
1	GND	31

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Table 37 shows the 41 pin assignment in FR(HSP) mode for 4K120Hz. In this mode, it can be assigned 14 optional pins in the cable. On the other hand, the power supply should be connected by using another cable to support large current capacity.

Table 37 SSGSS(41pin) Pin Assignment in FR(HSP) mode for 4K120Hz

Pin No (TX)	41pins	Pin No (RX)
41	(Option)	1
40	(Option)	2
39	(Option)	3
38	(Option)	4
37	(Option)	5
36	(Option)	6
35	(Option)	7
34	(Option)	8
33	(Option)	9
32	(Option)	10
31	(Option)	11
30	(Option)	12
29	(Option)	13
28	(Option)	14
27	LOCKN	15
26	HTPDN	16
25	GND	17
24	Rx0n	18
23	Rx0p	19
22	GND	20
21	Rx1n	21
20	Rx1p	22
19	GND	23
18	Rx2n	24
17	Rx2p	25
16	GND	26
15	Rx3n	27
14	Rx3p	28
13	GND	29
12	Rx4n	30
11	Rx4p	31
10	GND	32
9	Rx5n	33
8	Rx5p	34
7	GND	35
6	Rx6n	36
5	Rx6p	37
4	GND	38
3	Rx7n	39
2	Rx7p	40
1	GND	41

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Table 38 shows the 51 pin assignment in FR(HSP) mode for 4K120Hz. In this mode, it can be assigned 24 optional pins in the cable. On the other hand, the power supply should be connected by using another cable to support large current capacity.

Table 38 SSGSS(51pin) Pin Assignment in FR(HSP) mode for 4K120Hz

Pin No (TX)	51pins	Pin No (RX)
51	(Option)	1
50	(Option)	2
49	(Option)	3
48	(Option)	4
47	(Option)	5
46	(Option)	6
45	(Option)	7
44	(Option)	8
43	(Option)	9
42	(Option)	10
41	(Option)	11
40	(Option)	12
39	(Option)	13
38	(Option)	14
37	(Option)	15
36	(Option)	16
35	(Option)	17
34	(Option)	18
33	(Option)	19
32	(Option)	20
31	(Option)	21
30	(Option)	22
29	(Option)	23
28	(Option)	24
27	LOCKN	25
26	HTPDN	26
25	GND	27
24	Rx0n	28
23	Rx0p	29
22	GND	30
21	Rx1n	31
20	Rx1p	32
19	GND	33
18	Rx2n	34
17	Rx2p	35
16	GND	36
15	Rx3n	37
14	Rx3p	38
13	GND	39
12	Rx4n	40
11	Rx4p	41
10	GND	42
9	Rx5n	43
8	Rx5p	44
7	GND	45
6	Rx6n	46
5	Rx6p	47
4	GND	48
3	Rx7n	49
2	Rx7p	50
1	GND	51

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5.1.1.2. FR(HSP) mode for 8K60Hz

Table 39 shows the 51 pin assignment in FR(HSP) mode for 8K60Hz. In this mode, both the power supply and option pin should be connected by using another cable to support large current capacity.

Table 39 SSGSS(51pin) Pin Assignment in FR(HSP) mode for 8K60Hz

Pin No (TX)	51pins	Pin No (RX)
51	LOCKN	1
50	HTPDN	2
49	GND	3
48	Rx0n	4
47	Rx0p	5
46	GND	6
45	Rx1n	7
44	Rx1p	8
43	GND	9
42	Rx2n	10
41	Rx2p	11
40	GND	12
39	Rx3n	13
38	Rx3p	14
37	GND	15
36	Rx4n	16
35	Rx4p	17
34	GND	18
33	Rx5n	19
32	Rx5p	20
31	GND	21
30	Rx6n	22
29	Rx6p	23
28	GND	24
27	Rx7n	25
26	Rx7p	26
25	GND	27
24	Rx8n	28
23	Rx8p	29
22	GND	30
21	Rx9n	31
20	Rx9p	32
19	GND	33
18	Rx10n	34
17	Rx10p	35
16	GND	36
15	Rx11n	37
14	Rx11p	38
13	GND	39
12	Rx12n	40
11	Rx12p	41
10	GND	42
9	Rx13n	43
8	Rx13p	44
7	GND	45
6	Rx14n	46
5	Rx14p	47
4	GND	48
3	Rx15n	49
2	Rx15p	50
1	GND	51

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5.2. Interoperability Order of Priority

For interoperability, the following points are STRONGLY RECOMMENDED to be paid attention to. The pin assignment of V-by-One® HS plus transmission is absolutely irreplaceable and it should be fixed.

✓ V-by-One® HS plus Hot plug detect

✓ V-by-One® HS plus Lock detect

✓ V-by-One® HS plus Ground

✓ V-by-One® HS plus Lane

The following is an example of 8 lane case. V-by-One® HS plus related pin assignment should be kept.

Table 40 Irreplaceable V-by-One® HS plus Transmission Signal on 41 Pin Assignment in FR(HSP) mode

TX side		Desicritption	RX side	
Pin No	symbol		symbol	Pin No
41	(Option)	(user option signal)	(Option)	1
40	(Option)	(user option signal)	(Option)	2
39	(Option)	(user option signal)	(Option)	3
38	(Option)	(user option signal)	(Option)	4
37	(Option)	(user option signal)	(Option)	5
36	(Option)	(user option signal)	(Option)	6
35	(Option)	(user option signal)	(Option)	7
34	(Option)	(user option signal)	(Option)	8
33	(Option)	(user option signal)	(Option)	9
32	(Option)	(user option signal)	(Option)	10
31	(Option)	(user option signal)	(Option)	11
30	(Option)	(user option signal)	(Option)	12
29	(Option)	(user option signal)	(Option)	13
28	(Option)	(user option signal)	(Option)	14
27	LOCKN	V-by-One HS plus Lock detect signal	LOCKN	15
26	HTPDN	V-by-One HS plus Hot plug detect signal	HTPDN	16
25	GND	Ground	GND	17
24	Tx0n	V-by-One HS plus Lane0	Rx0n	18
23	Tx0p	V-by-One HS plus Lane0	Rx0p	19
22	GND	Ground	GND	20
21	Tx1n	V-by-One HS plus Lane1	Rx1n	21
20	Tx1p	V-by-One HS plus Lane1	Rx1p	22
19	GND	Ground	GND	23
18	Tx2n	V-by-One HS plus Lane2	Rx2n	24
17	Tx2p	V-by-One HS plus Lane2	Rx2p	25
16	GND	Ground	GND	26
15	Tx3n	V-by-One HS plus Lane3	Rx3n	27
14	Tx3p	V-by-One HS plus Lane3	Rx3p	28
13	GND	Ground	GND	29
12	Tx4n	V-by-One HS plus Lane4	Rx4n	30
11	Tx4p	V-by-One HS plus Lane4	Rx4p	31
10	GND	Ground	GND	32
9	Tx5n	V-by-One HS plus Lane5	Rx5n	33
8	Tx5p	V-by-One HS plus Lane5	Rx5p	34
7	GND	Ground	GND	35
6	Tx6n	V-by-One HS plus Lane6	Rx6n	36
5	Tx6p	V-by-One HS plus Lane6	Rx6p	37
4	GND	Ground	GND	38
3	Tx7n	V-by-One HS plus Lane7	Rx7n	39
2	Tx7p	V-by-One HS plus Lane7	Rx7p	40
1	GND	Ground	GND	41

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If power is supplied via a cable, the following guideline should be observed.

✓ Power pins should be placed from Rx pin No. 1.

✓ Minimum number of power pins are defined but other option pins can be assigned to power pins.

✓ User needs to pay attention to the effect of power supply noise on V-by-One® HS plus lane.

The following is an example of 8 lane case. Power supply pin assignment should be from Rx pin No. 1.

Table 41 Irreplaceable Power Supply Pins on 41 Pin Assignment in FR(HSP) mode

TX side		Desicritption	RX side	
Pin No	symbol		symbol	Pin No
41	Vcc	Supply voltage for module	Vcc	1
40	Vcc	Supply voltage for module	Vcc	2
39	Vcc	Supply voltage for module	Vcc	3
38	Vcc	Supply voltage for module	Vcc	4
37	(Option)	(user option signal)	(Option)	5
36	(Option)	(user option signal)	(Option)	6
35	(Option)	(user option signal)	(Option)	7
34	(Option)	(user option signal)	(Option)	8
33	(Option)	(user option signal)	(Option)	9
32	(Option)	(user option signal)	(Option)	10
31	(Option)	(user option signal)	(Option)	11
30	(Option)	(user option signal)	(Option)	12
29	(Option)	(user option signal)	(Option)	13
28	(Option)	(user option signal)	(Option)	14
27	LOCKN	V-by-One HS plus Lock detect signal	LOCKN	15
26	HTPDN	V-by-One HS plus Hot plug detect signal	HTPDN	16
25-1	-	-	-	17-41

If a system needs more power supply, option pins can be assigned to Vcc pins as power supply.

Table 42 Expanded Power Supply Example on 41 Pin Assignment in FR(HSP) mode

TX side		Desicritption	RX side	
Pin No	symbol		symbol	Pin No
41	Vcc	Supply voltage for module	Vcc	1
40	Vcc	Supply voltage for module	Vcc	2
39	Vcc	Supply voltage for module	Vcc	3
38	Vcc	Supply voltage for module	Vcc	4
37	Vcc	Supply voltage for module	Vcc	5
36	Vcc	Supply voltage for module	Vcc	6
35	Vcc	Supply voltage for module	Vcc	7
34	Vcc	Supply voltage for module	Vcc	8
33	(Option)	(user option signal)	(Option)	9
32	(Option)	(user option signal)	(Option)	10
31	(Option)	(user option signal)	(Option)	11
30	(Option)	(user option signal)	(Option)	12
29	(Option)	(user option signal)	(Option)	13
28	(Option)	(user option signal)	(Option)	14
27	LOCKN	V-by-One HS plus Lock detect signal	LOCKN	15
26	HTPDN	V-by-One HS plus Hot plug detect signal	HTPDN	16
25-1	-	-	-	17-41

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Option pins can be used for any purpose below.

✓ For another power supply in order to enhance power limit.

✓ For ground to stabilize power supply.

✓ For another control signals like I2C, SPI, GPIO or other user defined signals.

✓ If there are remainder of option pins, those pins should be assigned to ground.

The following is an example of 8 lane case. There are 13 user option pins which can be used arbitrary.

Table 43 User Option Pins on 41 Pin Assignment in FR(HSP) mode

TX side			RX side	
Pin No	symbol	Desicritption	symbol	Pin No
41	Vcc	Supply voltage for module	Vcc	1
40	Vcc	Supply voltage for module	Vcc	2
39	Vcc	Supply voltage for module	Vcc	3
38	Vcc	Supply voltage for module	Vcc	4
37	(Option)	(user option signal)	(Option)	5
36	(Option)	(user option signal)	(Option)	6
35	(Option)	(user option signal)	(Option)	7
34	(Option)	(user option signal)	(Option)	8
33	(Option)	(user option signal)	(Option)	9
32	(Option)	(user option signal)	(Option)	10
31	(Option)	(user option signal)	(Option)	11
30	(Option)	(user option signal)	(Option)	12
29	(Option)	(user option signal)	(Option)	13
28	(Option)	(user option signal)	(Option)	14
27	LOCKN	V-by-One HS plus Lock detect signal	LOCKN	15
26	HTPDN	V-by-One HS plus Hot plug detect signal	HTPDN	16
25	GND	Ground	GND	17
24	Tx0n	V-by-One HS plus Lane0	Rx0n	18
23	Tx0p	V-by-One HS plus Lane0	Rx0p	19
22	GND	Ground	GND	20
21	Tx1n	V-by-One HS plus Lane1	Rx1n	21
20	Tx1p	V-by-One HS plus Lane1	Rx1p	22
19	GND	Ground	GND	23
18	Tx2n	V-by-One HS plus Lane2	Rx2n	24
17	Tx2p	V-by-One HS plus Lane2	Rx2p	25
16	GND	Ground	GND	26
15	Tx3n	V-by-One HS plus Lane3	Rx3n	27
14	Tx3p	V-by-One HS plus Lane3	Rx3p	28
13	GND	Ground	GND	29
12	Tx4n	V-by-One HS plus Lane4	Rx4n	30
11	Tx4p	V-by-One HS plus Lane4	Rx4p	31
10	GND	Ground	GND	32
9	Tx5n	V-by-One HS plus Lane5	Rx5n	33
8	Tx5p	V-by-One HS plus Lane5	Rx5p	34
7	GND	Ground	GND	35
6	Tx6n	V-by-One HS plus Lane6	Rx6n	36
5	Tx6p	V-by-One HS plus Lane6	Rx6p	37
4	GND	Ground	GND	38
3	Tx7n	V-by-One HS plus Lane7	Rx7n	39
2	Tx7p	V-by-One HS plus Lane7	Rx7p	40
1	GND	Ground	GND	41

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The following pin assignment is an example of connecting I2C signals. In some use cases, the I2C is used for serial interface between Tx PCB and Rx PCB. So d SDA signal assignment

Table 44 Tx PCB Arrangement Example to Rx PCB #41 Pin Assignment in FR(HSP) mode

TX side		Desicritption	RX side	
Pin No	symbol		symbol	Pin No
41	Vcc	Supply voltage for module	Vcc	1
40	Vcc	Supply voltage for module	Vcc	2
39	Vcc	Supply voltage for module	Vcc	3
38	Vcc	Supply voltage for module	Vcc	4
37	(Option)	(user option signal)	(Option)	5
36	(Option)	(user option signal)	(Option)	6
35	(Option)	(user option signal)	(Option)	7
34	(Option)	(user option signal)	(Option)	8
33	(Option)	(user option signal)	(Option)	9
32	(Option)	(user option signal)	(Option)	10
31	(Option)	(user option signal)	(Option)	11
30	(Option)	(user option signal)	(Option)	12
29	SCL	Serial Clock Line	SCL	13
28	SDA	Serial Data Line	SDA	14
27	LOCKN	V-by-One HS plus Lock detect signal	LOCKN	15
26	HTPDN	V-by-One HS plus Hot plug detect signal	HTPDN	16
25-1	-	-	-	17-41

One type of Tx PCB might be connected to more than one type of Rx PCB in user's system.

✓ Irreplaceable V-by-One® HS plus lines are simply connected to Rx PCB from Tx PCB.

✓ Tx HTPDN line might be connected to Rx PCB via a cable or Tx PCB ground (refer to Figure 57).

✓ Irreplaceable power supply lines might be simply connected to Rx PCB from Tx PCB.

✓ Option pins might be connected to Rx PCB via passive component on Tx PCB (e.g. 0Ω resistor).

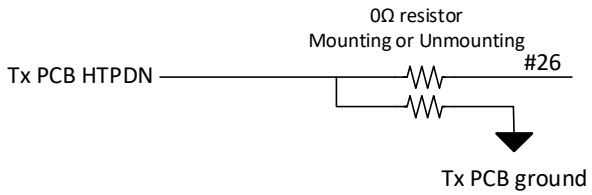

Figure 57 Tx HTPDN Circuit on Tx PCB

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6. Glossary

Table 45 Glossary of Terms

Term	Description
Data Lane	One differential signal pair
framing symbol	FSACTIVE, FSBS, FSBP, FSBE, and FSBE_SR are the framing symbols. One framing symbol is transmitted at the one pixel clock. The data amount of framing symbols sending is depended on the byte mode setting.
Character	8 bit data before 8b/10b encoder and after 8b/10b decoder. 10 bit data after 8b/10b encoder and before 8b/10b decoder. In addition to the pixel data, special character is assigned. Refer to Table 12.

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7. Acronyms

Table 46 Acronyms

Term	Description
3D	three Dimensional
3DEN	3D mode ENable
3DLR	3D Left/Right Indicator
ALN	ALigNment
CDR	Clock Data Recovery
CMY	Cyan Magenta Yellow (color representation)
CTLE	Continuous Time Linear Equalizer
DFE	Decision Feedback Equalizer
DTV	Digital TeleVision
EMI	ElectroMagnetic Interference
FFC	Flexible Flat Cable
GPIO	General-Purpose Input/Output
HDR	High Dynamic Range
HF	High Frequency
I2C	Inter-Integrated Circuit
LF	Low Frequency
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
RGB	Red Green Blue (color representation)
RGBW	Red Green Blue White(color representation)
RGBY	Red Green Blue Yellow (color representation)
SPI	Serial Peripheral Interface
TDR	Time Domain Reflectometry
XOR	eXclusive OR
YUV	Y for luminance U and V for chrominance (color representation)

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8. Revision History

Date	Version	Change of Content
June 1, 2023	1.00	1st Version
July 14, 2023	1.01	Revised Figure24 and 25 Defined the input signal to measure the eye diagram in Chapter 3.3.2. Fixed typo in Chapter 3.7
-	-	-

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