
<i>Application Note</i>	<i>THAN0060-Rev.1.50_E</i>
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THCV215/THCV216 Application Note

System Diagram and PCB Design Guideline

Contents

Contents..... 2

Application Diagrams..... 3

Dual/10bit(30bit per pixel) with Maximum Pre-emphasis..... 3

Dual/8bit(24bit per pixel) without Pre-emphasis..... 4

Single/8bit(24bit per pixel) without Pre-emphasis..... 5

Recommendations for Power Supply 6

Recommended Power Supply for THCV215..... 6

Recommended Power Supply for THCV216..... 7

Note 8

PCB Layout Considerations 10

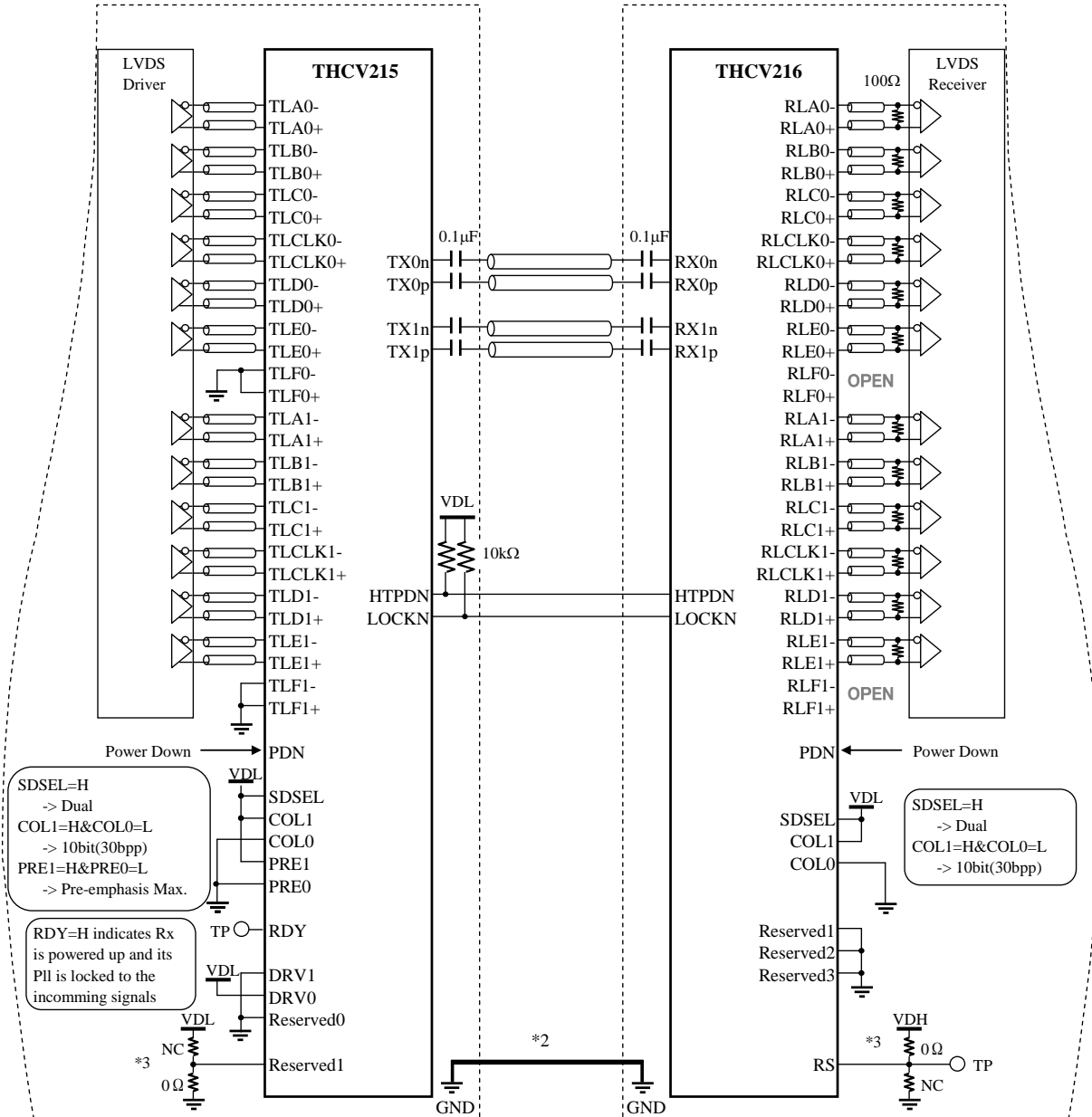
Application Diagrams

Dual/10bit(30bit per pixel) with Maximum Pre-emphasis

Setting SDSEL **HIGH** places THCV215/THCV216 in the Dual Link mode.

Setting COL1 **HIGH** and COL0 **LOW** results in the 10bit mode (30bit per pixel.)

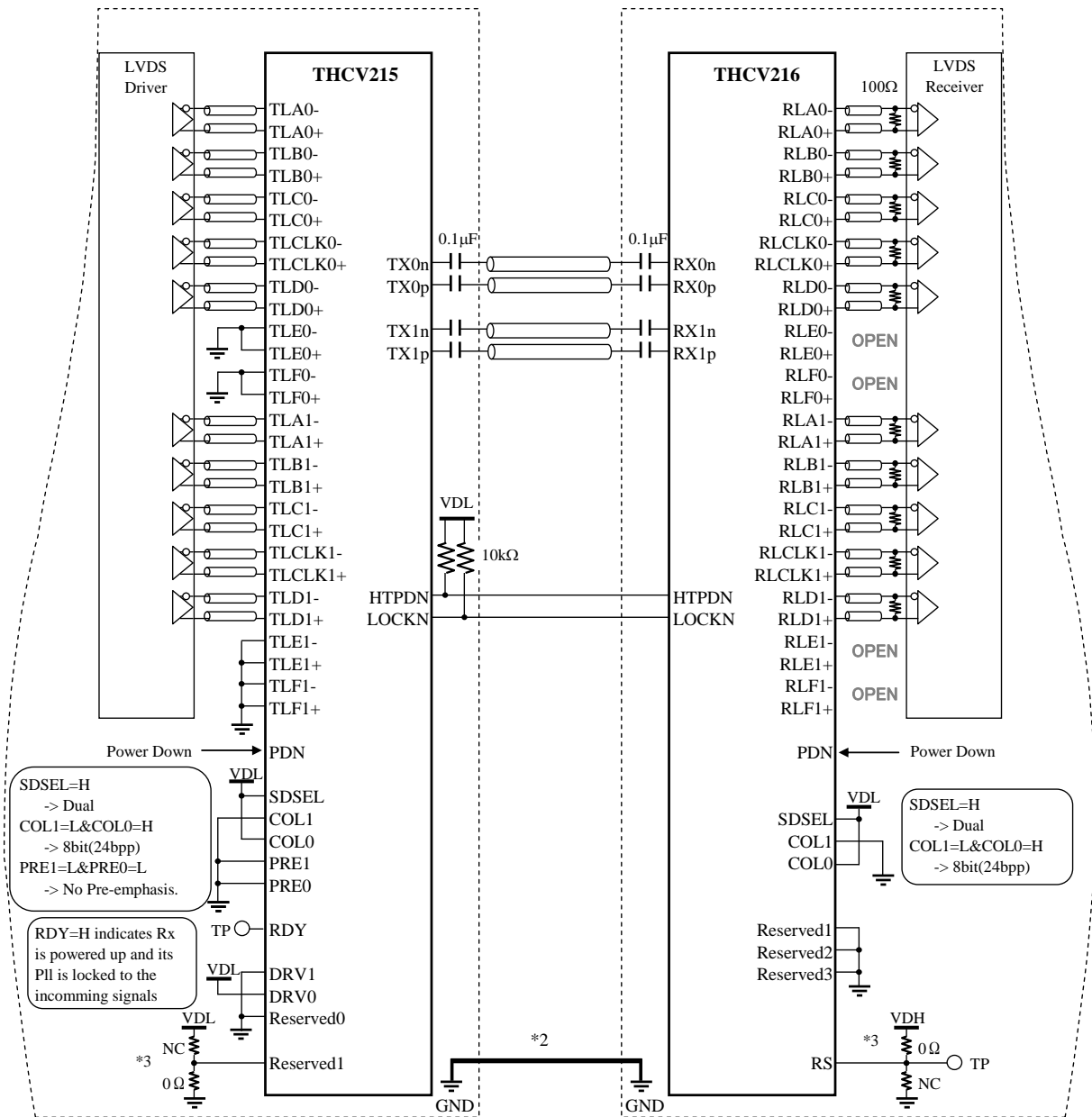
Setting PRE1 **HIGH** and PRE0 **LOW** maximizes the strength of pre-emphasis.



- *1 indicates microstrip lines or cables with their differential characteristic impedance being 100 Ω
- *2 Connect GNDs of both Tx and Rx PCB
- *3 Field BET Operation. Please see the datasheet for details. (THCV215-216_Rev.x.xx_E.pdf)

Dual/8bit(24bit per pixel) without Pre-emphasis

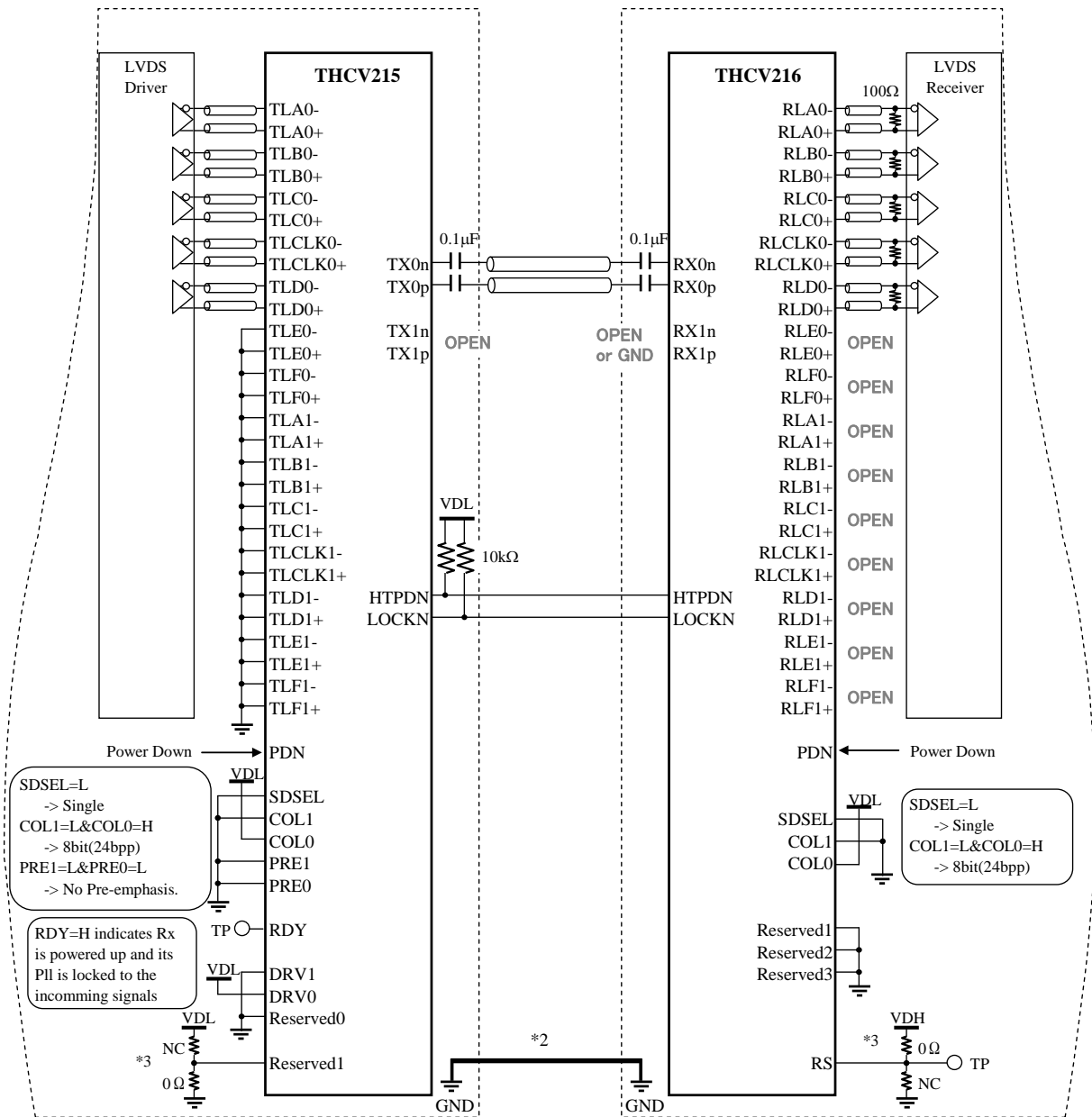
Setting **SDSEL HIGH** places THCV215/THCV216 in the Dual Link mode.
 Setting **COL1 LOW** and **COL0 HIGH** results in the 8bit mode (24bit per pixel).
 Setting **PRE1 LOW** and **PRE0 LOW** disables pre-emphasis.



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
 *2 Connect GNDs of both Tx and Rx PCB
 *3 Field BET Operation. Please see the datasheet for details. (THCV215-216_Rev.x.xx_E.pdf)

Single/8bit(24bit per pixel) without Pre-emphasis

Setting **SDSEL LOW** places THCV215/THCV216 in the Single Link mode.
 Setting **COL1 LOW** and **COL0 HIGH** results in the 8bit mode (24bit per pixel).
 Setting **PRE1 LOW** and **PRE0 LOW** disables pre-emphasis.

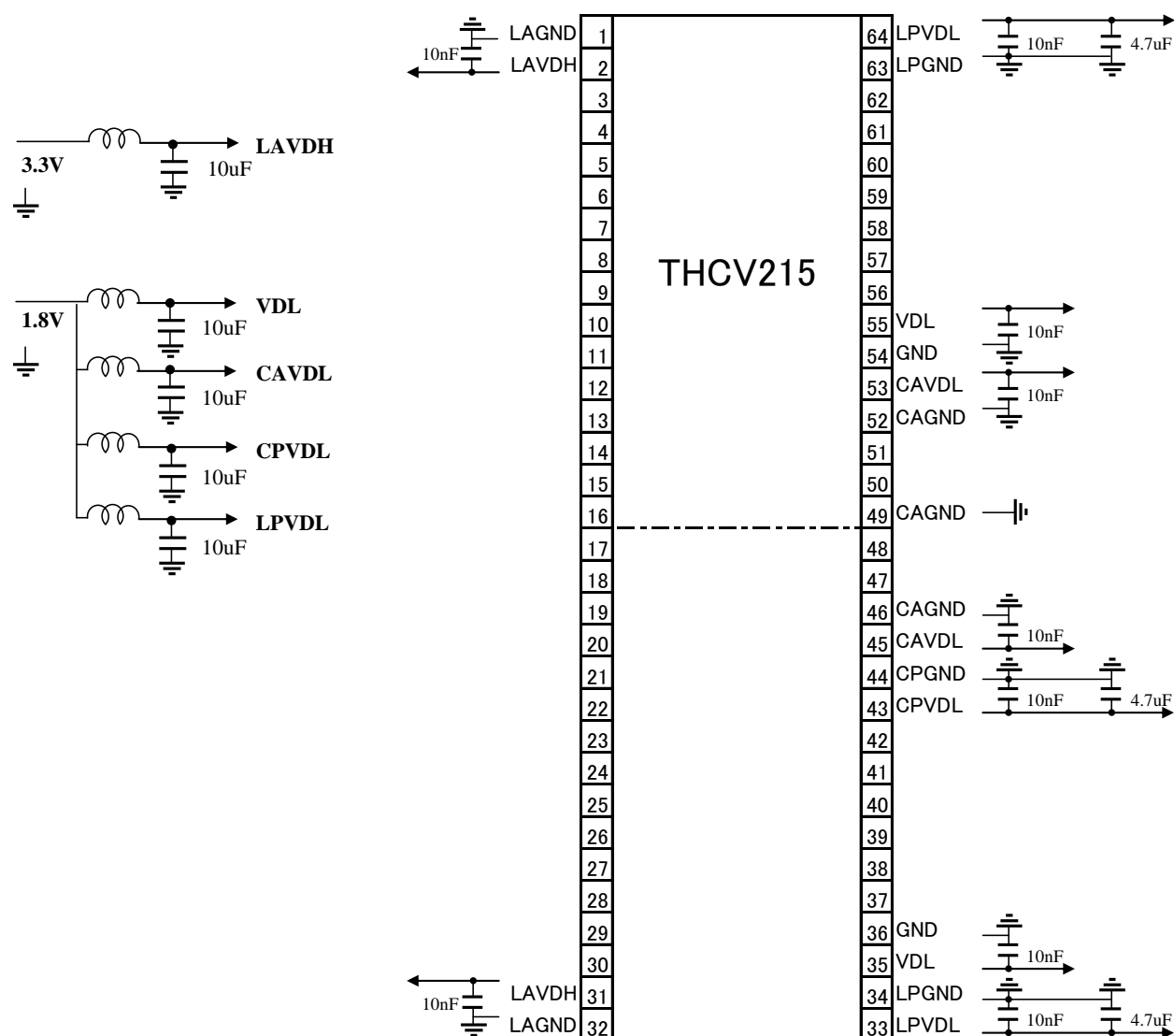


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
 *2 Connect GNDs of both Tx and Rx PCB
 *3 Field BET Operation. Please see the datasheet for details. (THCV215-216_Rev.x.xx_E.pdf)

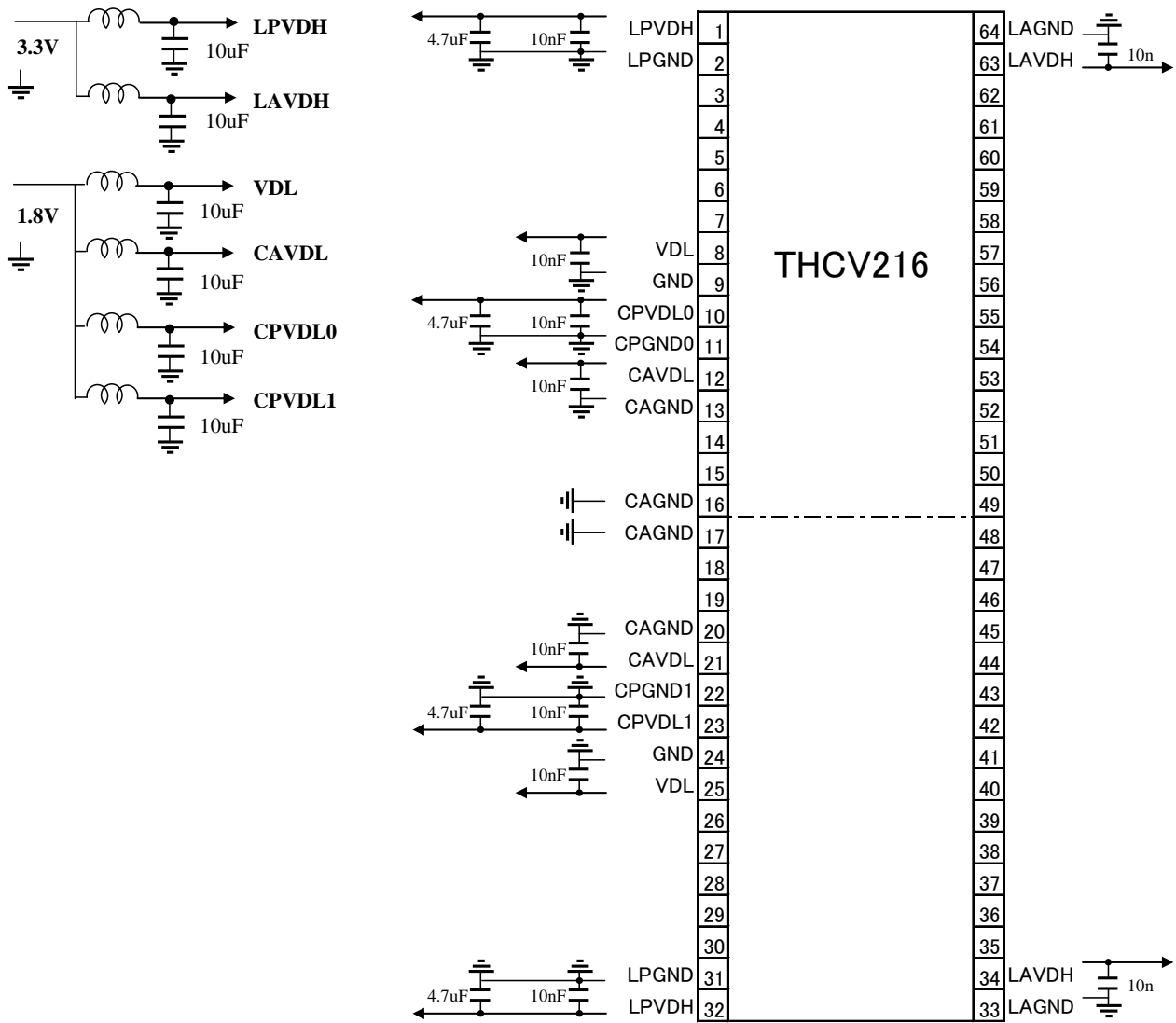
Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 10nF or 0.1μF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible.
- Adding 4.7μF capacitors to PLL's power pins, along with the smaller bypass capacitors, is recommended.

Recommended Power Supply for THCV215



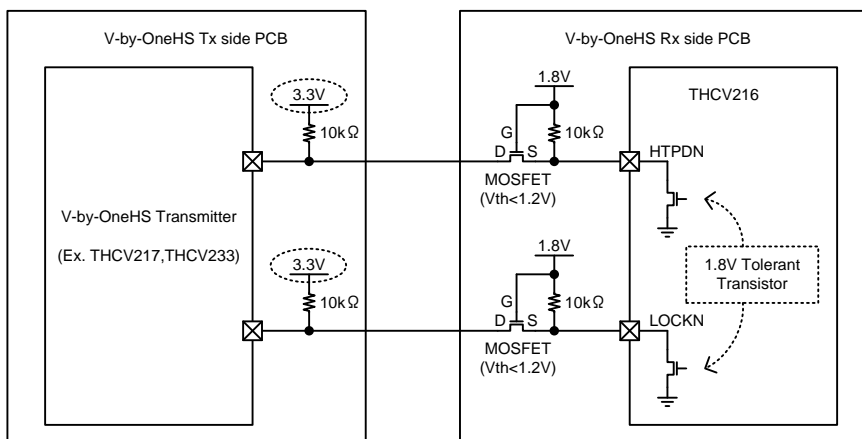
Recommended Power Supply for THCV216



Note

1) HTPDN/LOCKN connection between high VDD V-by-One® HS transmitter and THCV216

When using THCV216 with high VDD V-by-One® HS transmitter, user have to take care of HTPDN/LOCKN connection because THCV216 HTPDN/LOCKN output pins absolute maximum ratings are $V_{DL}+0.3V$; therefore high VDD pull-up at transmitter side can cause violation of usage. Users are supposed to connect those HTPDN/LOCKN line between two devices with appropriate level-shifter configuration.

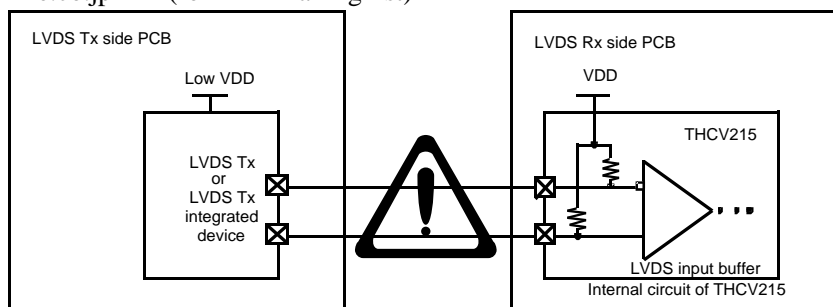


2) LVDS input pin connection

When LVDS line is not driven from the previous device, the line is pulled up to 3.3V internally in THCV215. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THCV215. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

If this situation is not avoidable and PD=L is hard to apply, there still is several remedy; therefore please contact to

mspsupport@thine.co.jp (for FAE mailing list)



3) Power On Sequence

Don't input RCLK# +/- before THCV215 is on in order to keep absolute maximum ratings. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

4) Unused LVDS input pins

First, select appropriate color depth with COL0, COL1 pins. If there are inevitably remained LVDS no input pins which are originally active, tie them to GND.

Second, avoid the situation that LVDS input pins in use are open. You can use PDN=L control during no LVDS

input period to cut off pulled-up resistors.

5)Cable Connection and Disconnection

Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

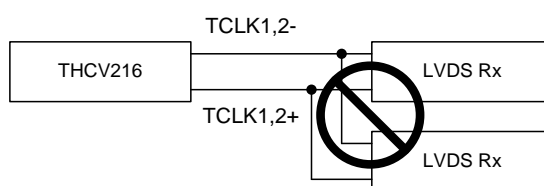
6)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THCV215 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

7)Multi Drop Connection

Multi drop connection is not recommended. If it is not avoidable, please contact to

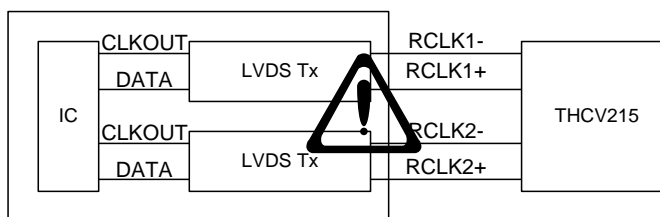
mssupport@thine.co.jp (for FAE mailing list)



8)Multiple counterpart use

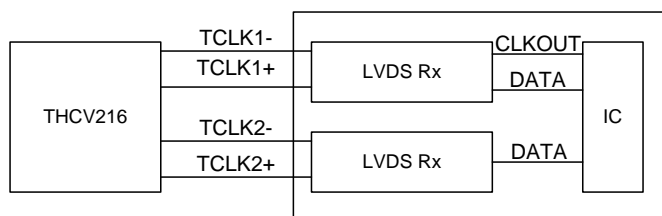
Multiple counterpart use such as following systems are not recommended. If it is not avoidable, please check if Data Sheet p.15 tTISK spec can be kept or not and more further, please contact to

mssupport@thine.co.jp (for FAE mailing list)



Multiple counterpart use such as following systems are not recommended. If it is not avoidable, please contact to

mssupport@thine.co.jp (for FAE mailing list)



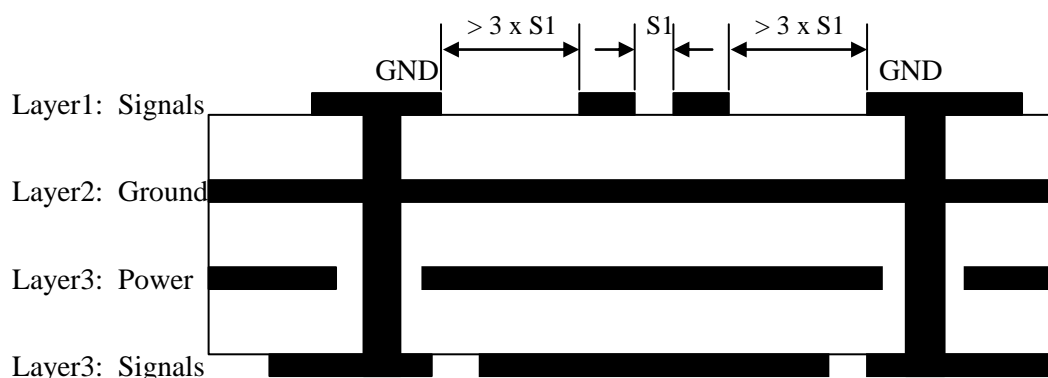
9) Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure. HTPDN should be from just one THCV216 to multiple Tx because its purpose is only ignition of all Tx. LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data. LOCKN of Tx side can be simply split to multiple Tx.

PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended microstrip lines or coupled microstrip lines whose differential characteristic impedance is 100Ω .
- Minimize the distance between traces of a differential pair ($S1$) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low._

PCB Cross-sectional View for Microstrip Lines



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1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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