Application Note	***THCV333-334_DesignGuide_Rev.1.10_E***

THCV333-Q/THCV334-Q
Application Note

Design Guideline

Contents

This Design Guide provides reference information of hardware, code and other important information for THCV333-Q (hereinafter called “SER”) and THCV334-Q (hereinafter called “DES”).

Design Flow

Design Flow Chart

THCV333-Q and THCV334-Q system typical design flow is shown below.

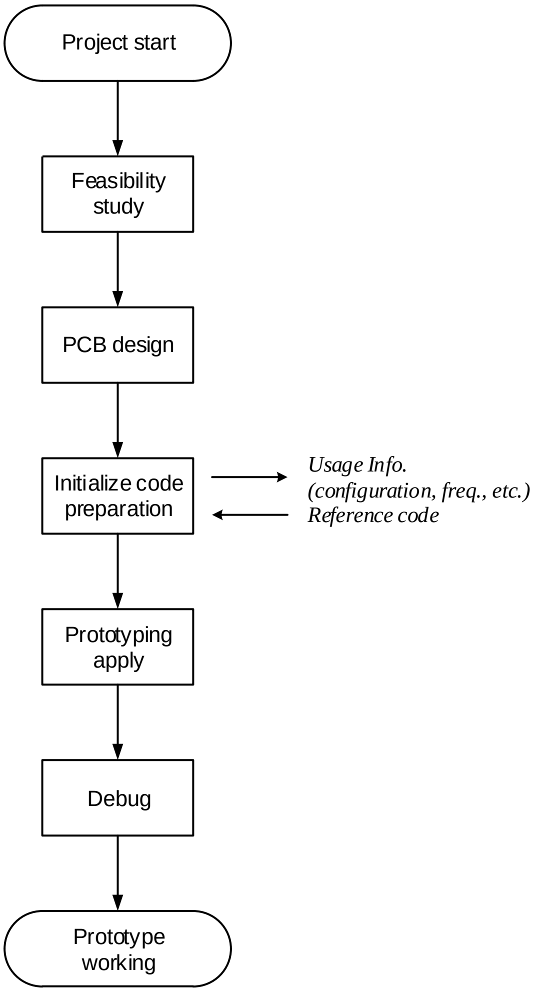


Figure 1 SER and DES typical design flow

Reference code for each usage Initialization can be support option as a meaningful start point of coding.

Initialization coding consideration materials example

Initialization code requires understanding of application system. Below is an example of consideration.

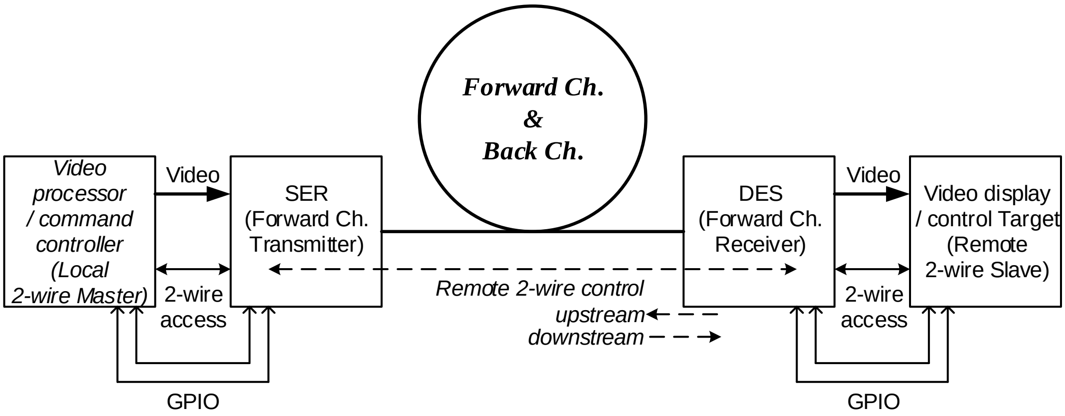
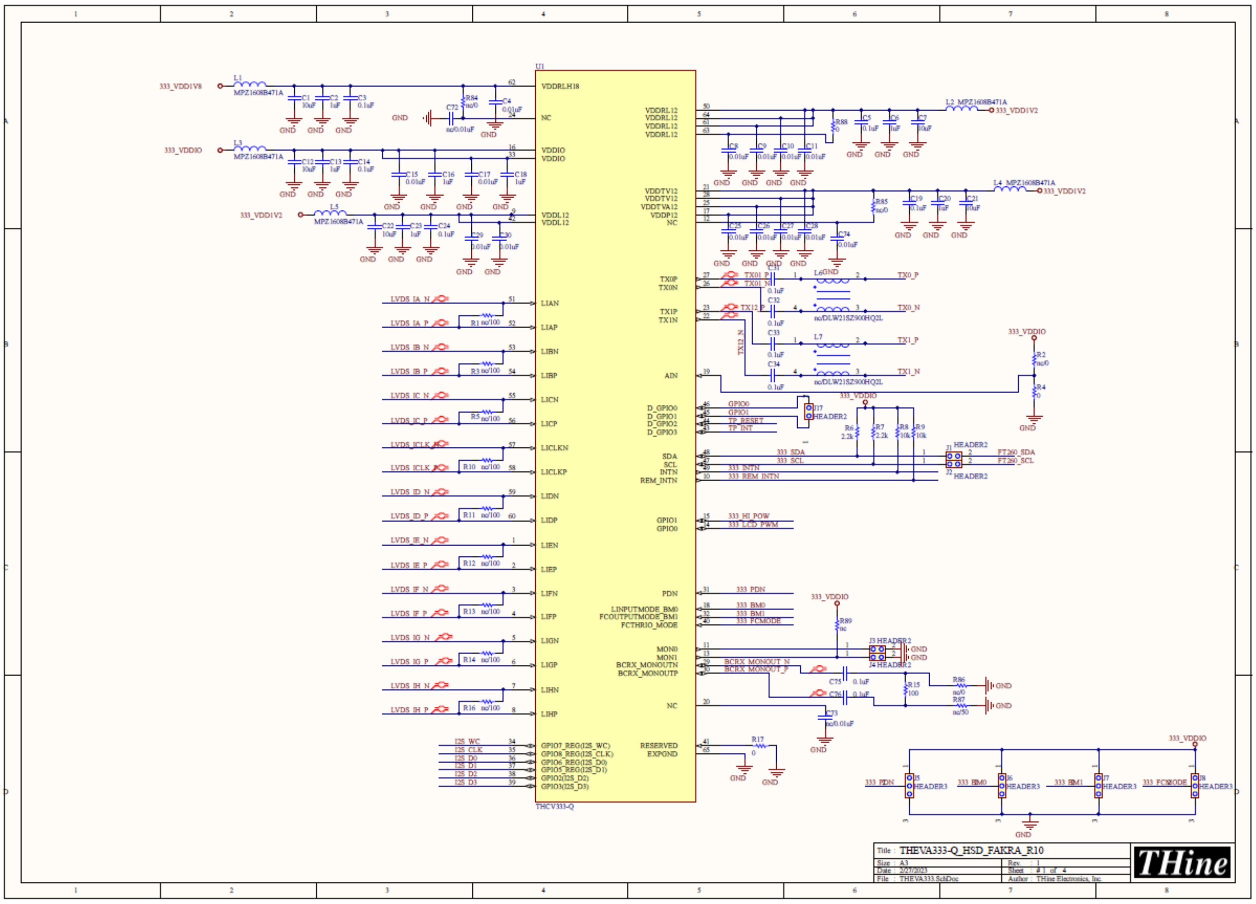


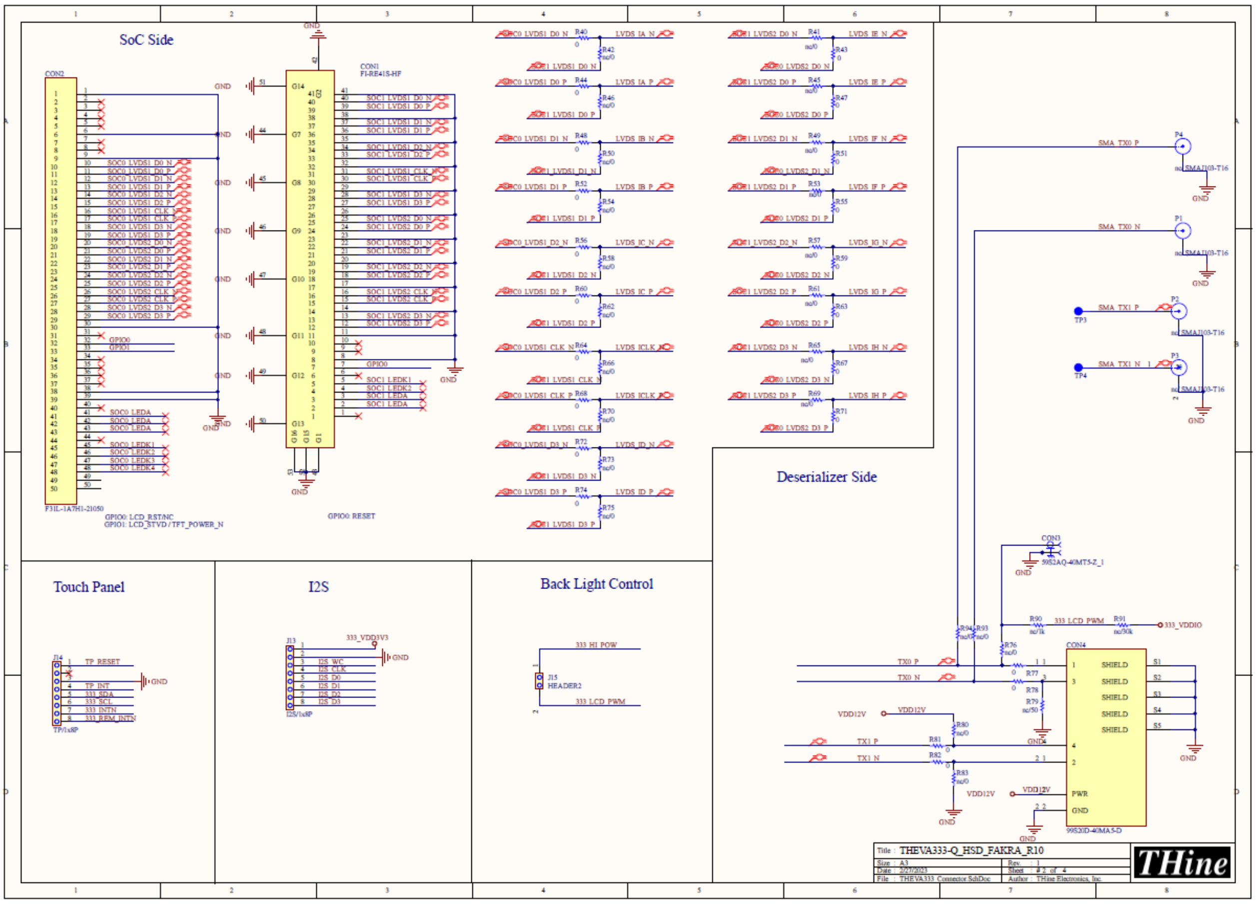
Figure 2 Example schematic diagram of Application system with regard to consider initialization code

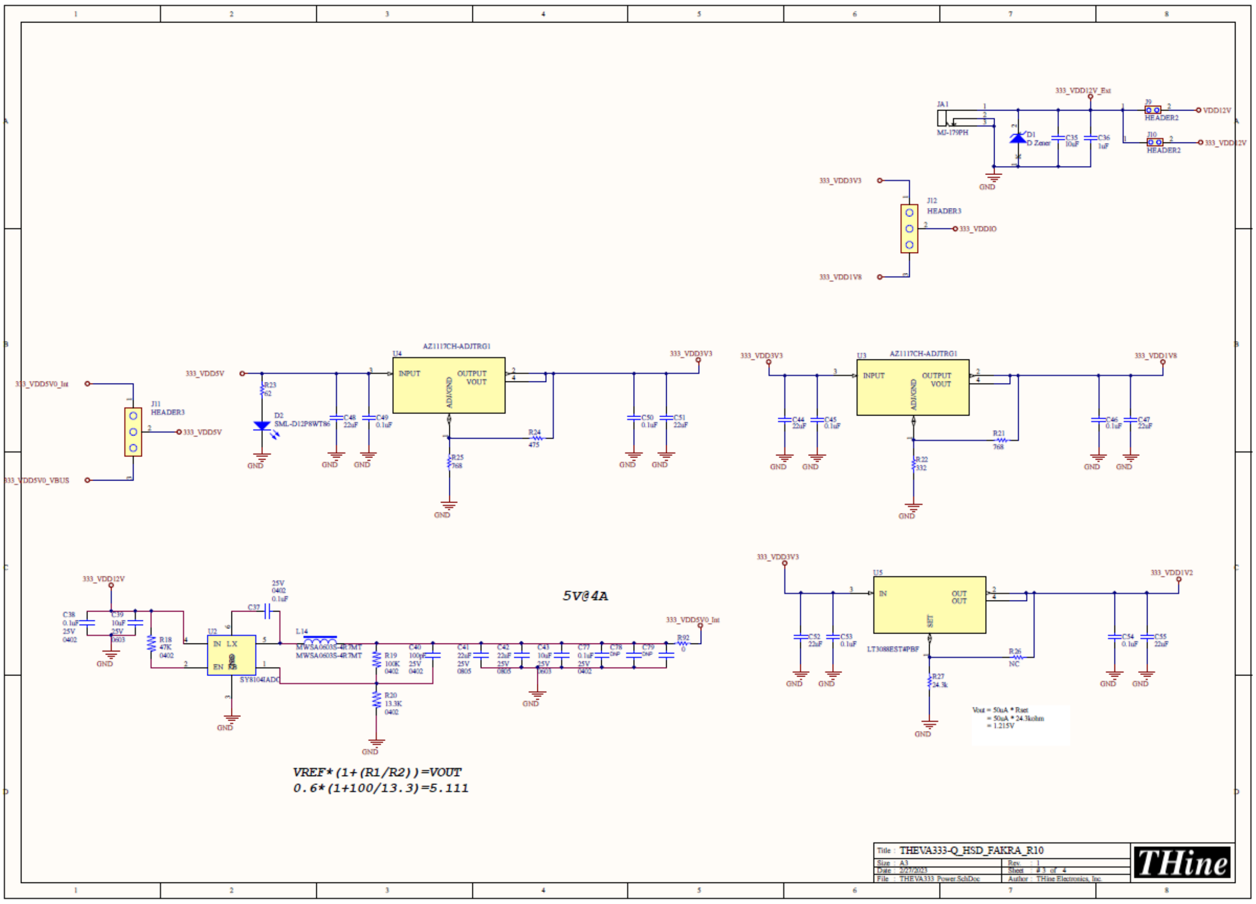
Table 1 Initialization code reference materials example

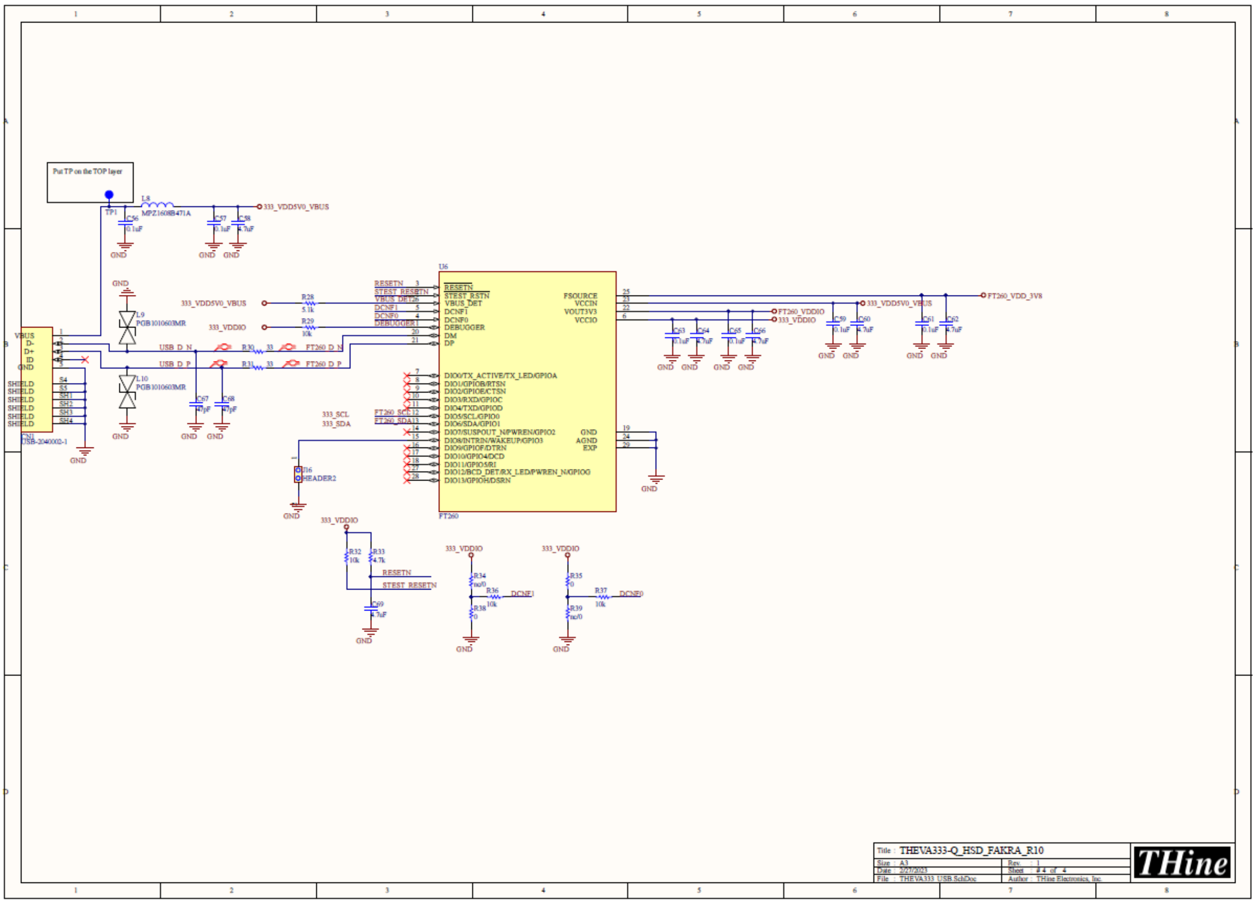
Category	Required items	example
Configuration	Tx IC name	THCV333-Q
Configuration	Tx IC number	1
Configuration	Rx IC name	THCV334-Q
Configuration	Rx IC number	1
Configuration	2-wire control source (2-wire Master) location	THCV333-Q side only. (Leading controller is only one located at THCV333-Q side)
Configuration	2-wire control target device addr.	THCV333-Q (Sub-Link Master) 7'h0B
Configuration	Bi-directional Control Channel (BCC) use or not	Yes (use BCC)
Local 2-wire Master Info.	2-wire slave clock-stretching allowed or not	Allowed (Sub-Link Pass-Through mode is recommended)
Remote 2-wire Slave Info.	Remote 2-wire Slave SCL communication Speed	400kbps
Remote 2-wire Slave Info.	Remote 2-wire Slave Device Address	7'h7A
Remote 2-wire Slave Info.	Remote 2-wire Slave Sub-Address Byte number	2Byte
SER input Info.	Open-LDI input clock (1/TRCIP) frequency	90MHz
SER input Info.	Open-LDI input port number	1port
SER input Info.	Open-LDI input color bit per pixel	24bit RGB
SER output Info.	Forward Channel (FC) output lane number	1lane
DES input Info.	Forward Channel (FC) input lane number	1lane
GPIO Info.	GPIO purpose	Touch Panel Interrupt
GPIO Info.	GPIO usage number	1
GPIO Info.	GPIO upstream number	1 (DES INTN_IN is used)
GPIO Info.	GPIO downstream number	0
GPIO Info.	GPIO time sensitive upstream number	0
GPIO Info.	GPIO time sensitive downstream number	0

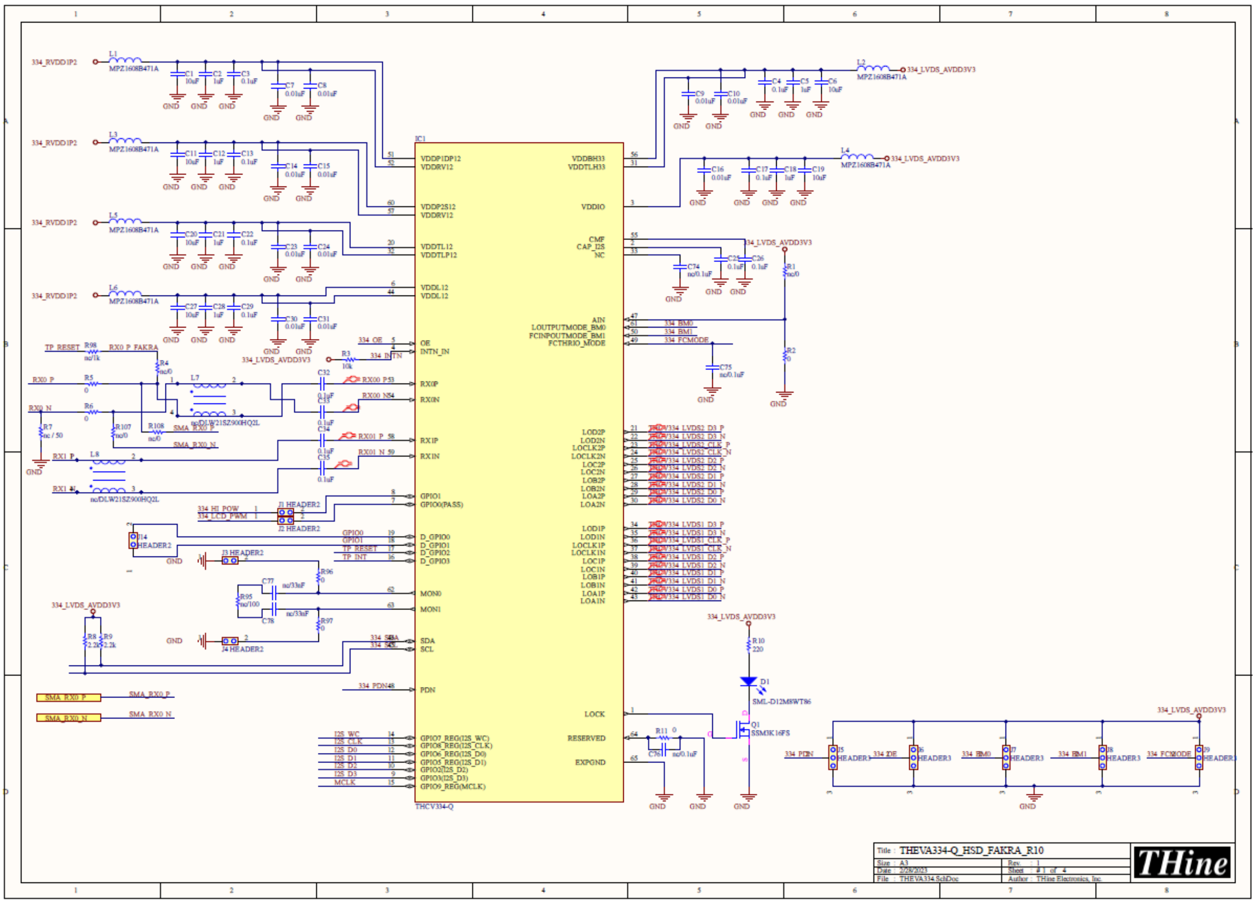
Example Circuit 1:SER-DES

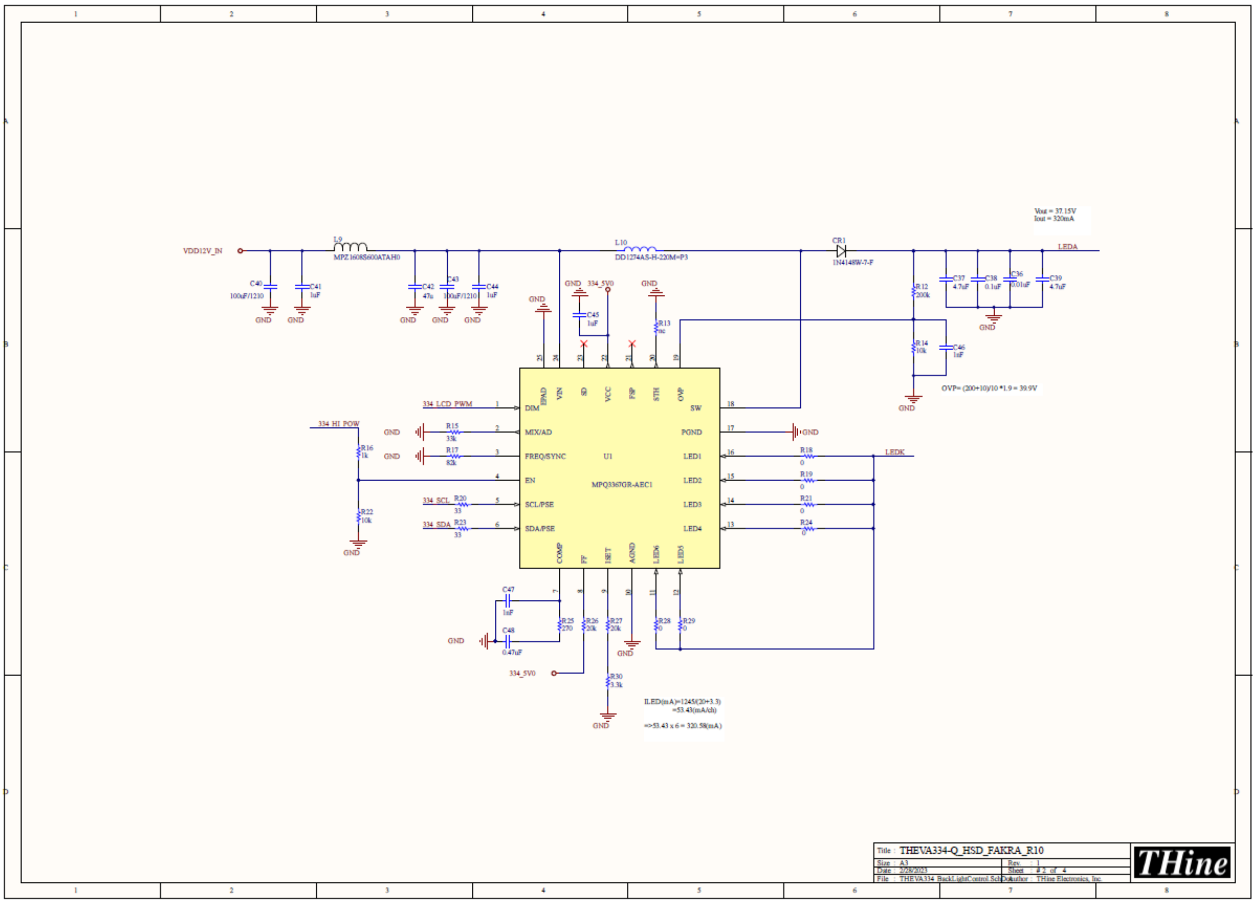


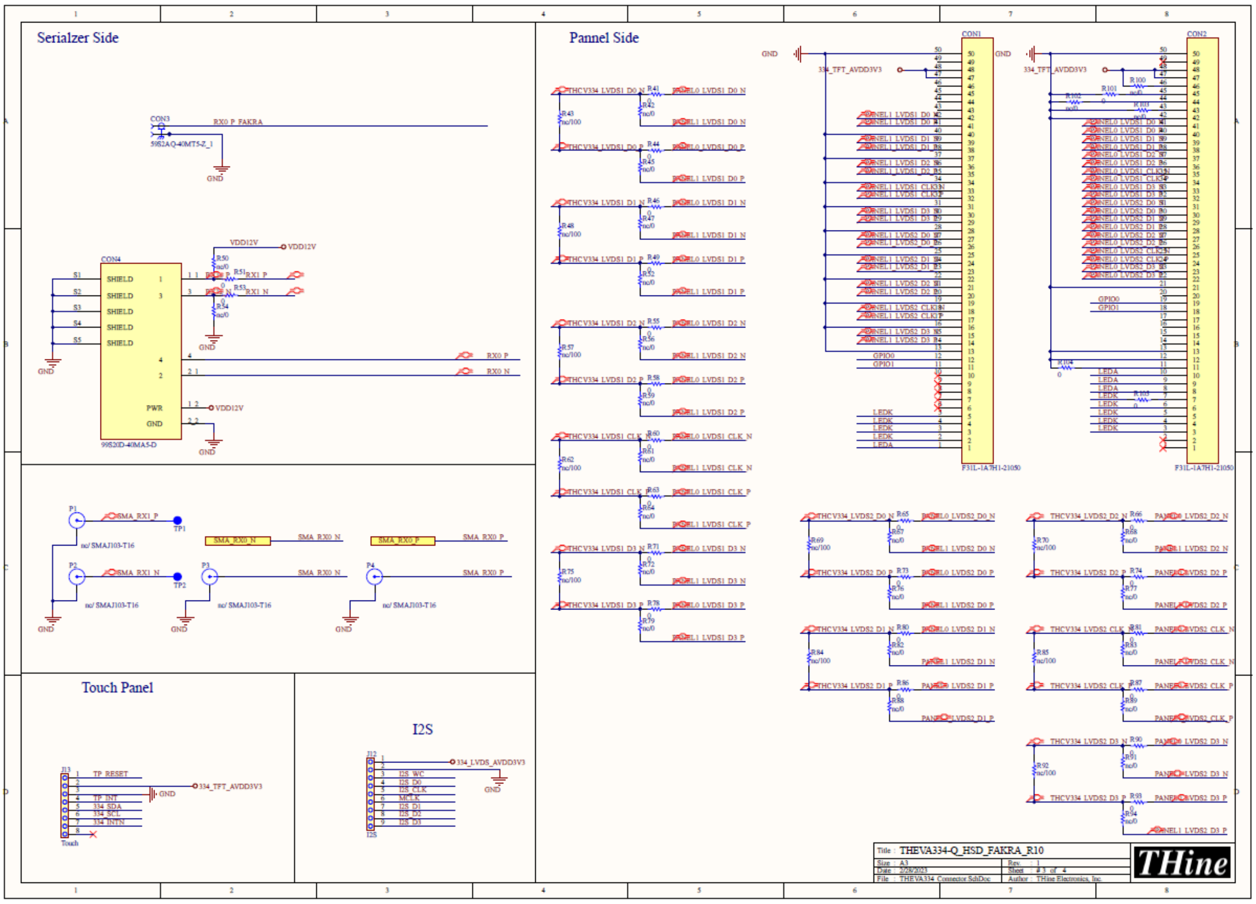


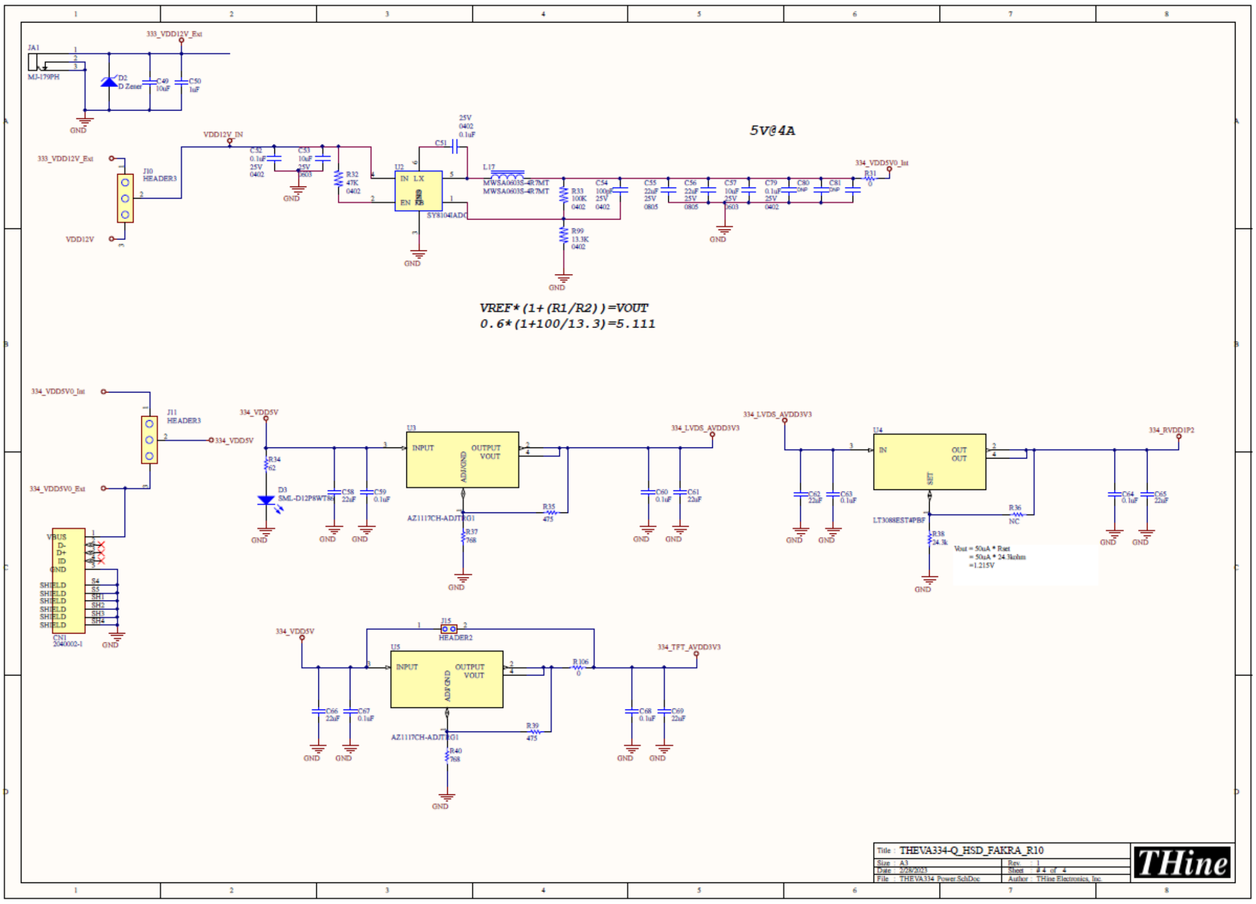

5V@4A
VREF*(1+(R1/R2))=VOUT
0.6*(1+100/13.3)=5.111
Vout = 50uA * Rset
= 50uA * 24.3kohm
= 1.215V
AZ1117CH-ADJTRG1
LT3088EST#PBF
Title : THEVA333-Q_HSD_FAKRA_R10


Put TP on the TOP layer
333_VDD5V0_VBUS
MPZ1608B471A
PGB1010603MR
USB_D_N
USB_D_P
FT260_D_N
FT260_D_P
FT260_VDD_3V8
FT260_VDDIO
333_VDDIO
333_SCL
333_SDA
HEADER2
RESETN
FT260
GND
THEVA333-Q_HSD_FAKRA_R10
THine


THCV334-Q
Title THEVA334-Q_HSD_FAKRA_R10
THine


VDD12V_IN
L9
MPZ1608S600ATAH0
C40
100uF/1210
C41
1uF
C42
47u
C43
100uF/1210
C44
1uF
L10
DD1274AS-H-220M=P3
CR1
1N4148W-7-F
Vout = 37.15V
Iout = 320mA
LEDA
C37
4.7uF
C38
0.1uF
C36
0.01uF
C39
4.7uF
R12
200k
R14
10k
C46
1nF
OVP= (200+10)/10 *1.9 = 39.9V
334_5V0
C45
1uF
R13
nc
EPAD
VIN
SD
VCC
FSP
STH
OVP
334_LCD_PWM
DIM
334_HI_POW
R16
1k
R15
33k
MIX/AD
R17
82k
FREQ/SYNC
EN
U1
MPQ3367GR-AEC1
334_SCL
R20
33
SCL/PSE
334_SDA
R23
33
SDA/PSE
R22
10k
SW
PGND
LED1
LED2
LED3
LED4
R18
0
R19
0
R21
0
R24
0
LEDK
COMP
FF
ISET
AGND
LED6
LED5
C47
1nF
C48
0.47uF
R25
270
R26
20k
R27
20k
R28
0
R29
0
R30
3.3k
334_5V0
GND
ILED(mA)=1245/(20+3.3)
=53.43(mA/ch)
=>53.43 x 6 = 320.58(mA)
Title : THEVA334-Q_HSD_FAKRA_R10
Size : A3
Date : 2/28/2023
File : THEVA334_BackLightControl.SchDoc
Rev. : 1
Sheet : # 2 of 4
Author : THine Electronics, Inc.




5V@4A
VREF*(1+(R1/R2))=VOUT
0.6*(1+100/13.3)=5.111
333_VDD12V_Ext
VDD12V_IN
VDD12V
334_VDD5V0_Int
334_VDD5V0_Ext
334_VDD5V
334_LVDS_AVDD3V3
334_RVDD1P2
334_TFT_AVDD3V3
SY8104IADC
MWSA0603S-4R7MT
AZ1117CH-ADJTRG1
LT3088EST#PBF
Vout = 50uA * Rset
= 50uA * 24.3kohm
=1.215V
Title : THEVA334-Q_HSD_FAKRA_R10
Size : A3
Date : 2/28/2023
File : THEVA334 Power.SchDoc
Rev. : 1
Sheet : 4 of 4
Author : THine Electronics, Inc.

Example Circuit Component Parts Supplemental Information

Additional informative information about example circuit is shown here.

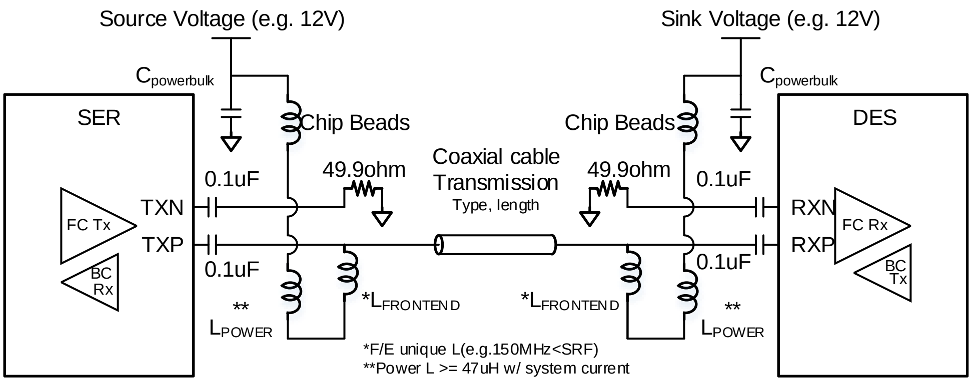


Figure 3 Example Schematic Diagram of Single-Line Configuration

$L_{FRONTEND}$ and L_{POWER} are key component for single line configuration. Some examples are introduced here. $L_{FRONTEND}$ default guideline is 2.2uH in terms of robustness against whole system noise including power effect. LFRONTEND is supposed to be equal or less than 3.3uH. Too small $L_{FRONTEND}$ is also unavailable. L_{POWER} is supposed to be equal or more than 47uH.

Table 2 Example Inductor components

Symbol	Value	Maker	Part Number	Note
$L_{FRONTEND}$	2.2uH	Murata	LQW32FT2R2	AEC-Q200
	2.0uH	Murata	LQW21FT2R0	AEC-Q200
	3.3uH	Murata	LQW32FT3R3	AEC-Q200
	2.2uH	TDK	ADL2012-2R2M	AEC-Q200
	2.2uH	Taiyo Yuden	BRC2012T2R2MD	
	3.3uH	Taiyo Yuden	BRC2012T3R3MDV	Automotive
L_{POWER}	47uH	Murata	LQH44PH470MPR	AEC-Q200
	47uH	Murata	LQW32FT470	AEC-Q200
	47uH	TDK	VLS3015CX-470M-H	AEC-Q200
	47uH	Taiyo Yuden	BRL3225T470KV	Automotive

Reference code

General programming guideline

SER and DES general setting overview are as follows.
-Video stream input / output general configuration is basically controlled by pin setting without 2-wire setting
-Audio I2S general configuration must be set by 2-wire communication control.
-GPIO bridge input / output general configuration must be set by 2-wire communication control.

Typical implementation cases are exemplified below.
-DES Output Disable to Enable (OE) control in order to start Open-LDI output stable from the beginning.
-Low frequency (e.g. single oLDI Rx below 50MHz) requires PLL HIGHFREQIN_REG arrangement.
-2-wire remote communication before video input requires .special “dummy DE” procedure and OE control.

DES remote initialization from SER (BCC Primary) by Pass Through mode code sample1:100MHz x1Port

SER 2-wire slave 7bit address is 0b0001011 (0x0B) below, being with write command, 0x16 as 8bit.
SER (BCC Primary) to DES connection is assumed. R_2WIRE_PASS_L0_DES_ID[7:1]= 0b1110111 (0x77) on BCC 2-wire Pass Through mode1 (Address rename), being with write command, 0xEE as 8bit.
R_2WIRE_PASS_ADR_BYTE_NUM=0x01(2Byte Address),
R_2WIRE_PASS_DATA_BYTE_NUM=0x00(1Byte Data)
“68”, “00”, “FE” are all hexadecimal value in below table.
Open-LDI clock:100MHz 1Port, FC 1Lane, 1920x720 60Hz RGB888 data. No Audio transmitted.
SER pins are FCTHRIO_MODE=0, LINPUTMODE_BM0=0(:1Port), and FCOUTPUTMODE_ BM1=0(:1Lane).
DES pins are FCTHRIO_MODE=0, FCINPUTMODE_BM1=0(:1Lane), LOUTPUTMODE_ BM0=0(:1Port) and OE=0(:Disable before register entry in order to avoid unstable output during initialization.)

Table 3 SER(BCC Primary)-DES Initialization code sample1 with Pass Through mode:90MHzx1Port

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	16	06	11	01	Stop	// SER Dummy DE ON
2	Start	16	01	13	03	Stop	// SER FC Drive Strength 600mV (operation default)
3	Start	16	0C	08	05	Stop	// SER GPIO D_GPIO0 Through GPO (error hold)
4	Start	16	0C	09	05	Stop	// SER GPIO D_GPIO1 Through GPO (error hold)
5	Start	EE	0C	08	03	Stop	// DES GPIO D_GPIO0 Through GPI
6	Start	EE	0C	09	03	Stop	// DES GPIO D_GPIO1 Through GPI
7	Start	16	06	11	00	Stop	// SER Dummy DE OFF
8	Start	EE	01	09	01	Stop	// DES Open-LDI LVDS Tx output enable

Software reset code from SER (BCC Primary) to DES (BCC Secondary) by Pass Through mode

Internal state software reset may provide recovery from unintended status in the middle of Normal operation. Reset action requires internal wait time for internal ready so that users must insert wait time in the middle of the code. If software reset is not work enough, hardware reset (PDNx=low) operation is another considerable option for system trouble.

Table 4 Software reset code from SER (BCC Primary) to DES with Pass Through mode

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	EE	01	09	00	Stop	// DES Open-LDI LVDS Tx output disable
2	Start	16	13	04	03	Stop	// SER Interrupt All Masked (and Status Clear)
3	Start	EE	00	0F	77	Stop	// DES Power Down registers access Enable
4	Start	EE	00	00	03	Stop	// DES PHY PLL Power Down
(5)	Start	EE	00	02	01	Stop	// DES PHY Open-LDI Tx Power Down (if required)
(6)	Start	EE	00	11	11	Stop	// DES Logic FIFO Reset-Auto-Clear (if required)
(7)	Start	EE	00	12	01	Stop	// DES Logic Open-LDI Tx Reset-Auto-Clear (if required)
(8)	Start	EE	00	02	00	Stop	// DES PHY Open-LDI Tx Power On (if required)
9	wait	12	ms				// wait time for FCBC CX Link Up Time t10 and related time
10	Start	16	00	0F	77	Stop	// SER Power Down registers access Enable
11	Start	16	00	00	02	Stop	// SER PHY PLL Power Down
(12)	Start	16	00	01	01	Stop	// SER PHY Open-LDI Rx Power Down (if required)
(13)	Start	16	00	02	01	Stop	// SER PHY FC Tx Power Down (if required)
(14)	Start	16	00	03	15	Stop	// SER PHY BC Rx Power Down (if required)
(15)	Start	16	00	10	01	Stop	// SER Logic Open-LDI Rx Reset-Auto-Clear (if required)
(16)	Start	16	00	11	11	Stop	// SER Logic FIFO Reset-Auto-Clear (if required)
(17)	Start	16	00	12	01	Stop	// SER Logic FC Tx Reset-Auto-Clear (if required)
(18)	Start	16	00	13	01	Stop	// SER Logic BC Rx Reset-Auto-Clear (if required)
(19)	Start	16	00	03	00	Stop	// SER PHY BC Rx Power On (if required)
(20)	Start	16	00	02	00	Stop	// SER PHY FC Tx Power On (if required)
(21)	Start	16	00	01	00	Stop	// SER PHY Open-LDI Rx Power On (if required)
22	Start	16	00	00	00	Stop	// SER PHY PLL Power On
23	wait	12	ms				// wait time for FCBC CX Link Up Time t10 and related time
24	Start	EE	00	00	00	Stop	// DES PHY PLL Power On
25	Start	EE	01	09	01	Stop	// DES Open-LDI LVDS Tx output Enable

Some software reset control may freeze BCC. Users must keep the shown procedure.
Software and Register reset, 0x0020 0x01, may requires BCC recovery dummy access on the very 1st BCC access just after the rest. The very 1st BCC remote 2-wire access may result into NACK.
Software, Register and Major PHY reset, 0x0030 0xAA, may requires BCC recovery dummy access on the very 1st BCC access just after the rest. The very 1st BCC remote 2-wire access may result into NACK.

Main-Link Equalizer setting reference

For most cases, Adaptive Equalizer mode (DES_RXAEQEN=0x1) works stable.

Register LEQOC_n(n=0,1) shows automatically selected Adaptive Equalizer strength under current operation.

Main-Link signal integrity condition, receiver Eye-Diagram, is supposed to be examined by oscilloscope.

DES_RXLEQCTLR, Main-Link Equalizer baseline Raise, can arrange signal integrity as secondary parameter. Basically Extremely short or long distance cases may require fine tuning of DES_RXLEQCTLR.

DES_RXLEQCTLC offers capability of manual control on Equalizer strength under static Equalizer mode.

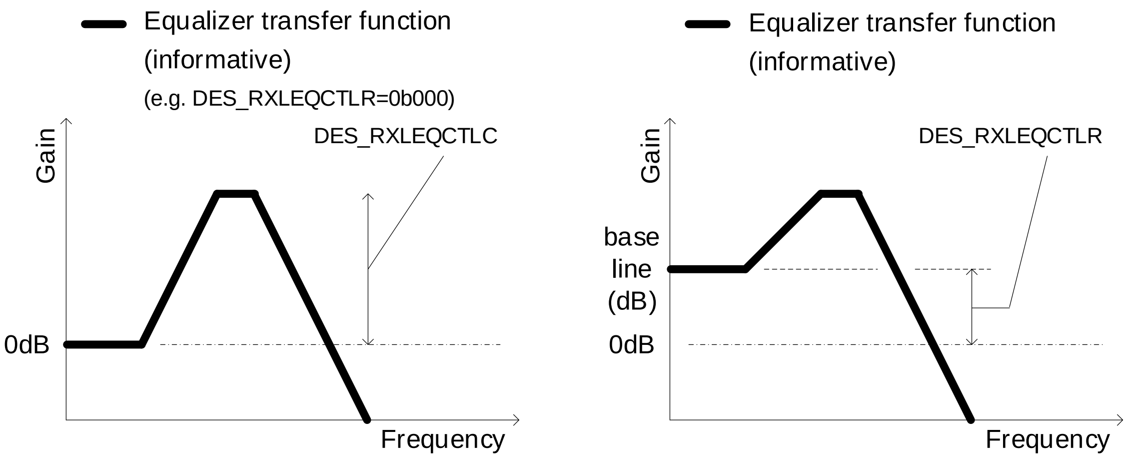


Figure 4 Schematic diagram of Equalizer control behavior

BCC control reference

BCC Primary 2-wire Set and Trigger mode

Below description is applied to BCC Primary 2-wire Set & Trigger mode.

Access to BCC Secondary Register with 2-wire Set & Trigger mode

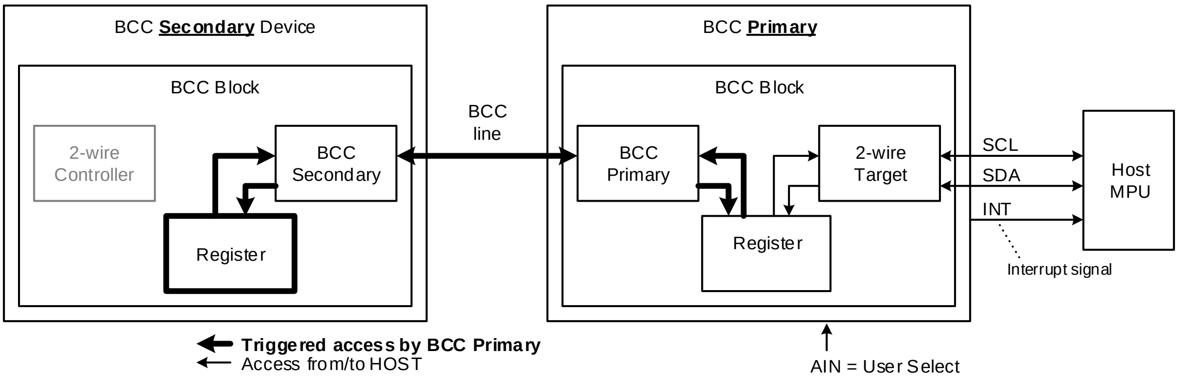


Figure 5 Access to remote BCC secondary register via 2-wire Set & Trigger mode configuration

Table 5 Remote BCC Secondary reg. write by BCC Primary 2-wire Set & Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 and clear access status register (INTN_DONE_TRANS, etc).	W	0x1321/1421[4:3]
2	Set start address of BCC Secondary register to write with needed addr. Byte (*1).	W	From 0x0B30
3	Set data for BCC Secondary to write, following after step2 address (*1).	W	(0x0B3x)-0x0B37
4	Set Device ID of BCC Primary device. (Value corresponding to AIN setting. e.g.[AIN]=[0] → 7'h0B)	W	0x0B38 bit[7:1]
5	Write 0 to indicate remote "write" access	W	0x0B38 bit0
6	Set Sub-Address Byte number of BCC Secondary (*1). (Byte num.= register value+1)	W	0x0B0A
7	Set data Byte number to write to BCC Secondary (*1). (Byte num.= register value+1)	W	0x0B0B
8	Select 2-wire remote access target path Enable on Lane0 and Lane1 Write 0x1(Lane0) or 0x3(Lane1) to R_2WIRE_SETTING_START. (Start remote write access to BCC Secondary side)	W	0x0B30 (*2)
9	When write access is completed, INTN_DONE_TRANS register value become 1 and interrupt occurs (INT=H → L).	-	-
10	If write access was normally ended, NTN_DONE_TRANS read is "0x1".	R	0x1321/1421[4]

*1 R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd8 is recommended
*2 It is prohibited that HOST MPU start access to BCC Secondary or remote 2-wire serial slave before the previous access to BCC Secondary or remote side 2-wire serial slave is completed.

Table 6 Remote BCC Secondary reg. read by BCC Primary Set & Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 and clear access status register (INTN_DONE_TRANS, etc).	W	0x1321/1421[4:3]
2	Set start address of BCC Secondary register to read with needed addr. Byte.	W	From 0x0B30
3	Set Device ID of BCC Primary device. (Value corresponding to AIN setting. e.g.[AIN]=[0] → 7'h0B)	W	0x0B38 bit[7:1]
4	Write 1 to indicate remote "read" access	W	0x0B38 bit0
5	Set Sub-Address Byte number of BCC Secondary. (Byte num.= register value+1)	W	0x0B0A
6	Set data Byte number to read from BCC Secondary(*1) (Byte num.= register value+1)	W	0x0B0B
7	Select 2-wire remote access target path, Lane0 or Lane1 Write to R_2WIRE_SETTING_START. (Start remote write access to BCC Secondary side) 0x01:Lane0 read with Sub-Address 0x02:Lane0 read with No Sub-Address 0x03:Lane1 read with Sub-Address 0x04:Lane1 read with No Sub-Address	W	0x0B30 (*2)
8	When read access is completed, read data is stored in BCC Primary register (Address 0x0B40-0x0B47) and INTN_DONE_TRANS register value become 1 and interrupt occurs (INT=H → L).	-	-
9	If read access was normally ended, INTN_DONE_TRANS read is "0x1".	R	0x1321/1421[4]
10	HOST MPU read data stored in BCC Primary register.	R	0x0B40-0x0B47

*1 R_2WIRE_DATA_BYTE < 'd8 (max 8Byte)
*2 It is prohibited that HOST MPU start access to BCC Secondary or remote 2-wire serial slave before the previous access to BCC Secondary or remote side 2-wire serial slave is completed.

Access to 2-wire target devices connected to BCC Secondary with 2-wire Set & Trigger mode

HOST MPU can access to remote side 2-wire serial target register via SER as BCC Primary and BCC Secondary by DES as VCC Primary register settings on 2-wire Set & Trigger mode. BCC Secondary has 2-wire serial controller block.

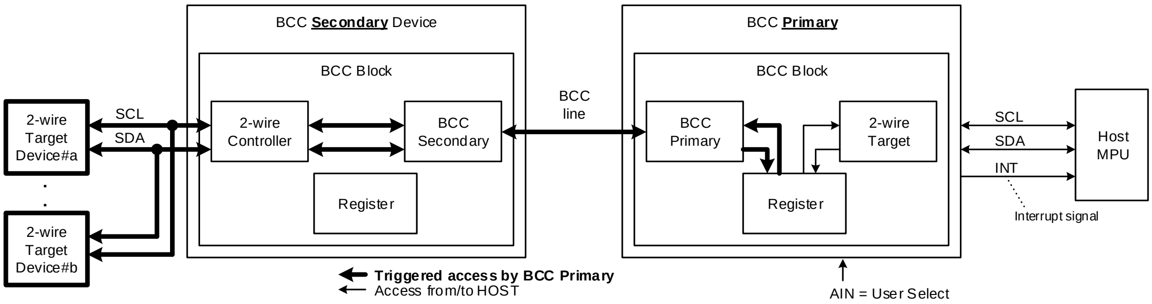


Figure 6 Host MPU to 2-wire target devices at BCC Secondary side via BCC Primary access configuration

Table 7 Remote 2-wire target reg. write by BCC Primary 2-wire Set & Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 and clear access status register (INTN_DONE_TRANS, etc).	W	0x1321/1421[4:3]
2	Set start address of target 2-wire slave register to write with needed addr. Byte (*1).	W	From 0x0B30
3	Set data for target 2-wire slave to write, following after step2 address (*1).	W	(0x0B3x)-0x0B3F
4	Set Device ID of target remote 2-wire slave device.	W	0x0B38 bit[7:1]
5	Write 0 to indicate remote “write” access	W	0x0B38 bit0
6	Set Sub-Address Byte number of 2-wire slave (*1). (Byte num.= register value+1)	W	0x0B0A
7	Set data Byte number to write to 2-wire slave (*1). (Byte num.= register value+1)	W	0x0B0B
8	Select 2-wire remote access target path Enable on Lane0 and Lane1 Write 0x1(Lane0) or 0x3(Lane1) to R_2WIRE_SETTING_START. (Start remote write access to BCC Secondary side)	W	0x0B30 (*2)
9	When write access is completed, INTN_DONE_TRANS register value become 1 and interrupt occurs (INT=H → L).	-	-
10	If write access was normally ended, INTN_DONE_TRANS read is “0x1”.	R	0x1321/1421[4]

*1 R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd8 is recommended
*2 It is prohibited that HOST MPU start access to BCC Secondary or remote 2-wire serial slave before the previous access to BCC Secondary or remote side 2-wire serial slave is completed.

Table 8 Remote 2-wire target reg. read by BCC Primary Set & Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 and clear access status register (INTN_DONE_TRANS, etc).	W	0x1321/1421[4:3]
2	Set start address of 2-wire slave register to read with needed addr. Byte.	W	From 0x0B30
3	Set Device ID of target remote 2-wire slave device.	W	0x0B38 bit[7:1]
4	Write 1 to indicate remote "read" access	W	0x0B38 bit0
5	Set Sub-Address Byte number of target 2-wire Slave. (Byte num.= register value+1)	W	0x0B0A
6	Set data Byte number to read from 2-wire Slave(*1) (Byte num.= register value+1)	W	0x0B0B
7	Select 2-wire remote access target path, Lane0 or Lane1 Write to R_2WIRE_START. (Start remote write access to BCC Secondary side) 0x01:Lane0 read with Sub-Address 0x02:Lane0 read with No Sub-Address 0x03:Lane1 read with Sub-Address 0x04:Lane1 read with No Sub-Address	W	0x0B30 (*2)
8	When read access is completed, read data is stored in BCC Master register (Address 0x0B40-0x0B47) and INTN_DONE_TRANS register value become 1 and interrupt occurs (INT=H → L).	-	-
9	If read access was normally ended, INTN_DONE_TRANS read is "0x1".	R	0x1321/1421[4]
10	HOST MPU read data stored in BCC Master register.	R	0x0B40-0x0B47

*1 R_2WIRE_DATA_BYTE < 'd8 (max 8Byte)
*2 It is prohibited that HOST MPU start access to BCC Secondary or remote 2-wire serial slave before the previous access to BCC Secondary or remote side 2-wire serial slave is completed.

BCC Primary 2-wire Pass Through mode

Below descriptions are details of local and remote side 2-wire operation.

Divided Read operation always read target register by R_2WIREPT_DATA_BYTE defined unit. If R_2WIREPT_DATA_BYTE is not 0 (single read transaction unit is not 1Byte), 2-wire remote read operation may read access the address which originally user intends to read. As a result, 2-wire slave remote device may operate abnormal because of this unintended read action.

2-wire Pass Through mode BCC Secondary command, write and read

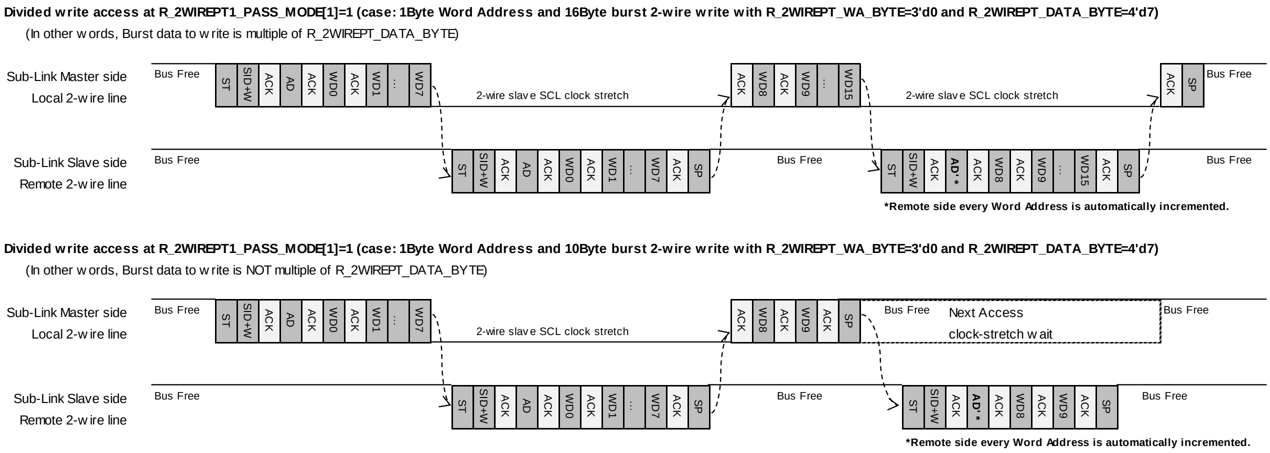
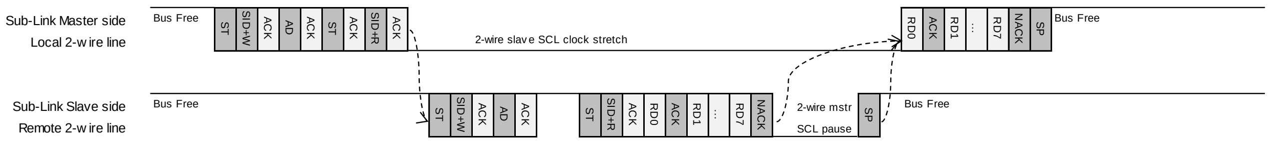


Figure 7 2-wire Pass Through mode BCC Secondary Divided Write

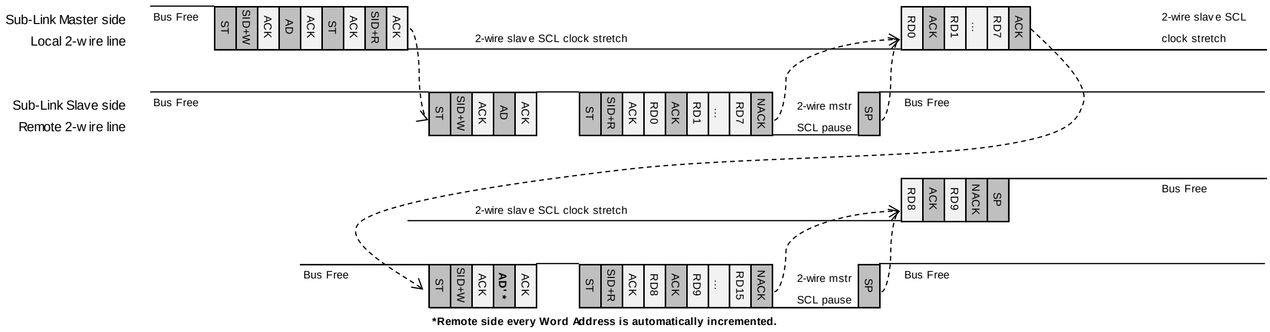
Divided read access at R_2WIREPT1_PASS_MODE[1]=1 (case: 1Byte Word Address and 8Byte burst 2-wire read with R_2WIREPT_WA_BYTE=3'd0 and R_2WIREPT_DATA_BYTE=4'd7)

(In other words, Burst data to read is multiple of R_2WIREPT_DATA_BYTE)



Divided read access at R_2WIREPT1_PASS_MODE[1]=1 (case: 1Byte Word Address and 10Byte burst 2-wire read with R_2WIREPT_WA_BYTE=3'd0 and R_2WIREPT_DATA_BYTE=4'd7)

(In other words, Burst data to read is NOT multiple of R_2WIREPT_DATA_BYTE)



[list of abbreviations]				
ST: Start Condition	ACK: Acknowledge	SID: Slave Address (Device Address)	WD: Write Data	+W: Write command indicator
SP: Stop Condition	NACK: No Acknowledge	AD: Word Address	RD: Read Data	+R: Read command indicator

Figure 8 2-wire Pass Through mode BCC Secondary Divided Read

Through GPIO signal bridge speed reference

Through GPIO sampling frequency example for particular Forward Ch. speed are calculated as below.
Maximum data-rate that can be bridged by Through GPIO are calculated as 4*sampling frequency for informative information.
Forward Channel Data-Rate can also be speeded up by register MODEREGS.VIDEO.DUPLICATE_REG function by x2. For example, when FTFC of original video was 1Gbps, this function could speed up FTFC to 2Gbps, which also results into GPIO bridge speed up and support 208.3kbps with 4 active GPIO, accommodating UART 115200bps.

Table 9 Through GPIO signal bridge frequency

(Gbps)	(ps)	4 or 8 cycles	4 or 8 active GPIOs	(Msample/sec)	(ksample/sec)	(Mbps)	(kbps)
FTFC/FRFC	TTFCBIT/TRFCBIT	FCTHRIO_MODE	GPIO_CNT_REGS.SMPNUM	fSMPL_FCbridge	fSMPL_BCbridge	maxData Rate_FCbridge	maxData Rate_BCbridge
1	1000	8	8	4.2	208.3	1.0	52.1
1	1000	8	4	8.3	416.7	2.1	104.2
1	1000	4	8	8.3	208.3	2.1	52.1
1	1000	4	4	16.7	416.7	4.2	104.2
2	500	8	8	8.3	416.7	2.1	104.2
2	500	8	4	16.7	833.3	4.2	208.3
2	500	4	8	16.7	416.7	4.2	104.2
2	500	4	4	33.3	833.3	8.3	208.3
3	333.3	8	8	12.5	625.0	3.1	156.3
3	333.3	8	4	25.0	1250.0	6.3	312.5
3	333.3	4	8	25.0	625.0	6.3	156.3
3	333.3	4	4	50.0	1250.0	12.5	312.5
4	250	8	8	16.7	833.3	4.2	208.3
4	250	8	4	33.3	1666.7	8.3	416.7
4	250	4	8	33.3	833.3	8.3	208.3
4	250	4	4	66.7	1666.7	16.7	416.7

Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 0.1uF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. All supply pins need capacitor placement one by one.
- Use the same ground plane for all ground pins including EXPGND.

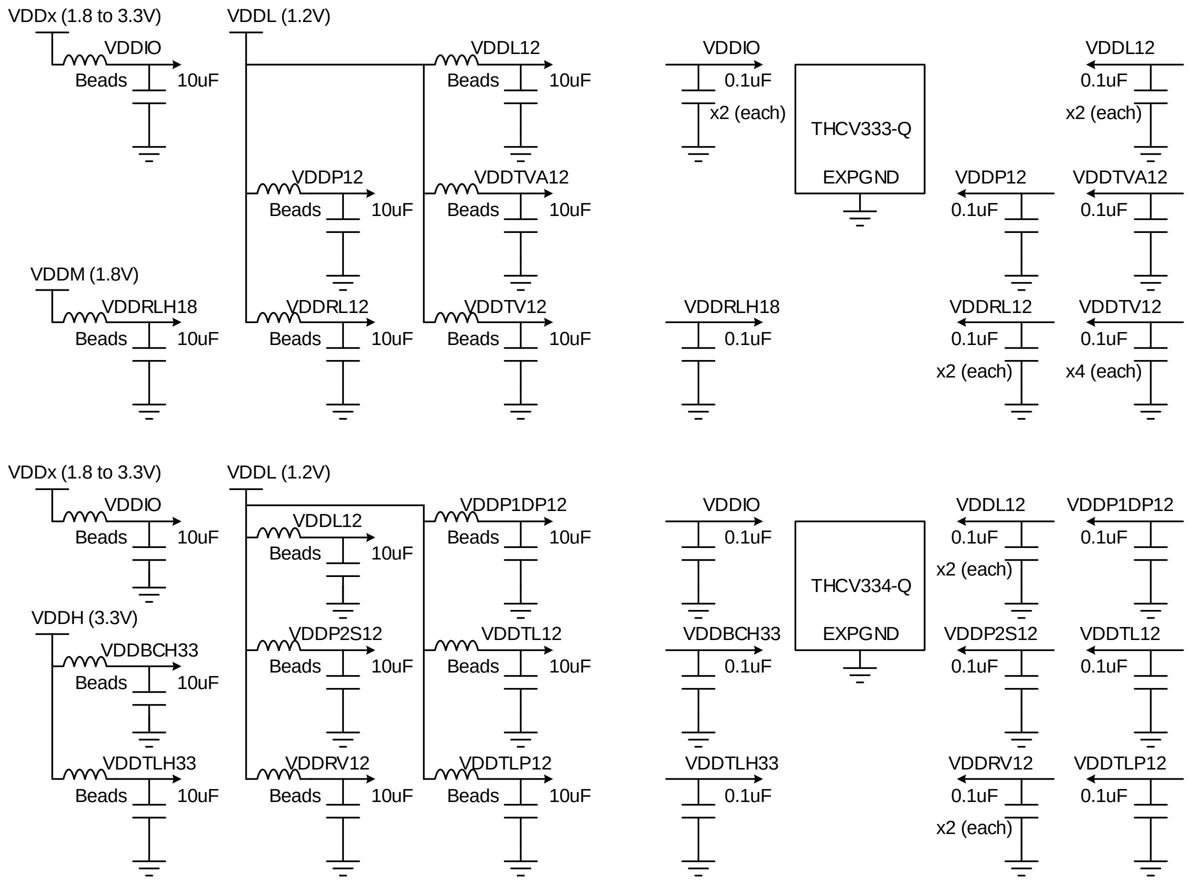


Figure 9 Power supply recommendation

Note

1) Power On Sequence

Don’t input clock nor data before SER and DES are powered on in order to keep absolute maximum ratings.

2) Cable Connection and Disconnection

Don’t connect and disconnect Open-LDI, CMOS, I2S, FC and BCC cable/connector, when power is supplied to the system.

3) GND Connection

Connect the each GND of the PCB where SER and DES are on it. It is better for EMI reduction to place GND cable as close to signal cable as possible.

4) Local and remote 2-wire serial access multi-controller requirement

Local and remote 2-wire serial access at the same time may be prohibited on BCC Secondary device. For multiple controller application, command collision avoidance scheme is supposed to be prepared.

Below figure is an example of schematic diagram of time domain or indicator driven command separation.

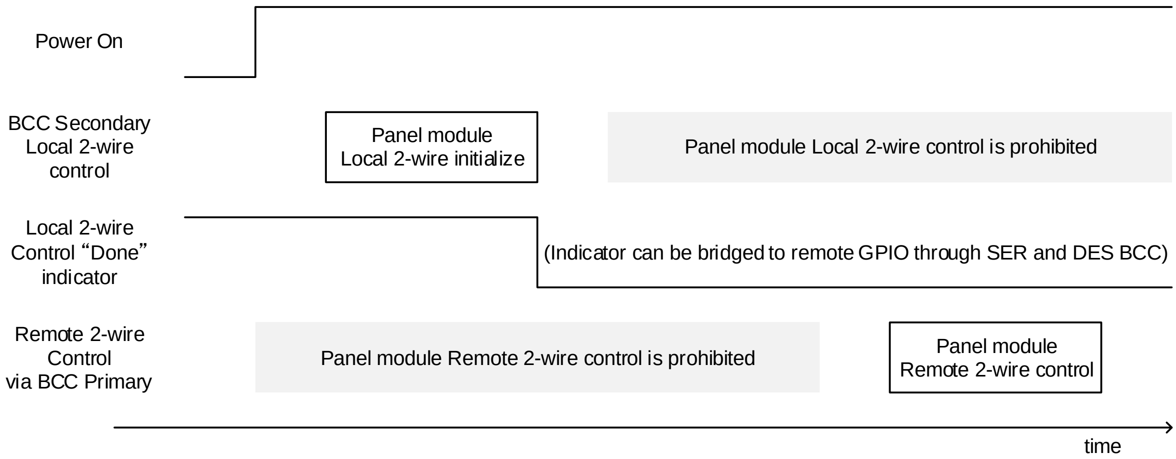


Figure 10 2-wire local and remote access timing chart

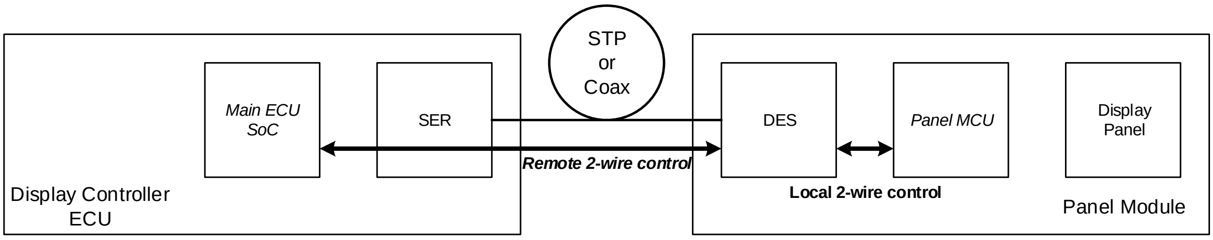


Figure 11 2-wire local and remote access configuration

5) ERR detect function transition time behavior

Forward Channel (FC) Rx ERR detect fault at LOCKN=H=>L and LOCKN=L=>H=>L transition time. ERR detection is reasonable on this time period because at the beginning of transition, FC is not yet logically stable before all the training is done, while FC Rx ERR detection already starts as normal behavior.

User must ignore FC Rx ERR detection on this time period.

6) INT function initialization

INT interrupt function is supposed to be cleared before start monitoring any desired status because INT status may change at power on condition and SER and DES internal boot up procedure.

7) BCC 2-wire Pass Through mode Read Byte setting care

Divided Read operation always read target register by R_2WIRE_PASS_DATA_BYTE_NUM defined unit. If R_2WIRE_PASS_DATA_BYTE_NUM is not 0 (single read transaction unit is not 1Byte), 2-wire remote read operation may read over the address which originally user intends to read. As a result, 2-wire target remote device may operate abnormal because of this unintended read action.

8) BCC remote 2-wire access command transmission failure handling

BCC 2-wire access in noisy environment may collapse as single transaction against fair enough access success rate. Informative several functional safety mechanism will be shown here.

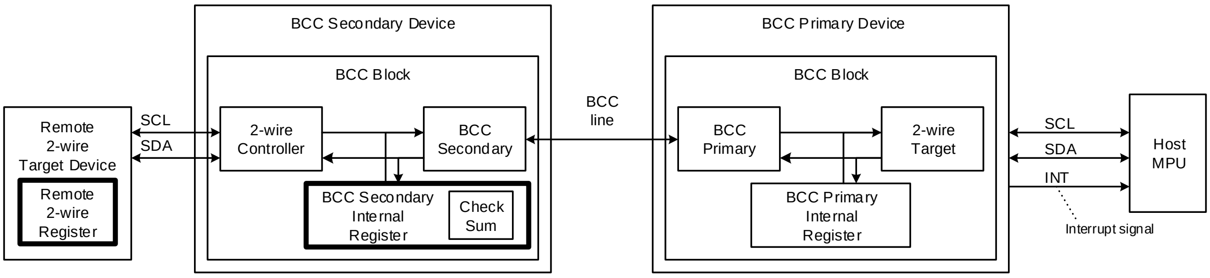


Figure 12 BCC 2-wire remote access configuration

One option is to place MCU on remote BCC Secondary side. Internal PCB communication can eliminate external module noise bothersome elements. BCC, still, provide best-effort remote command communication channel.

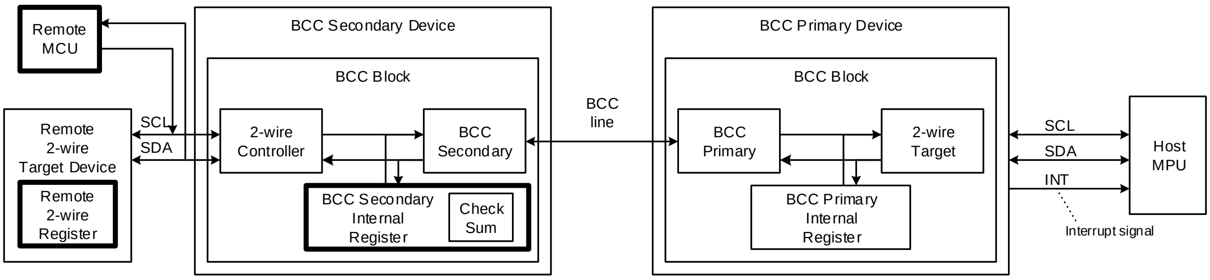


Figure 13 BCC 2-wire remote access configuration

Another option is "action, confirm, re-action, and reconfirm" redundant command access procedure. As informative content, collapsed read action is likely to return 0x00 data, while collapsed read action is not likely to return "just right" data. Repeat read results gives statistical estimate value of access target. BCC Slave device may have checksum information of all internal register so that checksum data can be used for total register status.

Write example							
	Write	=>	Read	=>	Read	=>	Re-write if expected value is not read
Read example							
	Read	=>	Read	=>	Read	=>	Filter outlier and process statistically

9) BCC basic protocol setting change in the middle of active operation

Except initialization procedure, R_2WIRE_PASS_MODE change in the middle of active operation requires BCC operation suspension. After R_2WIRE_PASS_MODE change action in the middle of BCC suspension, BCC operation can be resumed.

10) Temperature and Voltage drift environment care on FC function

Temperature and voltage drift can change the optimized setting of DES FC receiver, while offset cancel function autonomous setting establishment is held at the beginning of reset operation. For example, when temperature is severely drifted from -40degrees Celsius to 105degrees Celsius by system itself heat in hard winter, FC CRC error or LOCKN unlock happens because of this optimized-at-the-beginning-but-not-suited-at-the-end setting of FC receiver.

FC CRC or LOCKN states are supposed to be monitored by MCU and DES FC block had better be reset by register control under the temperature and voltage drift severe environment.

11) Frequency change care on FC

Basically active frequency change in the middle of normal operation is not allowed.

If and only if frequency change in the middle of operation is inevitable, FC block is required to be reset by register control after target operation frequency stabled status.

12) Interrupt Push-Pull High Active output mode for Functional Safety

Abnormal over-voltage and under-voltage monitoring is prepared for power domains. When 1.2V digital power supply under-voltage is detected, interrupt pin is reset to Hi-Z condition. Output mode of interrupt pin for functional safety is better to be set to Push-Pull High-Active and also external circuit of interrupt pin is better to be pull-up by resistor. Interrupt state is indicated by High driven, while normal operation is stayed as Low driven. The other under-voltage and over-voltage can be set to report as High driven by interrupt function activation.

13) BCC remote 2-wire access data Byte number for remote 2-wire NACK detection.

BCC 2-wire access data Byte setting, R_2WIRE_PASS_DATA_BYTE_NUM, should be set as more than intended burst read/write byte number in order to detect remote 2-wire NACK detection. If actual burst data access number is more than R_2WIRE_PASS_DATA_BYTE_NUM, remote 2-wire NACK event in remain number access is not feed backed to the HOST SoC 2-wire controller.

14) BCC remote 2-wire access NACK handling.

NACK indicates the problem on remote 2-wire operation. The next 2-wire access with no time takes over the broken operation and fails, then the 2nd next access with no-time recovers and behaves normal. In order to handle the next 2-wire access following NACK, dummy access may works to return to normal 2-wire operation. Another method is to wait for time out of broken BCC communication. After all the BCC time out, BCC also behaves normal.

15) Multiple Time Out Control.

In order to avoid miscommunication between local and remote BCC operation, time out timing parameter must be set as Local 2-wire Time Out > 2-wire bridge Time Out > Remote device Time Out. Default parameters keep this rule. Parameter change like BC_WDT should be carefully selected along with the rule.

16) Care on PLL and mode setting change

When PLL setting or mode setting is changed, proper wait time after setting change is required. 100ms is an example. Another method is to power down PLL before any PLL and mode setting change and to re-power on after changed. Mode change settings include DUPLICATE_REG(Low frequency mode), HIGHFREQIN_REG, R_LFEN and R_BPDEN.

17) BCC swap

THCV333 0x0108 TXLSWAP_REG swaps not only video but also BCC control is swapped. Users must care.

18) I2S_WC default output

THCV334 I2S_WC output setting-done behavior with no THCV333 I2S input is toggle output.
THCV334 I2S_WC output setting-done behavior with THCV333 I2S input is normal output.

19) Remote 2-wire NACK interrupt clear and reset

THCV334 0x1359 INTN_ERR_MASTER_NOACK_DET_M detection must be remote BCC accessed and cleared once happened if users continuously want to watch this interrupt. In other ways, remote NACK itself can be detected by 2-wire NACK itself not by interrupt function.

20) Remote 2-wire external target write timing consideration

Some remote 2-wire external target has "Write Cycle Time" specification like EEPROM. In this case, user should pay attention to remote side 2-wire communication timing between previous transaction STOP condition and next transaction START condition, which is supposed to be longer than "Write Cycle Time", however, may differ from the local 2-wire communication timing especially in burst write.

21) Frequency and setting care

The THCV333-Q requires internal settings to be adjusted according to the PCLK (FOLDIIN) from Open-LDI per port. See the table below for details.

PCLK (FOLDIIN)		
Item	10MHz to 25MHz	25MHz to 150MHz
PLL (0x0271 to 0x0278)	See 7.3.20 section	Auto (Default)

PCLK (FOLDIIN)		
Item	10MHz to 85MHz	85MHz to 150MHz
ULDT_EN (0x0019 bit[2:0])	0x7 (Default)	0x3

PCLK (FOLDIIN)		
Item	10MHz to 60MHz	60MHz to 150MHz
R_BPDEN (0x0506 bit[0])	0x0 (Default)	0x1

PCLK (FOLDIIN)		
Item	10MHz to 30MHz	30MHz to 150MHz
R_LFEN (0x0503 bit[0])	0x1	0x0 (Default)

PCLK (FOLDIIN)		
Item	10MHz to 60MHz	60MHz to 150MHz
HIGHFREQIN (0x0103 bit[0])	0x0	0x1 (Default)

The THCV333-Q also requires internal settings to be adjusted according to the V-by-One® HS II serial stream rate. See the table below for details.

V-by-One® HS II serial stream rate (TTFCBIT)		
Item	1.5Gbps to 1.6Gbps	1.6Gbps to 3.75Gbps
FLTSEL (0x091A bit[3:0])	0x8	0x0 (Default)

The THCV334-Q requires internal settings to be adjusted according to the V-by-One® HS II PCLK (PCLK.input). See the table below for details.

V-by-One® HS II PCLK.input		
Item	25MHz to 60MHz	60MHz to 133.3MHz
HIGHFREQIN (0x0103 bit[0])	0x0	0x1 (Default)

The THCV334-Q also requires internal settings to be adjusted according to the PCLK (FOLDIOUT) from Open-LDI per port. See the table below for details.

PCLK (FOLDIOUT)		
Item	10MHz to 25MHz	25MHz to 170MHz
PLL (0x0271 to 0x0278)	See 7.3.20 section	Auto (Default)

PCLK (FOLDIOUT)		
Item	10MHz to 30MHz	30MHz to 170MHz
R_LFEN (0x0504 bit[0])	0x1	0x0 (Default)

22) External pull-up register with internal pull-down register

THCV333-Q FCTHRIO_MODE, LINPUTMODE_BM0, FCOUTPUTMODE_BM1, and AIN have internal pull-down register at power up default. THCV334-Q FCTHRIO_MODE, FCINPUTMODE_BM1, LOUTPUTMODE_BM0, OE, and AIN have internal pull-down register at power up default. The value of internal pull-down register had better be considered as 29kohm. 2.2kohm +/-10% external pull-up register or smaller value register is an example to achieve external pull-up at power up default.

PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

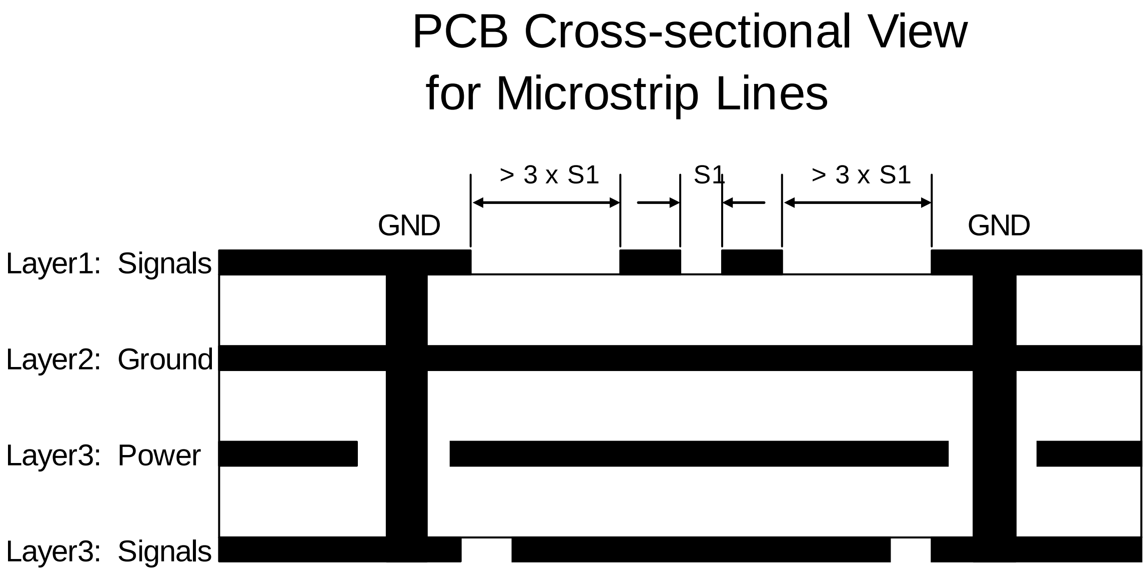


Figure 14 PCB cross-sectional view

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