

THTVS321

Transient Voltage Suppressor for I/O protection

General Description

THine THTVS Transient Voltage Suppressor family is designed to protect sensitive interconnect I/O from overvoltage caused by ESD (Electrostatic discharge), CDE (Cable Discharge Events) and EFT (Electrical fast transients).

The THTVS321 single-channel TVS is low capacitance ESD protection device which designed to protect sensitive CML, PECL LVDS physical layer for ASIC, FPGA, SOC, ASSP and Display port ,HDMI , PCIe and USB3.0 standard I/O.

The THTVS321 have extra small capacitance of 0.17pF (Typ) and working voltage of 3.6V Vrwm.

This allows to be used on circuits operating around up to 10GHz with signal integrity. They may be used to meet the ESD immunity requirements of IEC 61000- 4-2 Leve4.

The dynamic resistance is extremely low 0.18 Ohms (Typ) providing optimum protection of sensitive circuits.

The THTVS321 is designed to protect a single-end lines. For differential lines, two THTVS321s will be employed.

The THTVS321 is in a small 2-pin 0.6 x 0.3 x 0.25mm package. Low capacitance, small package, and high level of ESD protection will makes a flexible solution for high speed applications.

Features

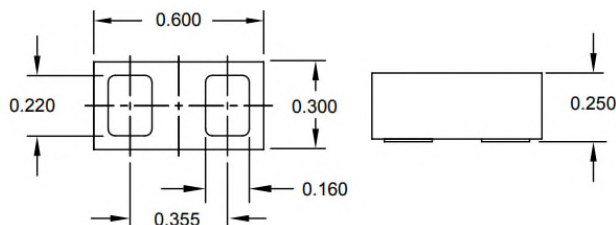
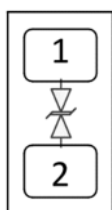
- ESD protection IEC 61000-4-2(ESD) ±8kV(contact), ±15kV(Air)
- Ultra-small package
- Protect one line
- Low capacitance: 0.17pF Typ
- Low dynamic resistance: 0.18 Ohm typ
- Operating voltage: Vrwm 3.6V
- Two pin package (0.6 x 0.3 x 0.25mm)
- Packaging: Tape and Reel

Applications

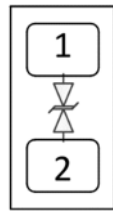
Applications for sensitive and high speed I/O protection as followed.

- FPGA/SoC high Seed I/O.
- CML/PECL/LVDS physical layer
- HDMI/DVI/DisplayPort™
- PCIExpress /eSATA
- Thunderbolt3
- USB3.0/3.1
- V-by-One® HS
- Sensitive Sensor I/O
- Connector and cable I/F

Schematic and package Diagram



Pin Configuration



Package pin configuration (Top view)

Pin Description

Pin No	Type	Description
1	I	Input or Ground ^{*1}
2	I	Input or Ground ^{*1}

*1: Ground must be tied to the PCB ground plane. Low impedance connection required.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Peak Pulse Power (tp = 1.2/50μs)	P _{Pk}	45	W
Peak Pulse Current (tp = 1.2/50μs)	I _{pp}	7	A
ESD per IEC 61000-4-2 (Air) ^{*1} ESD per IEC 61000-4-2 (Contact) ^{Notw}	V _{ESD}	+/- 15 +/- 8	kV
Operating Junction Temperature	T _J	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Notes.

*1: Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

Electrical Characteristics (T_j=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V _{RWM}	-	-	-	3.6	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA -40 to 85°C	5.5	8	10	V
Reverse Leakage Current	I _R	V _{RWM} = 3.6V	-	5	50	nA
Holding Current	I _H	-	50	120	-	mA
Clamping Voltage ^{*2}	V _C	tp=1.2/50μs(Voltage), 8/20μs(Current) Combination Waveform, R _S = 2Ω I _{pp} = 7A	-	5	6.5	V
ESD Clamping Voltage ^{*3}	V _C	I=4A, tp=0.2/100ns(TLP)	-	3.3	-	V
		I=16A, tp=0.2/100ns(TLP)	-	5.5	-	
Trigger Voltage ^{*3}	V _{TRIG}	Tp=0.2/100ns(TLP)	-	9.4	-	V
Dynamic Resistance ^{*4}	R _{DYN}	tp=0.2/100ns(TLP)	-	0.18	-	Ω
Junction Capacitance	C _j	V _R = 0V, f = 1MHz,	-	0.17	0.2	pF

Notes

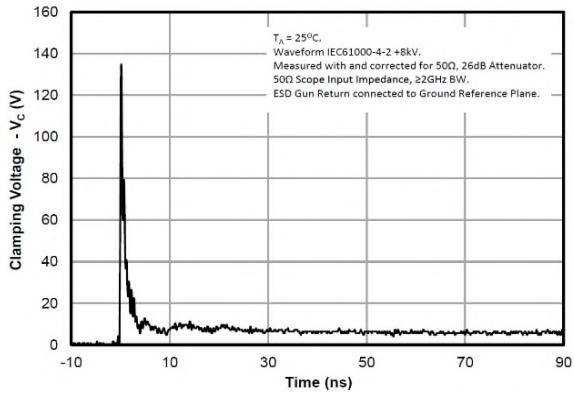
*2 Measured using a 1.2/50us voltage, 8/20us current combination waveform, RS = 8 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

*3 Transmission Line Pulse Test (TLP) Settings tp = 100ns, tr = 0.2ns, TLP I and V averaging window: t1 = 70ns to t2 = 90ns.

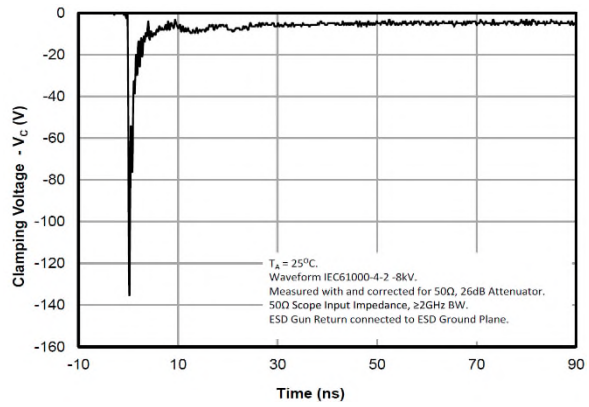
*4 Dynamic resistance calculated from I TLP = 4A to I TLP = 16A

Typical Characteristics

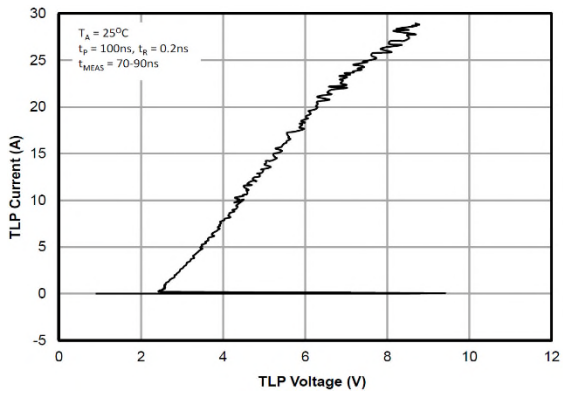
ESD Clamping (8kV Contact per IEC 61000-4-2)



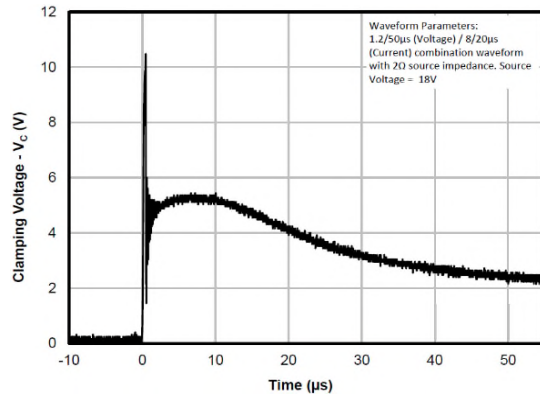
ESD Clamping (-8kV Contact per IEC 61000-4-2)



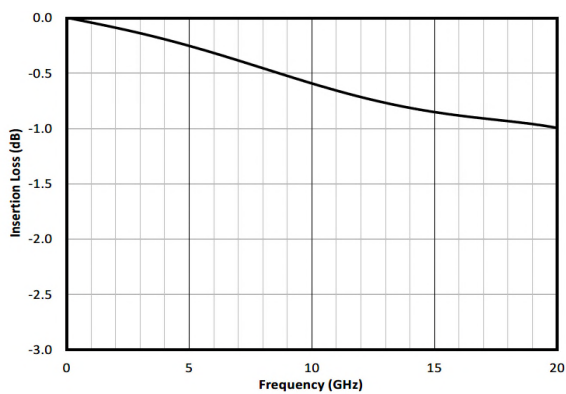
TLP Characteristic (Positive Pulse)



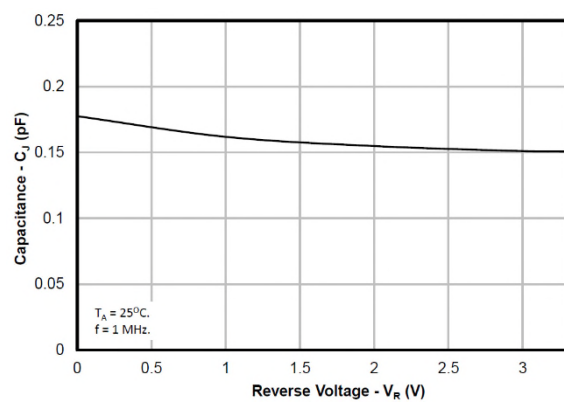
Clamping Characteristic



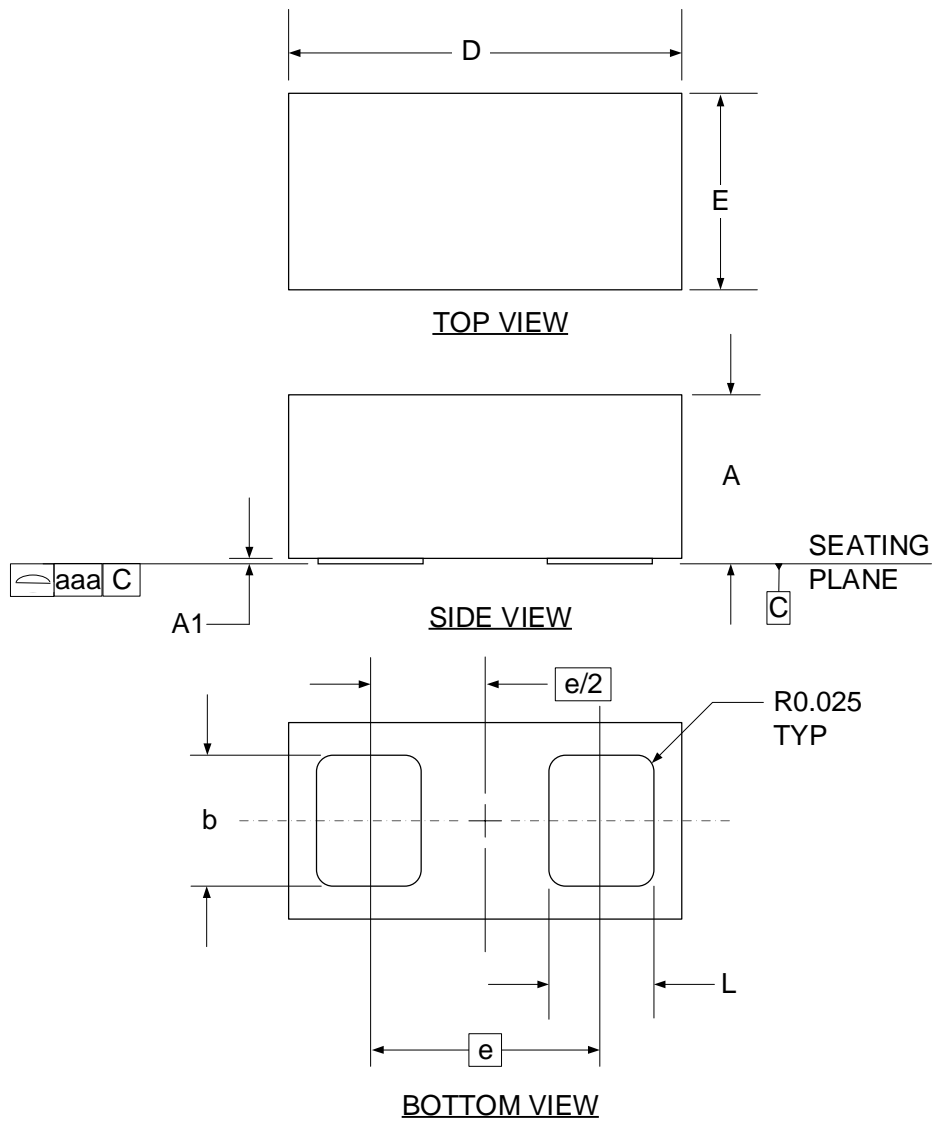
Insertion Loss - S21



Capacitance vs. Reverse Voltage

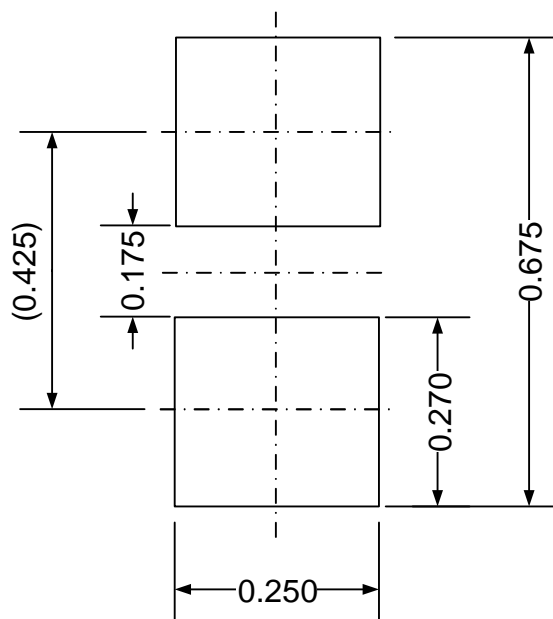


Package



Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	0.235	0.250	0.265
A1	Standoff	0.000	0.010	0.050
b	Terminal Width	0.200	0.220	0.240
D	Body Length	0.580	0.600	0.620
E	Body Width	0.280	0.300	0.320
e	Pitch	0.355 BSC		
L	Terminal Length	0.140	0.160	0.180
aaa	Coplanarity	0.08		

Land Pattern



TOP VIEW

Unit : mm

(Note)

Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjust the Land Pattern at your own risk.

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.
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