THCS253

I2C/GPIO High Speed Bus Signal Transceiver

System Design Guide

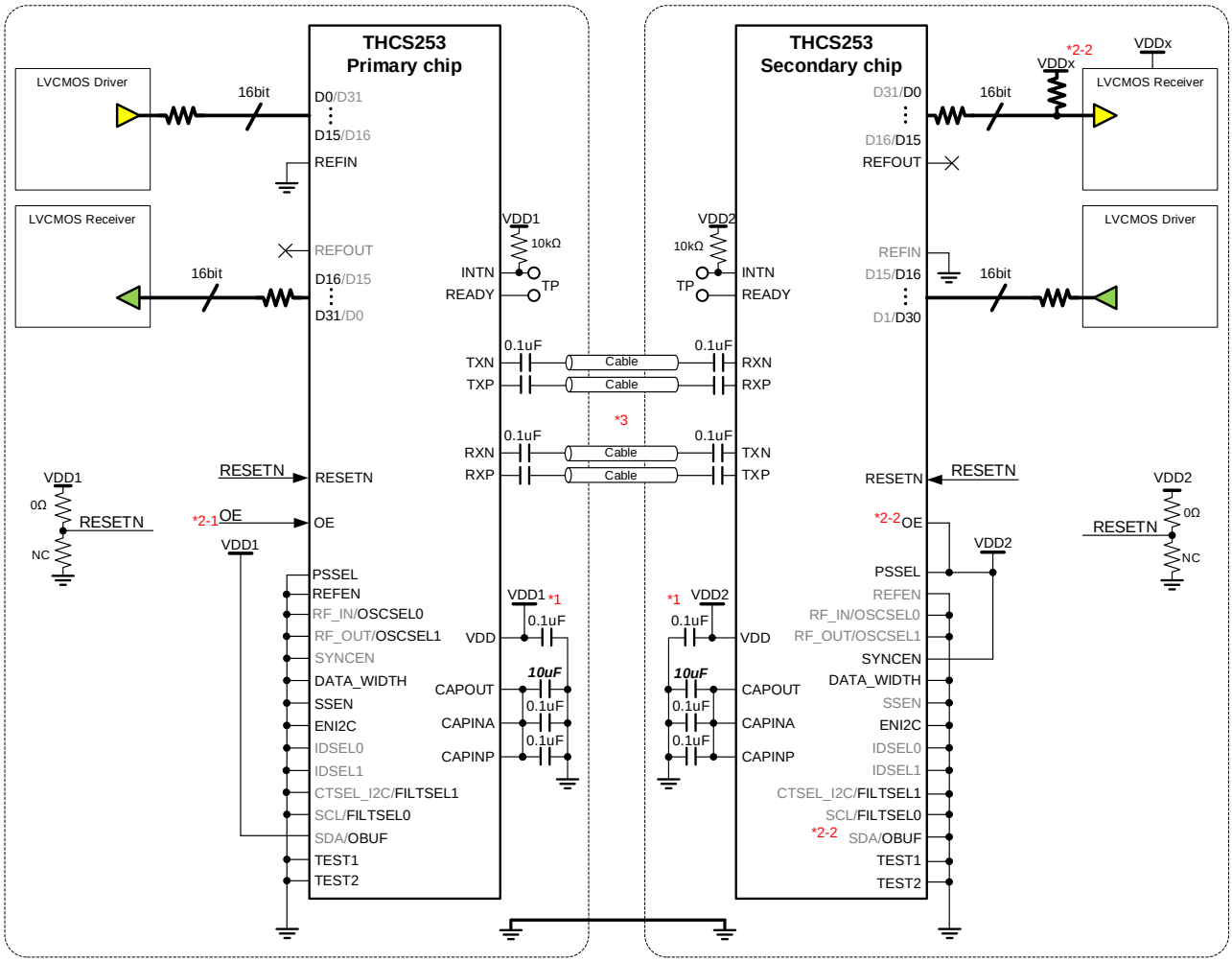
Contents

Example 1. I/O extension, Up/Down Stream synchronous mode

The primary chip performs parallel/serial conversion of input data using either the clock signal input to the REFIN pin or the built-in oscillator clock signal, whichever is selected, and outputs it from the TXP/N pin as a clock embedded serial signal. Secondary chip set to synchronous mode (SYNCEN pin = High) operate with clock signals regenerated from clock-embedded serial signals input to both the serial/parallel conversion circuit and the parallel/serial conversion circuit on the RXP/N pin. The Up/Down Stream will therefore have the same transmission bit rate.

Example 1 is an example of transmitting 16-bit GPIO data sampled asynchronously by the 20 MHz built-in oscillator clock on the Primary chip to the Secondary chip, and transmitting 16-bit GPIO data sampled asynchronously by the 20 MHz clock regenerated on the Secondary chip set to synchronous mode. This is an example of transmitting 16-bit GPIO data sampled asynchronously by a 20 MHz clock regenerated by the Secondary chip set to synchronous mode to the Primary chip.

When I2C is not used, all THCS253 settings are made at the setting terminals.



■Power supply（*1）

The Primary chip (VDD1) and Secondary chip (VDD2) can be used with different supply voltages.

■Data output control in start-up sequences

If I2C is not used, there are two options.

- Output enable control by OE pin（*2-1）

- Set to open drain output and pull-up with receive side power supply（*2-2）

■Disposal of unused terminals

Unused inputs should be fixed Low and outputs should be open.

■Cable for connection between Primary chip and Secondary chip（*3）

Use twisted pair cables with a differential impedance of 100 Ω. Impedance error should be within ±10%, but this is not a limitation if the signal waveform observed near the RXP/RXN terminals meets the Eye opening described in the datasheet.

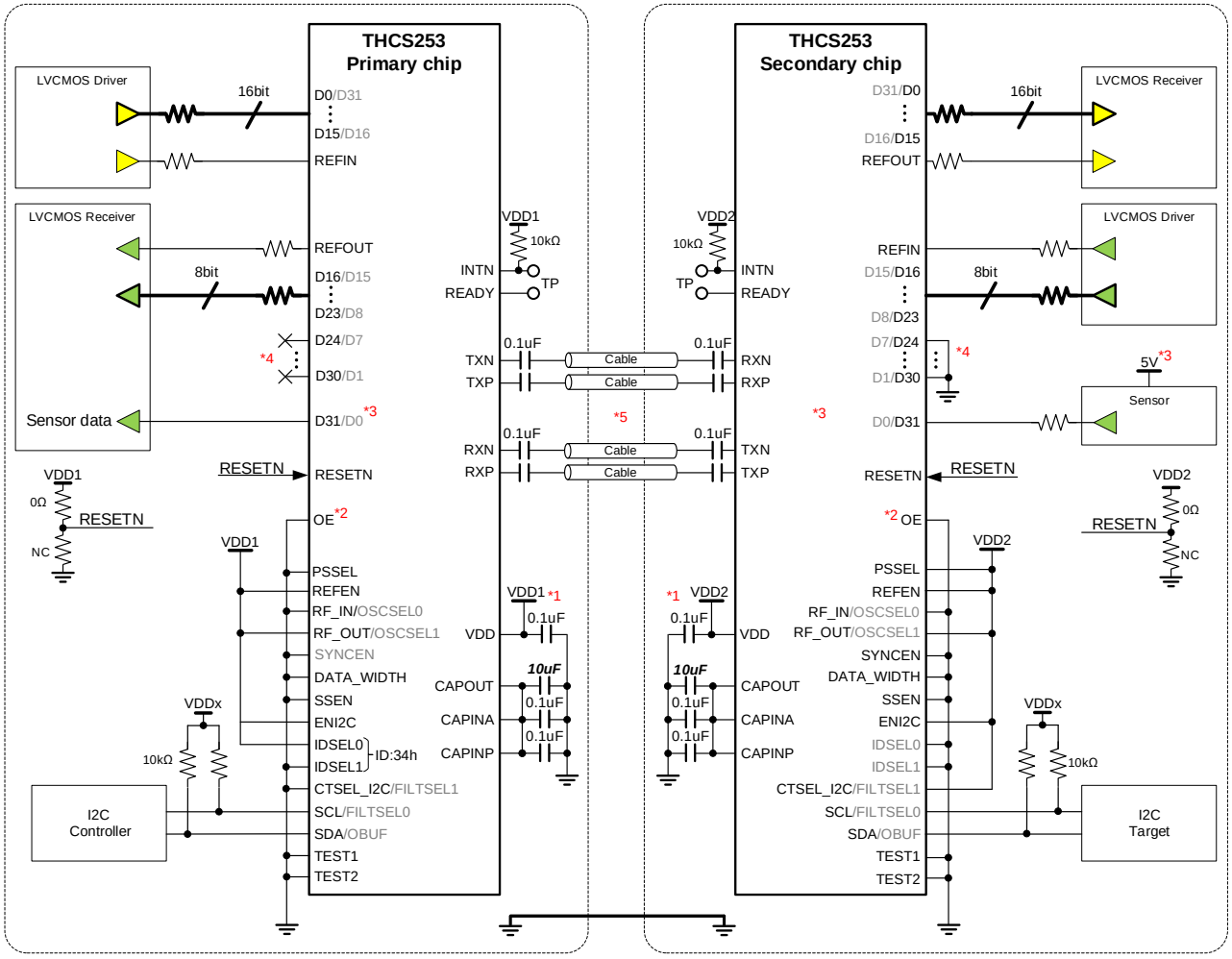
When unshielded twisted pair cables are bundled with other signal lines or power lines, data errors may occur due to crosstalk between the lines, resulting in malfunctions. Twisted pair cables must be shielded for each pair.

Example 2. I/O & I2C extension, Up/Down Stream asynchronous mode

The primary chip and secondary chip perform parallel/serial conversion with the REFIN pin input clock signal or the internal oscillator clock signal selected by each chip, and output from the TXP/N pin as clock embedded serial signals. Therefore, the bit rate of the Up/Down stream signal is based on the clock signal frequency selected for each chip.

Example 2 shows an example of transmitting I2C data in addition to GPIO data sampled at the falling edge of the clock signal input to each REFIN pin.

When using I2C, some settings (input/output direction, output buffer type, and digital filter settings) are set in registers.



■Power supply（*1）

The Primary chip (VDD1) and Secondary chip (VDD2) can be used with different supply voltages.

■Data output control in start-up sequences（*2）

By fixing the OE pin to Low, all GPIO pins are disabled (Hi-Z) in the initial state immediately after power-on, avoiding unnecessary voltage application to the connected devices. From this state, set the input/output polarity and output buffer type of each GPIO pin using the GPIO_OEN and GPIO_OBUF registers, and then set the OVERRIDE_OE register to "1" to enable GPIO, overriding the register setting over the OE pin setting.

Step 1. All outputs disabled by OE pin = Low （Hi-Z）

Step 2. GPIO_OEN、GPIO_OBUF, Set GPIO_I_FILTEN register as needed
Step 3. OVERRIDE_OE register is set to “1”

■5V Tolerant I/O、Voltage Level Conversion（*3）

There are up to four-5V input and output pins each. In the above example, a signal output from a 5V driven sensor is input to the 5V input terminal on the secondary chip side and output from the primary chip side at VDD1 voltage for 5V to VDD1 level conversion.

To use the 5V tolerant output pin as a 5V signal output, set the corresponding pin as an open drain and pull up to 5V externally.

■Disposal of unused terminals（*4）

Unused inputs should be fixed Low and outputs should be open.

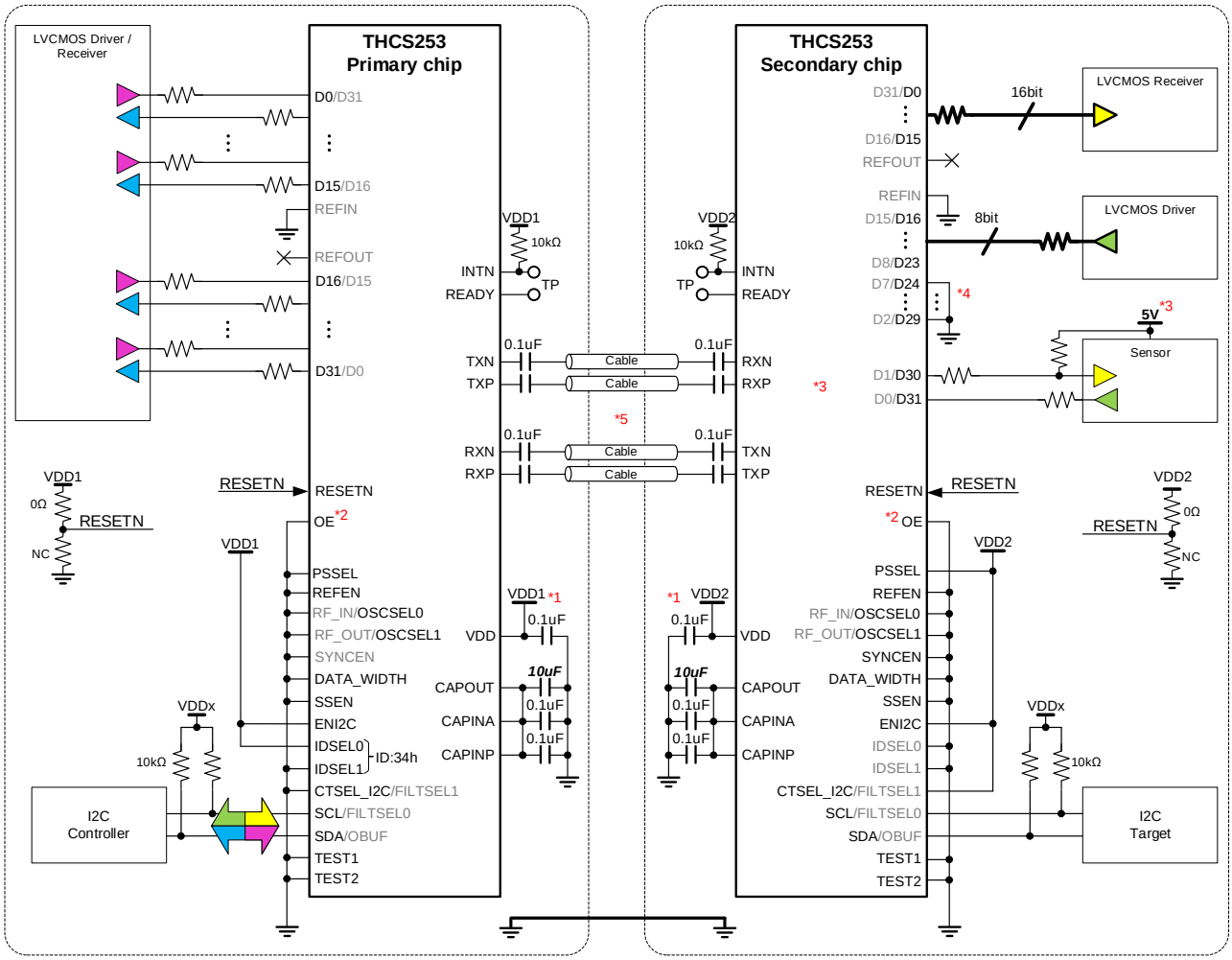
■Cable for connection between Primary chip and Secondary chip（*5）

Use twisted pair cables with a differential impedance of 100 Ω. Impedance error should be within ±10%, but this is not a limitation if the signal waveform observed near the RXP/RXN terminals meets the Eye opening described in the datasheet.

When unshielded twisted pair cables are bundled with other signal lines or power lines, data errors may occur due to crosstalk between the lines, resulting in malfunctions. Twisted pair cables must be shielded for each pair.

Example 3. I/O expansion with I2C

This mode uses I2C to control the state of each GPIO pin individually.



■Power supply（*1）

The Primary chip (VDD1) and Secondary chip (VDD2) can be used with different supply voltages.

■Data output control in start-up sequences（*2）

By fixing the OE pin to Low, all GPIO pins are disabled (Hi-Z) in the initial state immediately after power-on, avoiding unnecessary voltage application to the connected devices. From this state, set the input/output polarity and output buffer type of each GPIO pin using the GPIO_OEN and GPIO_OBUF registers, and then set the OVERRIDE_OE register to "1" to enable GPIO, overriding the register setting over the OE pin setting.

Step 1. All outputs disabled by OE pin = Low （Hi-Z）
Step 2. I2C_EXPAND register is set to “1”
Step 3. GPIO_OEN、GPIO_OBUF, Set GPIO_I_FILTEN register as needed
Step 4. OVERRIDE_OE register is set to “1”

■5V Tolerant I/O、Voltage Level Conversion（*3）

There are up to four-5V input and output pins each. In the above example, a signal output from a 5V driven sensor is input to the 5V input terminal on the secondary chip side and output from the primary chip side at

VDD1 voltage for 5V to VDD1 level conversion.

To use the 5V tolerant output pin as a 5V signal output, set the corresponding pin as an open drain and pull up to 5V externally.

■Disposal of unused terminals（*4）

Unused inputs should be fixed Low and outputs should be open.

■Cable for connection between Primary chip and Secondary chip（*5）

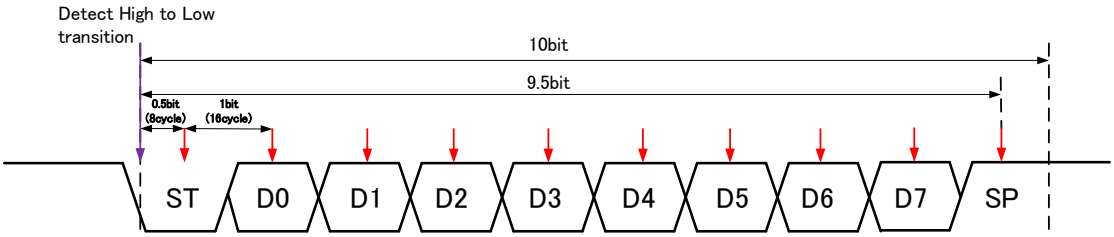
Use twisted pair cables with a differential impedance of 100 Ω. Impedance error should be within ±10%, but this is not a limitation if the signal waveform observed near the RXP/RXN terminals meets the Eye opening described in the datasheet.

When unshielded twisted pair cables are bundled with other signal lines or power lines, data errors may occur due to crosstalk between the lines, resulting in malfunctions. Twisted pair cables must be shielded for each pair.

Baud rate calculation method for UART communication

When propagating UART signals, sampling errors on the GPI pin that inputs the UART signals limit the baud rate of the UART device and the clock accuracy of the baud rate generator compared to when THCS253 is not used.

The following is an example of a UART communication method with 1-bit start bit, 8-bit data without parity, 1-bit stop bit, and 16 times baud rate oversampling for the receiving device.



The receiving device considers the sampling data 0.5 bits (8 sampling cycles) after detecting Low to be the start bit if it is Low, and then captures 8 bits of data and 1 bit of stop bit every 1 bit (16 sampling cycles) for a total of 9 times. In this case, if each bit is ideally sampled in the center, there is a margin of ±0.5 bits relative to the sampling point. However, it is necessary to take into account the sampling error in detecting the first low at the receiving side (one sampling period at the receiving side), the input setting time, the THS254 sampling error, and the baud rate error between transmission and reception, which requires attention in asynchronous communications. Since the baud rate is generated by dividing the clock source of the UART transmitter/receiver device, an error in the clock source can be considered a baud rate error as it is. It should also be noted that baud rate error is different in nature from sampling error and is an accumulated error. In other words, in order to accurately sample the stop bit 9.5 bits after the first low is detected, there must remain a margin of at least the input setup and hold time required for the receiving device after 9.5 bits. Therefore, the allowable baud rate error per bit is the remaining time after subtracting each sampling error and setup time from the 0.5-bit margin, divided by 9.5 bits. This results in the following equation for the baud rate tolerance between UART transmitting and receiving devices.

$$\left\{\left(\frac{1}{2\times BAUD}-\frac{1}{16\times BAUD}-\frac{1}{REFCK}-tSH\right)\div 9.5\right\}\div\frac{1}{BAUD}\times 100 > Baud\ \ rate\ \ tolerance(\%)$$

BAUD : Baud rate (Hz)
REFCK : THCS253 operation frequency (Hz)
tSH : UART device input setup/hold time, whichever is greater (sec)

Note that the baud rate error is the relative difference in baud rates generated at each of the transmitter and receiver. For example, if your device has a tolerance of ±2% on the transmit side and ±1% on the receive side for the clock source, the relative maximum error is 3%.

With a UART device input setup and hold time of 10ns and a THCS253 internal oscillator set to 80MHz (*tOSC = max.15.7ns), the acceptable baud rate error for UART communication at a baud rate of 1Mbps is approximately 4.3% according to the above formula. The baud rate error is about 4.3%.If the maximum baud rate error of the UART device used is 4%, it means that communication is possible at a maximum baud rate of 2.56 Mbps. However, since there may be factors other than the above formulas such as transition time depending on the environment, the above calculations should be considered only as a guide and should be used with a sufficient margin.

SCLK frequency calculation method for SPI communication

Write operation

It is calculated by the following formula, which takes into account the sampling error at the GPI pin input and the setup/hold time of the SPI Target device input.

$$\frac{1}{2 \times fSCLK} > \left(\frac{1}{REFCK}\right) + tSUP/tHLD$$

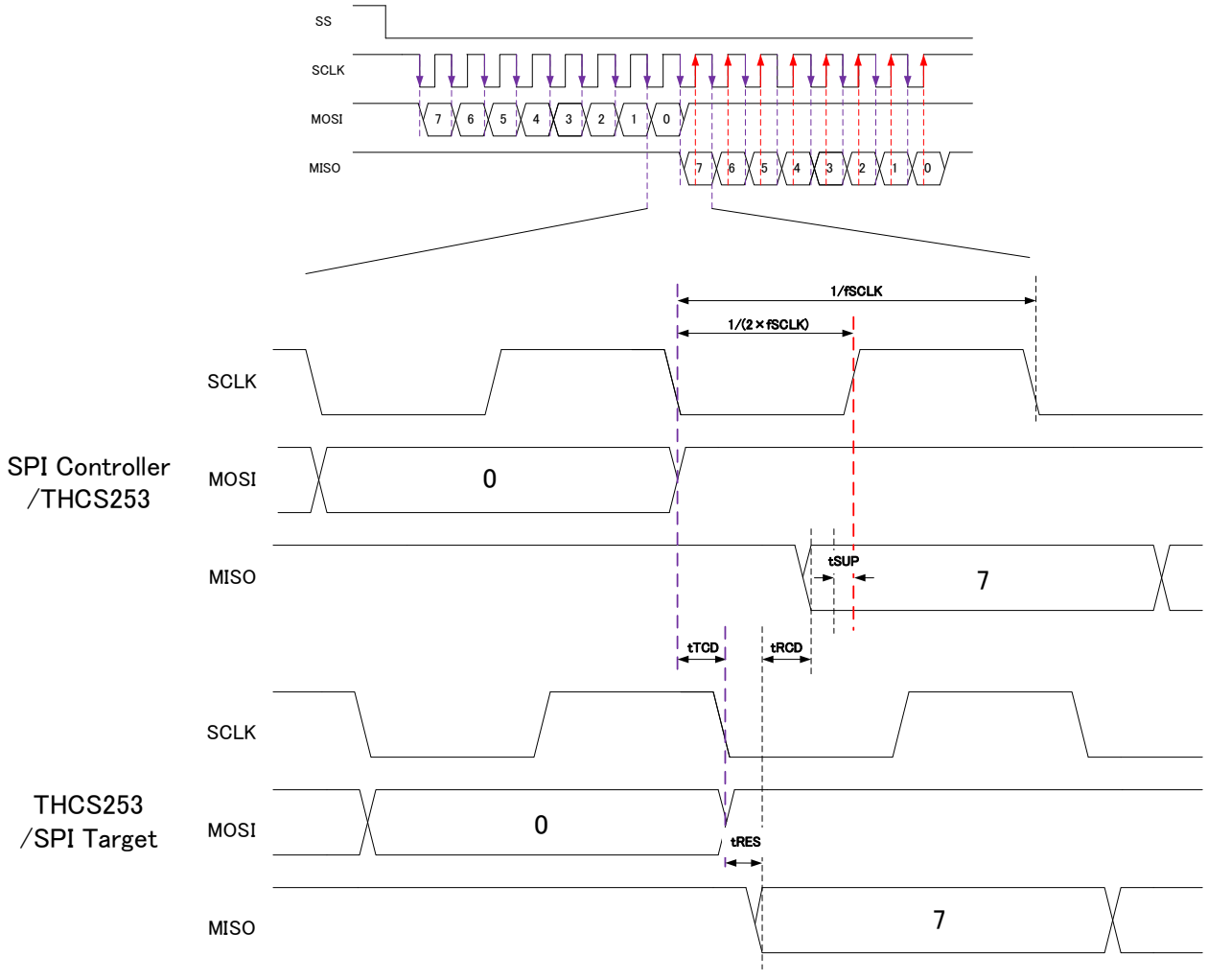
fSCLK	:	SCLK frequency (Hz)
REFCK	:	THCS253 operation frequency (Hz)
tSUP/tHLD	:	SPI Controller device input setup/hold time (sec)

If the tSUP/tHLD time is 10ns and REFCK is 80MHz, the maximum SCLK is 22MHz from the above formula.

Read operation

Read speed is limited by the delay (tTCD, tRCD) between Primary/Secondary of THCS253 and sampling error (equivalent to REFCK) at GPI pin input.

The timing chart for SPI read is shown below.



For the SPI Controller device to sample Read data correctly, the total delay shown in the timing chart above must be less than SCLK period x 1/2. Since the above timing chart does not show the sampling error due to asynchronous sampling of THCS253, the following equation is obtained by adding the sampling error (1/REFCK) to tTCD and tRCD.

$$\frac{1}{2 \times fSCLK} > \left(tTCD + \frac{1}{REFCK}\right) + tRES + \left(tRCD + \frac{1}{REFCK}\right) + tSUP$$

fSCLK	:	SCLK frequency (Hz)
REFCK	:	THCS253 operation frequency (Hz)
tTCD	:	THCS253 Primary to Secondary delay time (sec)
tRCD	:	THCS253 Secondary to Primary delay time (sec)
tRES	:	SPI Target device response time (sec)
tSUP	:	SPI Controller device input setup time (sec)

Assuming that the response time of the SPI target device and the input setup time of the SPI controller device are 10ns each, the calculation results are as follows.

$$fSCLK < 317KHz$$

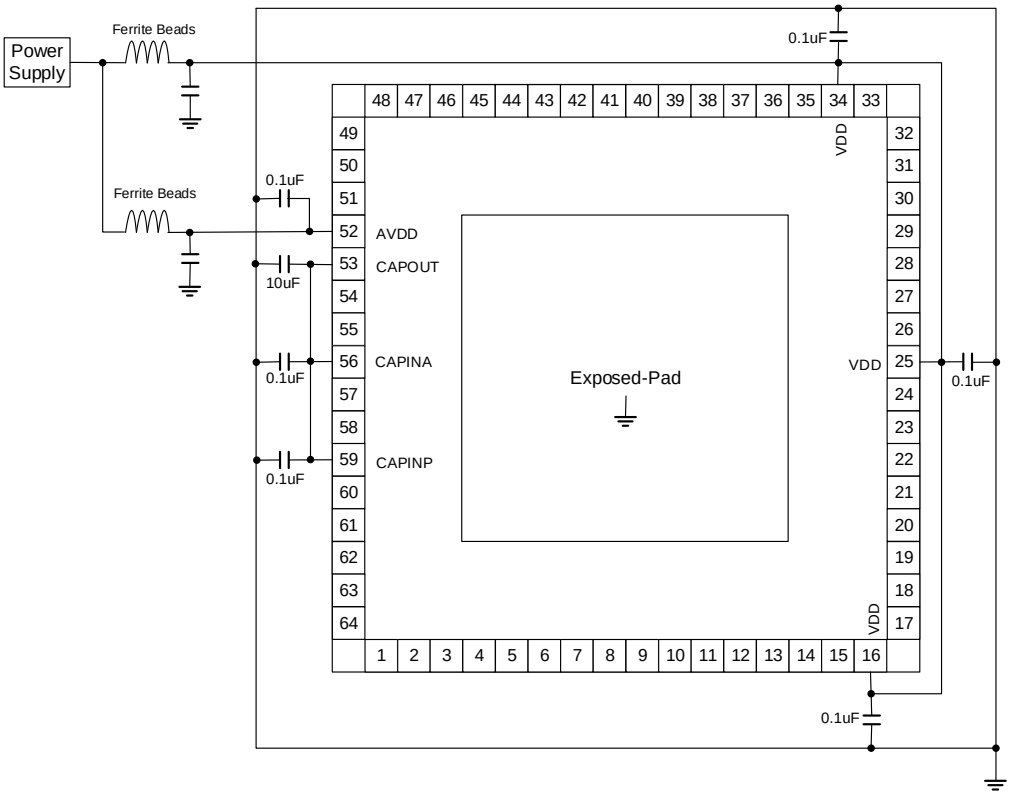
REFCK	:	80MHz
tTCD	:	12.5ns(80MHz)×61.3=766.2ns *digital noise filter disable
tRCD	:	12.5ns(80MHz)×61.3=766.2ns *digital noise filter disable
tRES	:	10ns
tSUP	:	10ns

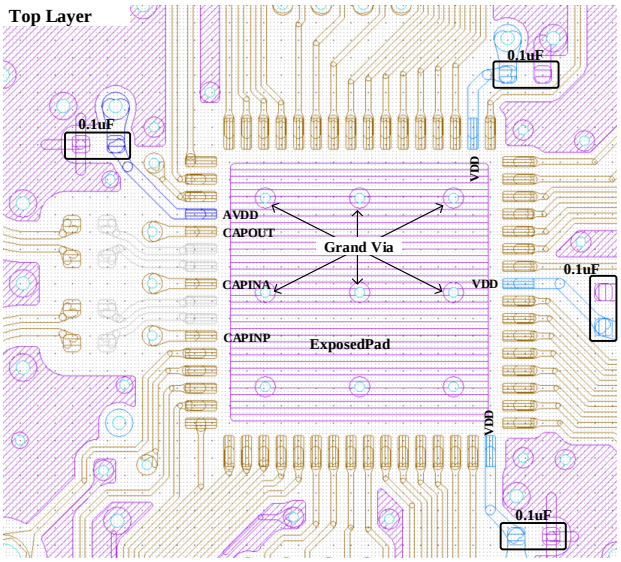
In the actual environment, multiple target devices are connected on the SPI bus, which deteriorates the transition time. The delay caused by this transition time deterioration cannot be ignored. In this case, the amount of delay due to transition time must be added to the right side of the above equation.

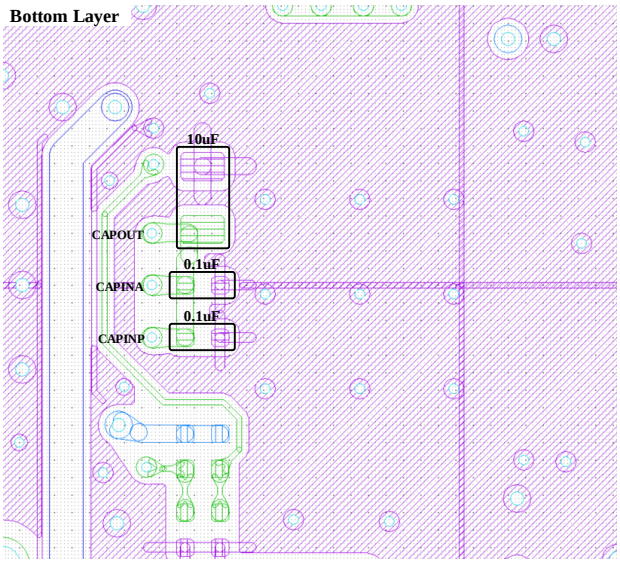
In the THCS series, either an external REFIN input or an internal oscillator can be selected as the REFCK, but it should be noted that the internal oscillator has a large frequency error. When using the THCS series product built-in oscillator, calculate using the maximum value of tOSC specified in the datasheet.

Design Guidelines for Power Supply

Insert filters (Ferrite Beads and Capacitors) in the Power Supply (VDD and AVDD).
And insert Bypass Capacitor (0.1uF) in the Power Supply pins.
This device is equipped with a 1.2V built-in regulator.
Insert Bypass Capacitors (CAPOUT: 10uF and CAPINA/CAPINP: 0.1uF) also for this regulator.
Bypass Capacitors should be attached just near the device. Insert the GND-Via to the Exposed-Pad to strengthen.

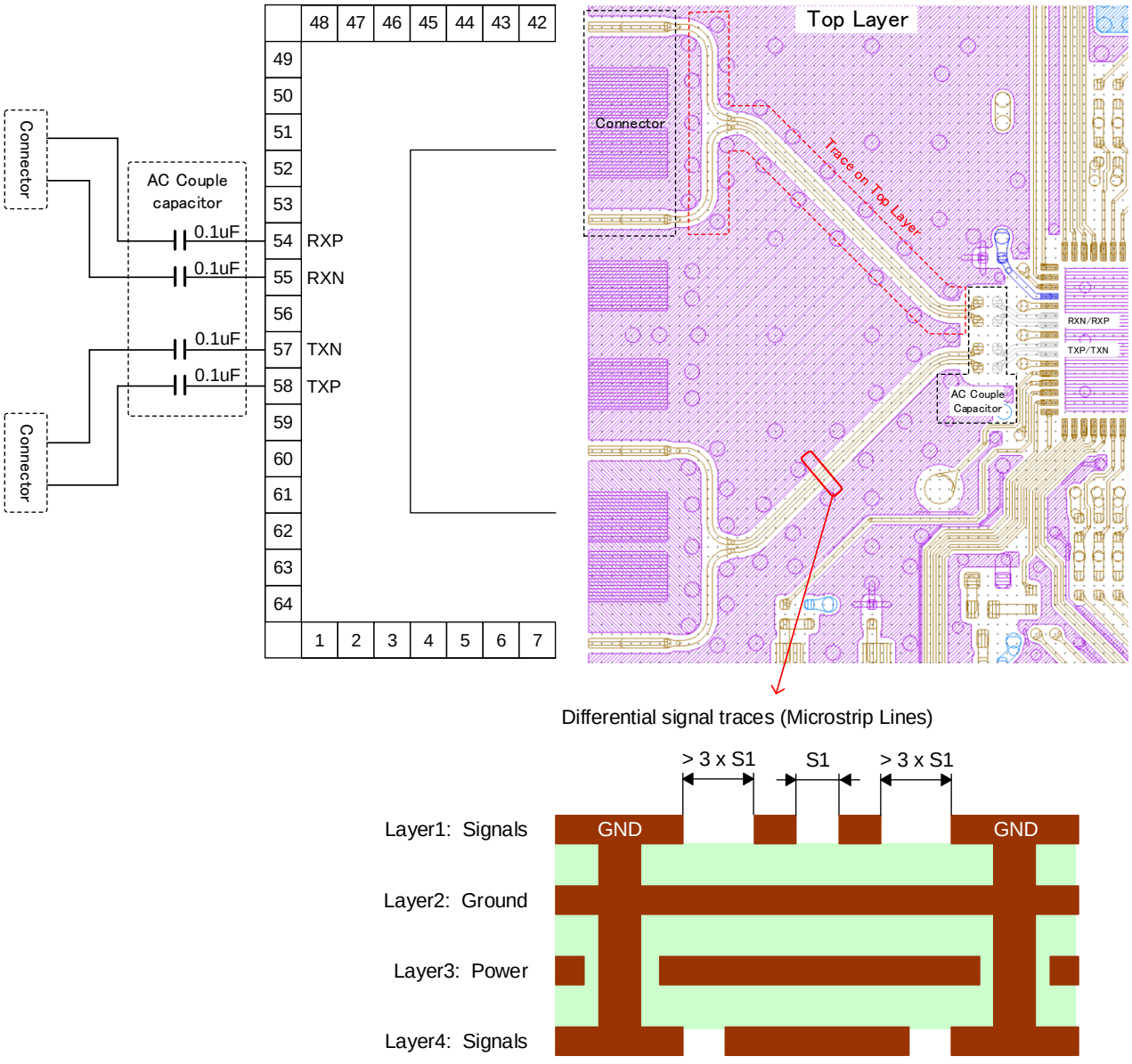






Design Guideline for High-Speed Signal

TXP/TXN and RXP/RXN are differential pairs of high-speed serial signals.
Differential pairs should be closely spaced and coupled to eliminate common mode noise.
Also, differential should be designed as 100Ω differential characteristic impedance (Zdiff).
The following is an example of microstrip line design.
The high-speed signal lines trace in only single layer.
The AC coupled capacitors should be attached just near the device.



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