THTVS411

Transient Voltage Suppressor for I/O protection

General Description

THine THTVS Transient Voltage Suppressor family is designed to protect sensitive interconnect I/O from overvoltage caused by ESD (Electrostatic discharge),CDE (Cable Discharge Events) and EFT (Electrical fast transients).

The THTVS411 single-channel TVS is low capacitance ESD protection device which designed to protect sensitive CML, PECL LVDS physical layer for ASIC, FPGA, SOC, ASSP and Display port ,HDMI ,PCIe and USB3.0 standard I/O.

The THTVS411 have a small capacitance of 0.45pF (Typ) and working voltage of 4V Vrwm.
This allows to be used on circuits operating around up to 8GHz with signal integrity. They may be used to meet the ESD immunity requirements of IEC 61000- 4-2.
The dynamic resistance is extremely low 0.12 Ohms (Typ) providing optimum protection of sensitive circuits.
The THTVS411 is designed to protect a single-end lines. For differential lines, two THTVS411s will be employed.
The THTVS411 is in a small 2-pin 0.6 x 0.3 x 0.25mm package. Low capacitance, small package, and high level of ESD protection will makes a flexible solution for high speed applications.

Features

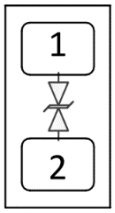
- ESD protection IEC 61000-4-2(ESD) ±25kV(air), ±20kV(contact)
- Ultra-small package
- Protect one line
- Low capacitance: 0.45pF Typ
- Low dynamic resistance: 0.12 Ohm typ
- Operating voltage: V_{rwm} 4.0V
- Two pin package (0.6 x 0.3 x 0.25mm)
- Packaging: Tape and Reel

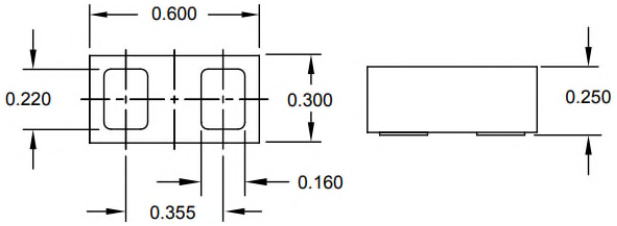
Applications

Applications for sensitive and high speed I/O protection as followed.

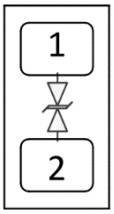
- FPGA/SoC/ASSP high Seed I/O.
- CML/PECL/LVDS physical layer
- HDMI/DVI/DisplayPort™
- PCI Express /eSATA
- USB3.0/3.1
- V-by-One® HS
- Sensitive Sensor I/O
- Connector and cable I/F

Schematic and package Diagram





Pin Configuration



Package pin configuration (Top view)

Pin Description

Pin No	Type	Description
1	I	Input or Ground*1
2	I	Input or Ground*1

*1: Ground must be tied to the PCB ground plane. Low impedance connection required.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Peak Pulse Power (tp = 1.2/50μs)	P_{Pk}	30	W
ESD per IEC 61000-4-2 (Air)*1 ESD per IEC 61000-4-2 (Contact)*1	V_{ESD}	+/- 25 +/- 20	kV
Operating Junction Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Notes.

*1: Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

Electrical Characteristics (Tj = 25 ℃)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	4.0	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	5.5	7.5	8.5	V
Reverse Leakage Current	I_R	V_{RWM} = 4.0V	-	-	50	nA
Holding Current	I_H	-	50	120	-	mA
Clamping Voltage*2	V_C	tp = 1.2/50μs Open Circuit,8/20μs Short Circuit Combination Waveform V_S = 16V,R_S = 2Ω , I_{SC} = 8A	-	5	8	V
ESD Clamping Voltage*3	V_C	I=4A,tlp=0.2/100ns	-	4.5	-	V
		I=16A,tlp=0.2/100ns	-	6	-	
Dynamic Resistance *4	R_{DYN}	tlp=0.2/100ns	-	0.12	-	Ω
Junction Capacitance	C_j	V_R = 0V, f = 1MHz,	-	0.45	0.55	pF

Notes

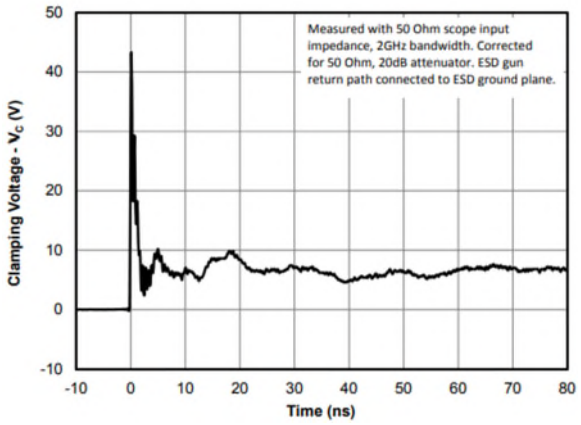
*2 Measured using a 1.2/50us voltage, 8/20us current combination waveform, RS = 8 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

*3 Transmission Line Pulse Test (TLP) Settings tp = 100ns, tr = 0.2ns, TLP I and V averaging window: t1 = 70ns to t2 = 90ns.

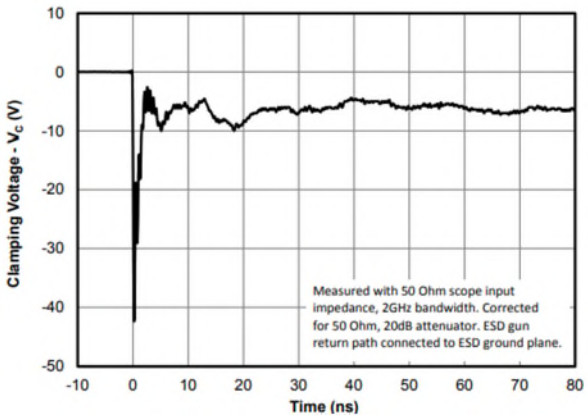
*4 Dynamic resistance calculated from I TLP = 4A to I TLP = 16A

Typical Characteristics

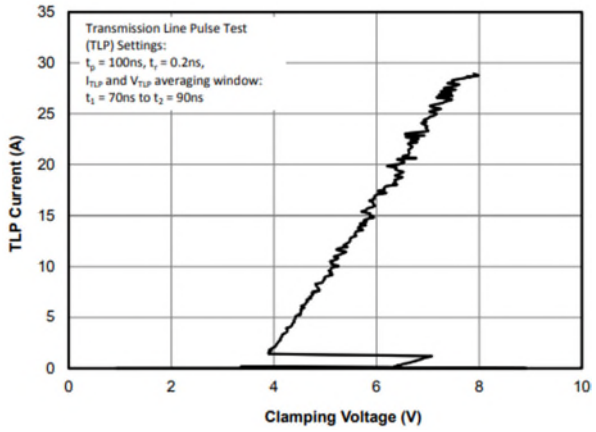
ESD Clamping (8kV Contact per IEC 61000-4-2)



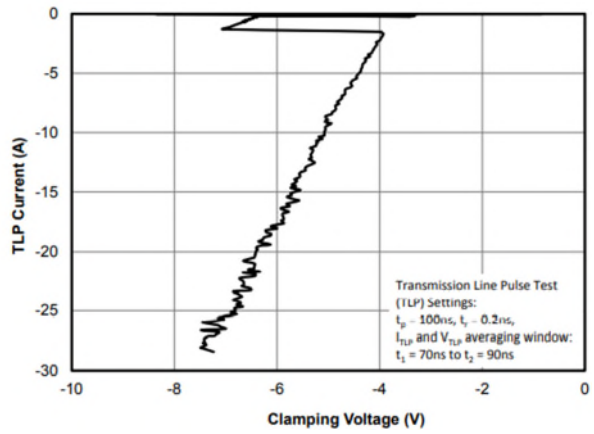
ESD Clamping (-8kV Contact per IEC 61000-4-2)



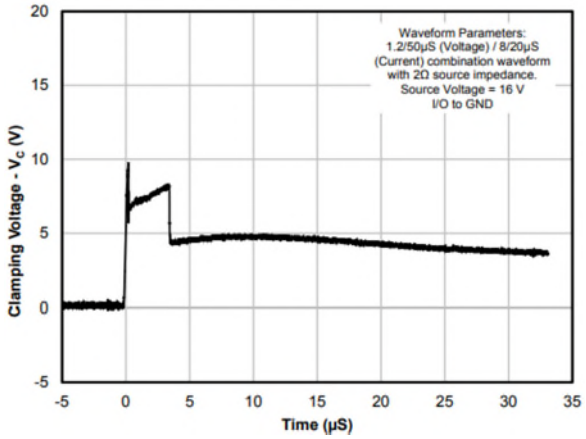
TLP Characteristic (Positive Pulse)



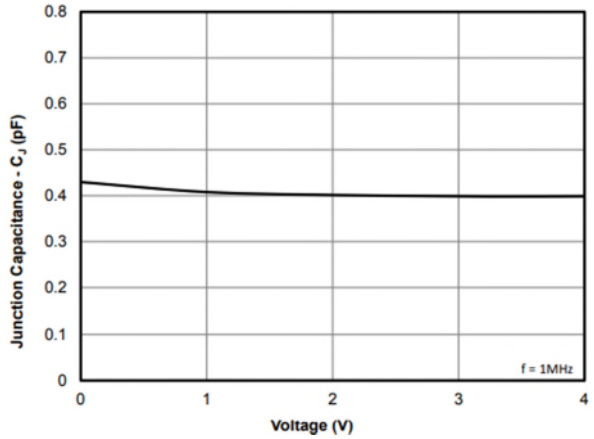
TLP Characteristic (Negative Pulse)



Clamping Characteristic

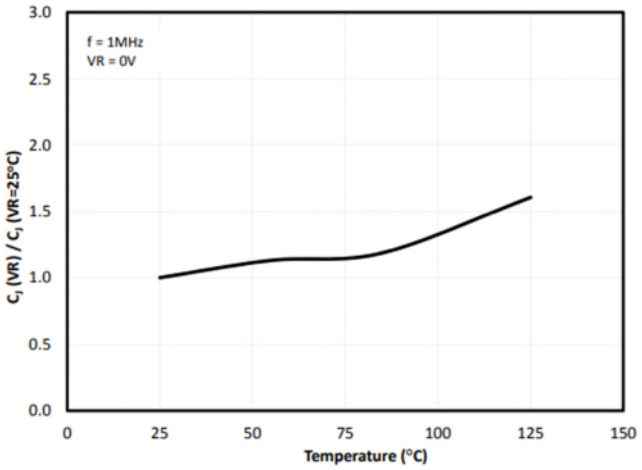


Capacitance vs. Reverse Voltage

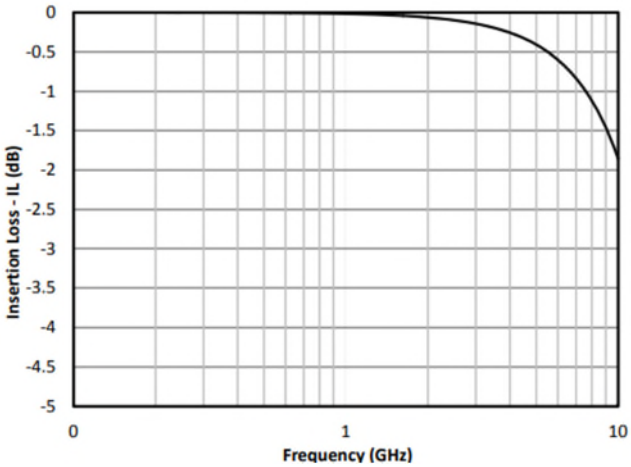


Typical Characteristics

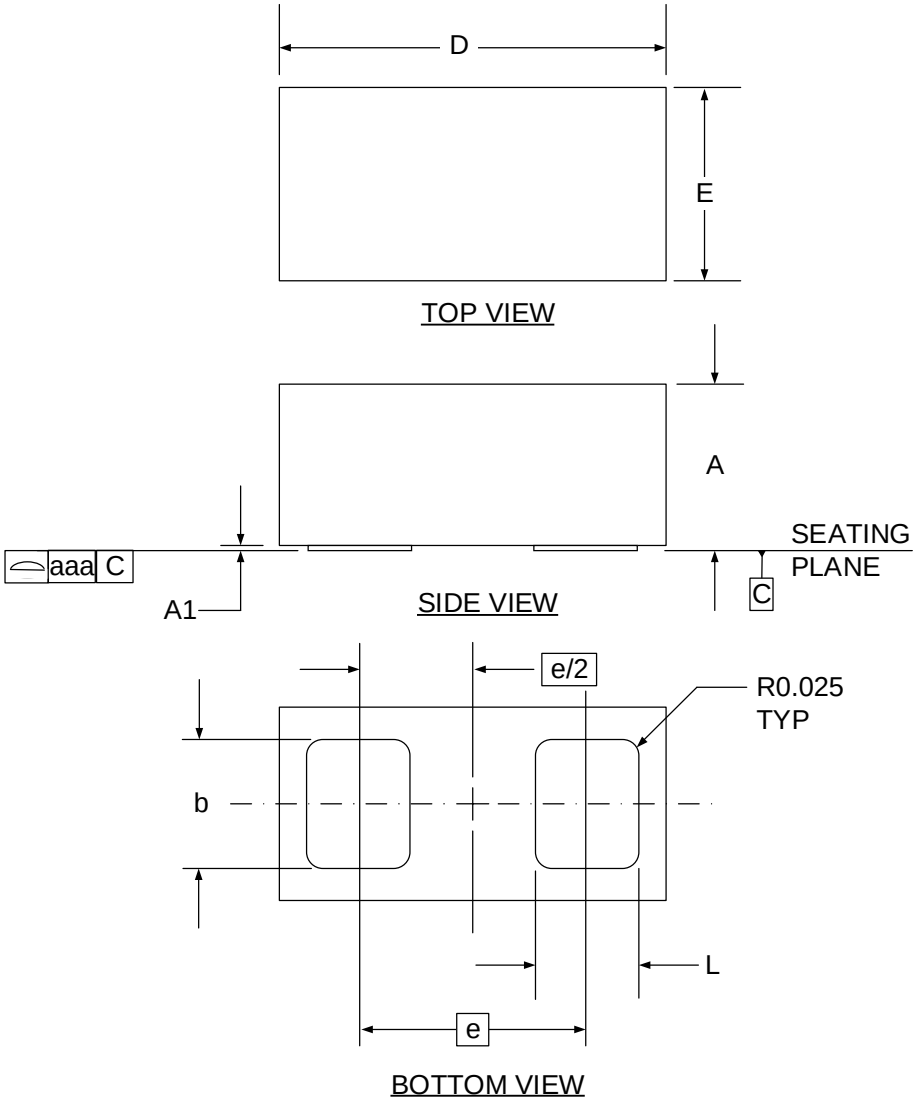
Capacitance vs. Temperature



Insertion Loss - S21



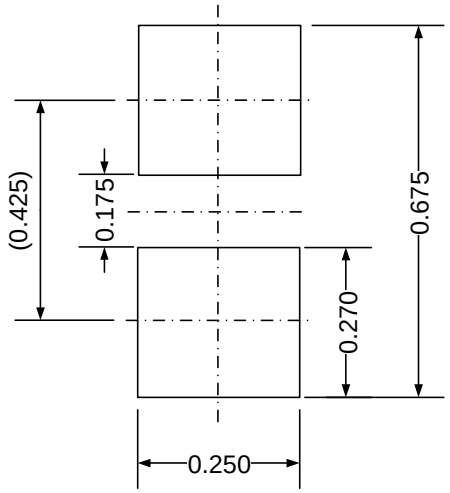
Package



Unit: mm

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	0.235	0.250	0.265
A1	Standoff	0.000	0.010	0.050
b	Terminal Width	0.200	0.220	0.240
D	Body Length	0.580	0.600	0.620
E	Body Width	0.280	0.300	0.320
e	Pitch		0.355 BSC	
L	-	0.140	0.160	0.180
aaa	Coplanarity		0.08	

Land Pattern



(Note)
Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjusts the Land Pattern at your own risk.

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

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