

# THTVS514

## Transient Voltage Suppressor for I/O Protection

### General Description

THTVS514 4ch TVS arrays are ultra-low capacitance ESD protection devices designed to protect sensitive or high speed I/O. THine THTVS series has been specifically designed to protect sensitive components which are connected to digital transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

THTVS514 has a 0.3pF(typ) small capacitance between I/O pins. ESD are highlighted by high ESD withstand voltage (Contact  $\pm 12\text{kV}$  per IEC 61000-4-2), It will protect four lines operating at 5.5V( $V_{\text{rwm}}$ ). THTVS514 is in a 2.5 x 1.0 x 0.55mm 10-Lead standard package and flow- through pin layout for easy and simple PCB design.

The THTVS514 four-channel TVS is for sensitive or high speed I/O which designed to protect ASIC, FPGA, SoC, ASSP, LVDS, PECL, CML digital I/O and HDMI, Display port, USB3.0 high speed standard I/O.

They may be used to meet the ESD immunity requirements of IEC 61000- 4-2/4/5.

The THTVS514 protects four single-end lines or two differential lines.

### Features

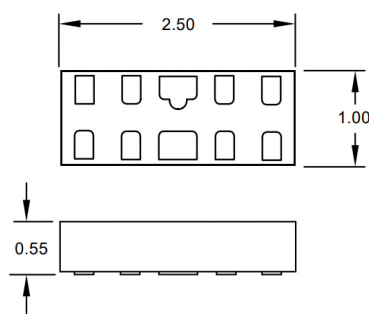
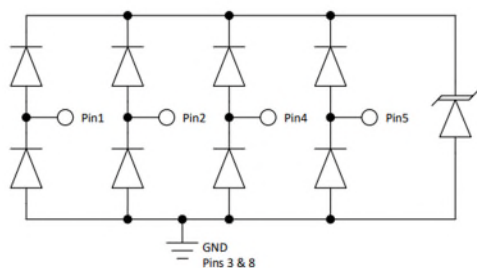
- ESD protection for high-speed data lines to IEC61000-4-2(ESD)  $\pm 17\text{kV}$  (air),  $\pm 12\text{kV}$  (contact)
- IEC61000-4-4(EFT) 40A (5/50ns)
- IEC61000-4-5(Surge) 6A (8/20 $\mu\text{s}$ )
- Protect four high speed lines
- Flow-through pin configuration
- Low capacitance: 0.3pF typ (I/O to I/O)
- Low dynamic resistance: 0.19 Ohm typ
- Operating voltage:  $V_{\text{rwm}}$  5.5V
- 10 pin standard package (2.5 x 1.0 x 0.55mm)
- Packaging: Tape and Reel

### Applications

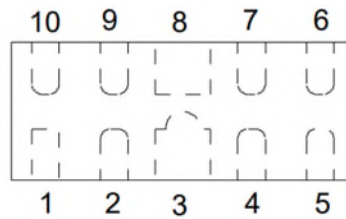
Applications for sensitive and high speed I/O protection as followed.

- FPGA/SoC/ASSP high speed I/O.
- CML/PECL/LVDS physical layer
- HDMI/DVI/DisplayPort<sup>TM</sup>
- PCIExpress /eSATA
- USB3.0/3.1
- V-by-One<sup>®</sup> HS
- Sensitive Sensor I/O
- Connector and cable I/F

### Schematic and Package Dimension



## Pin Configuration



THTVS514 package pin configuration (Top view)

## Pin Description

Pin No	Type	Description
1	I	Input
2	I	Input
3, 8	GND <sup>*1</sup>	Ground. Must be tied to the PCB ground plane
4	I	Input
5	I	Input
6, 7, 9, 10	NC	No internal connection

\*1: Low impedance connection to Ground required.

## Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Peak Pulse Current (tp = 8/20µs)	I <sub>PP</sub>	6	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup>	V <sub>ESD</sub>	+/- 17	kV
ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>		+/- 12	
Operating Junction Temperature	T <sub>J</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

Notes:

(1) ESD gun return path connected to Ground Reference Plane (GRP)

**Electrical Characteristics (T<sub>j</sub> = 25 °C)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V <sub>RWM</sub>	I/O pin to ground	-	-	5.5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA I/O pin to ground	6	-	-	V
Clamping Voltage	V <sub>C</sub>	I <sub>pp</sub> = 1A tp = 8/20µs Any I/O pin to GND	-	-	15	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5.5V	-	-	0.1	µA
ESD Clamping Voltage <sup>(2)</sup>	V <sub>C</sub>	I <sub>pp</sub> = 4A tp = 0.2/100ns (TLP) Any I/O pin to GND	-	10.8	-	V
		I <sub>pp</sub> = 16A tp = 0.2/100ns (TLP) Any I/O pin to GND	-	13.0	-	
Dynamic Resistance <sup>(2)(3)</sup>	R <sub>DYN</sub>	tp = 0.2/100ns (TLP)	-	0.19	-	Ω
Junction Capacitance	C <sub>j</sub>	V <sub>R</sub> = 0V, f = 1MHz I/O Pins to ground	-	-	0.8	pF
		V <sub>R</sub> = 0V, f = 1MHz between I/O pins	-	0.3	0.4	

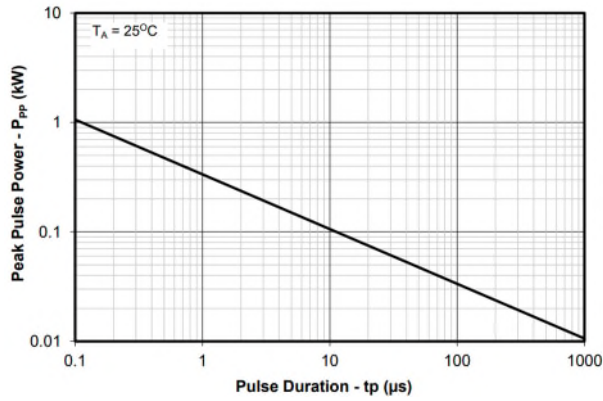
Notes:

(2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I<sub>TLP</sub> and V<sub>TLP</sub> averaging window: t1 = 70ns to t2 = 90ns.

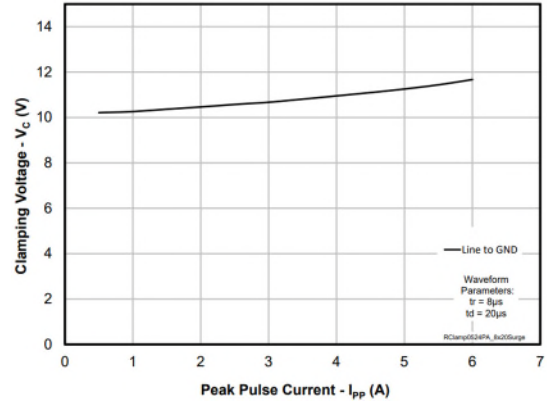
(3) Dynamic resistance calculated from I<sub>TLP</sub> = 4A to I<sub>TLP</sub> = 16A

## Typical Characteristics

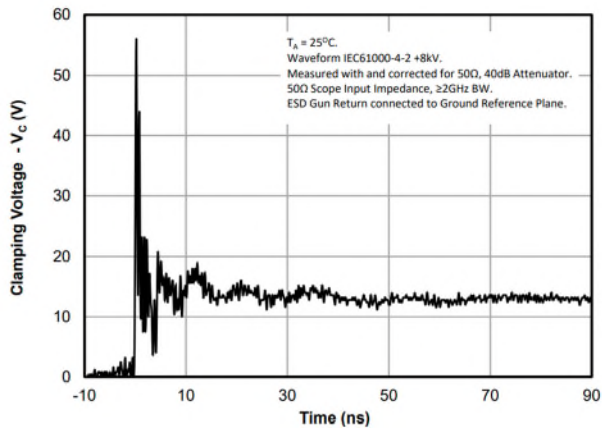
**Non-Repetitive Peak Pulse Power vs. Pulse Time**



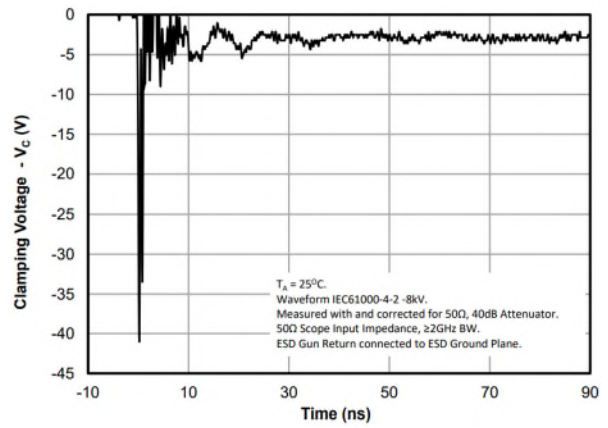
**8/20us Surge Clamping Characteristic**



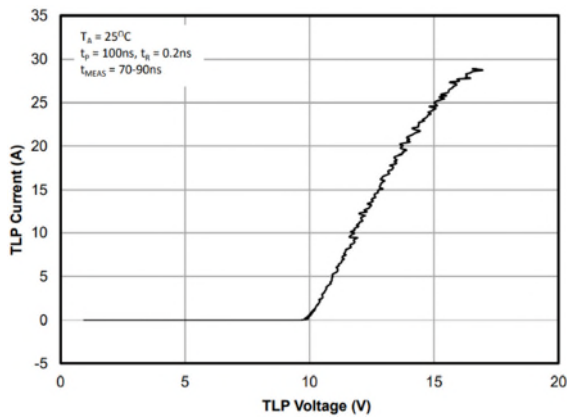
**ESD Clamping (8kV Contact per IEC 61000-4-2)**



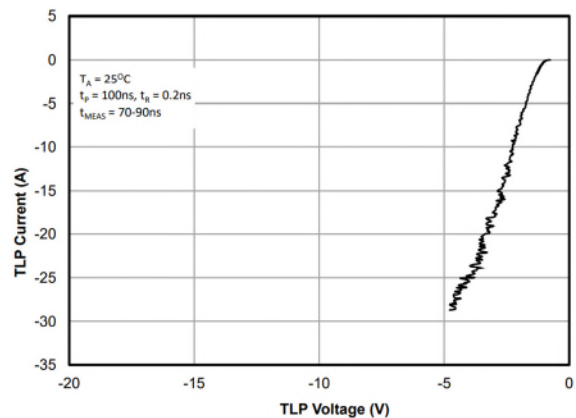
**ESD Clamping (-8kV Contact per IEC 61000-4-2)**



**TLP Characteristic (Positive Pulse)**

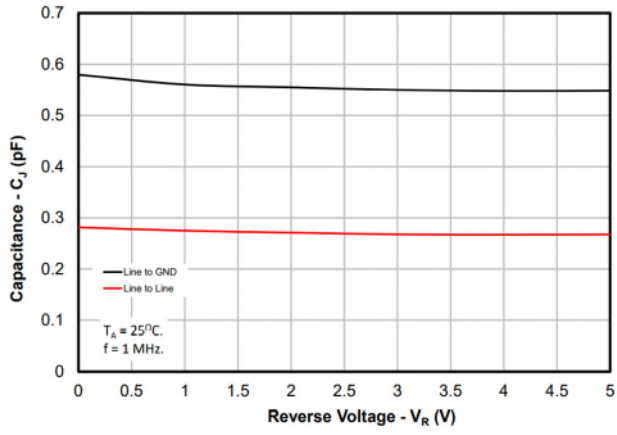


**TLP Characteristic (Negative Pulse)**

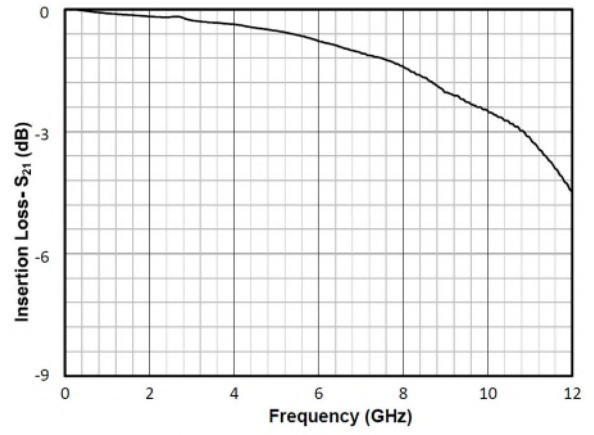


## Typical Characteristics

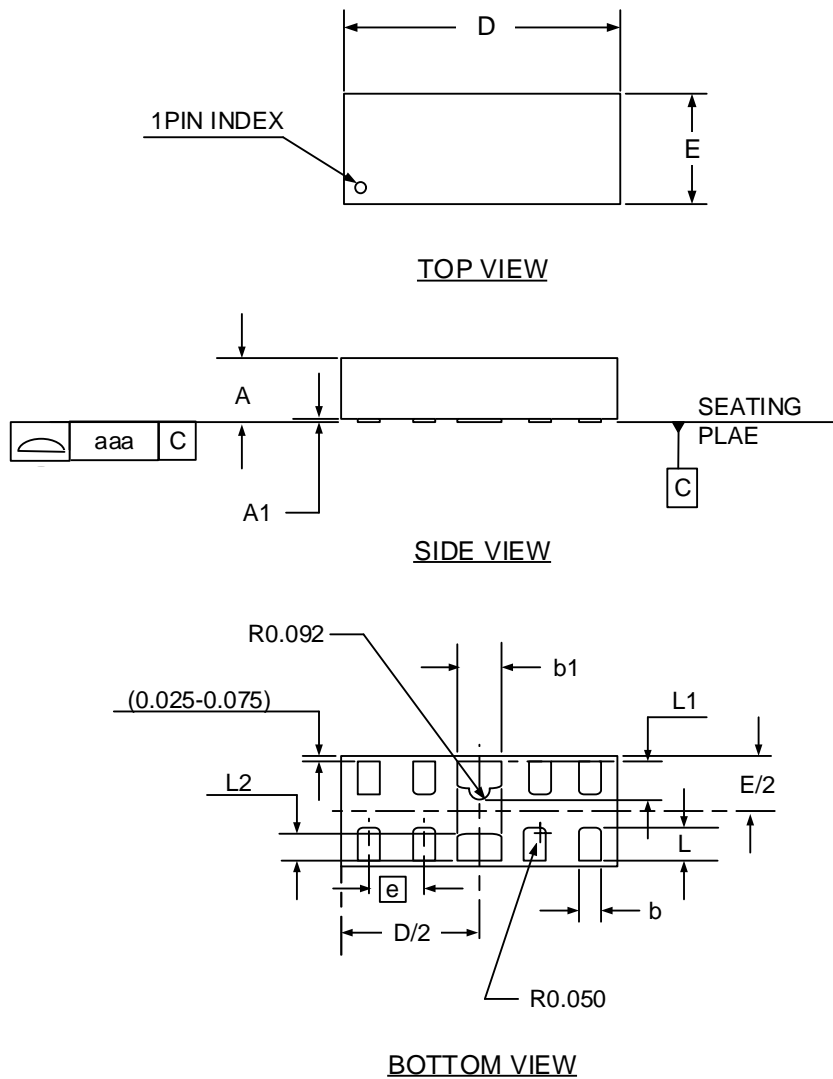
### Capacitance vs. Reverse Voltage



### Insertion Loss (Line to GND)



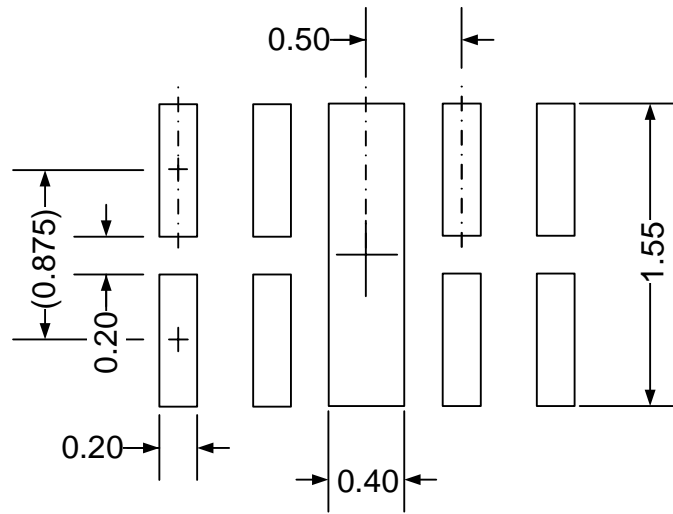
Package



Unit: mm

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	0.50	0.55	0.60
A1	Standoff	0.00	0.03	0.05
b	-	0.15	0.20	0.25
b1	-	0.35	0.40	0.45
D	Body Length	2.45	2.50	2.575
E	Body Width	0.95	1.00	1.075
e	Pitch	0.50 BSC		
L	-	0.25	0.30	0.35
L1	-	0.30	0.35	0.40
L2	-	0.194	0.244	0.294
aaa	Coplanarity	0.08		

Land Pattern



Note:

Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjusts the Land Pattern at your own risk.

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