

THTVS312

Transient Voltage Suppressor for I/O Protection

General Description

THTVS312 provides ESD protection to IEC6100-4-2 on digital I/O. The devices “snap-back” to a low on-state voltage when the breakdown voltage of the device is exceeded. This has the advantage of lowering the overall ESD clamping voltage. When the device is in the on-state, the dynamic resistance is 0.3 Ohms (typ), further minimizing the ESD clamping. Maximum capacitance is 0.4pF extremely small which allowing to be used in applications operating in 6GHz with signal integrity. It will be protected two single-end signals or a differential signal operating at 3.6V (V_{rwm}).

The combination of low peak ESD clamping, low dynamic resistance, and low capacitance makes this device suitable for digital signal and high speed applications such as LVDS, USB3.0/3.1, PECL, V-by-One[®] HS and general CML interfaces

Features

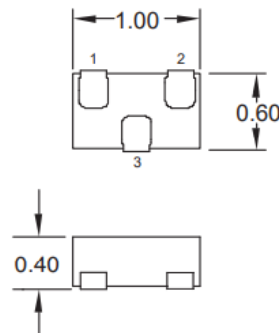
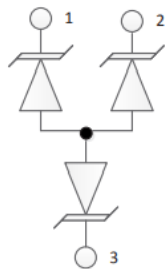
- ESD protection IEC 61000-4-2(ESD) ±20kV(air), ±17kV(contact)
- Protects two I/Os or a differential I/O
- Low capacitance: 0.3pF typ
- Low dynamic resistance: 0.3 Ohm typ
- Operating voltage: V_{rwm} 3.6V
- Three pin package (1.0 x 0.6 x 0.4 mm)
- Easy to mount package for two line
- Packaging: Tape and Reel

Applications

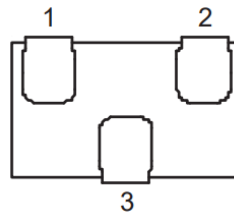
Applications for sensitive and high speed I/O protection as followed.

- FPGA/SoC/ASSP high speed I/O.
- CML/PECL/LVDS physical layer
- HDMI/DVI/DisplayPort[™]
- PCIExpress /eSATA
- USB3.0/3.1
- V-by-One[®] HS
- Sensitive Sensor I/O
- Connector and cable I/F

Schematic and Package Dimension



Pin Configuration



THTVS312 package pin configuration (Bottom view)

Pin Description

Pin No	Type	Description
1	I	Input or Ground* ¹ One of three pins is assigned to Ground
2	I	Input or Ground* ¹
3	I	Input or Ground* ¹

*¹ Low impedance connection to Ground required.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Peak Pulse Current (tp = 8/20μs)	I _{PP}	4	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	+/- 20	kV
ESD per IEC 61000-4-2 (Contact)		+/- 17	
Operating Junction Temperature	T _J	-40 to +125	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T_j = 25 °C)

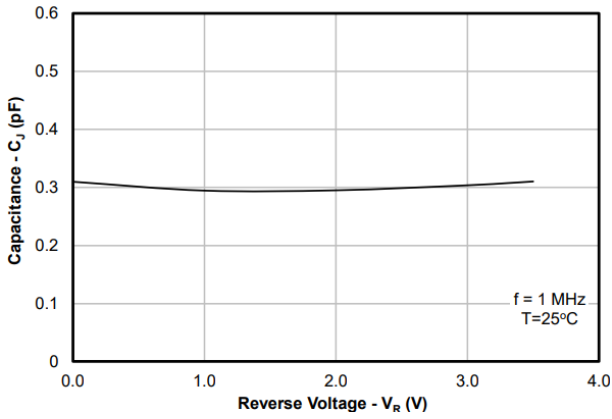
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V _{RWM}	Pin 1 or 2 to Pin3	-	-	3.6	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 10uA Pin 1 or 2 to Pin3	7.5	8.8	9.8	V
Reverse Leakage Current	I _R	V _{RWM} = 3.6V, Pin 1 or 2 to Pin3	-	0.01	0.05	μA
Clamping Voltage t _p = 8/20μs	V _C	I _{pp} = 1A, Pin 1 or 2 to Pin3	-	3.5	5	V
		I _{pp} = 4A, Pin 1 or 2 to Pin3	-	5	6.5	
I _{pp} = 16A, Pin 1 or 2 to Pin3		-	9.5	-		
I _{pp} = -16A, Pin 1 or 2 to Pin3		-	-9.5	-		
Dynamic Resistance (Positive)	R _{DYN}	t _p = 0.2/100ns Pin 1 or 2 to Pin3	-	0.30	-	Ω
Dynamic Resistance (Negative)		t _p = 0.2/100ns Pin 1 or 2 to Pin3	-	0.30	-	
Junction Capacitance	C _j	V _R = 0V, f = 1MHz, Pin 1 or 2 to Pin3	-	0.30	0.40	pF

Notes

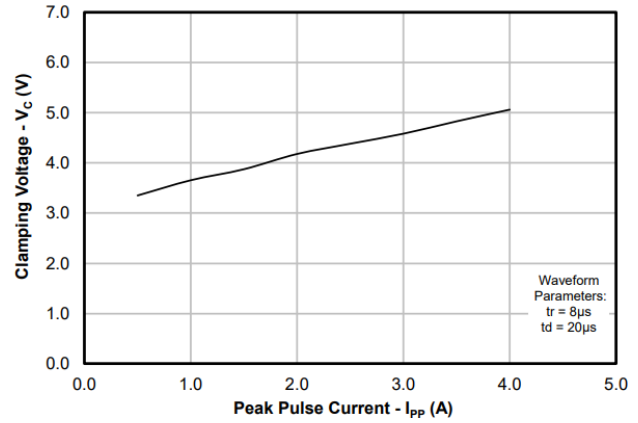
- 1) ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings: t_p = 100ns, t_r = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns.
- 3) Dynamic resistance calculated from ITLP = 4A to ITLP = 16A

Typical Characteristics

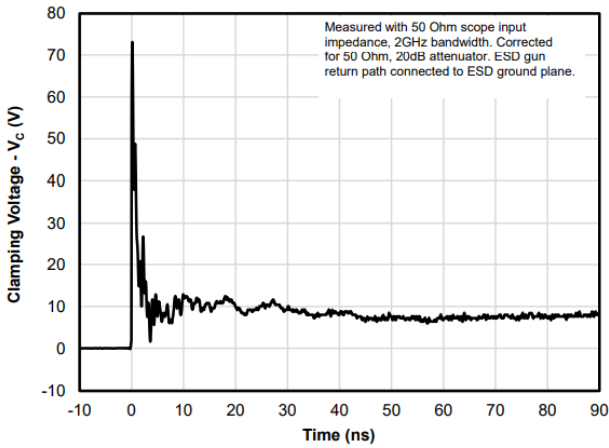
Junction Capacitance



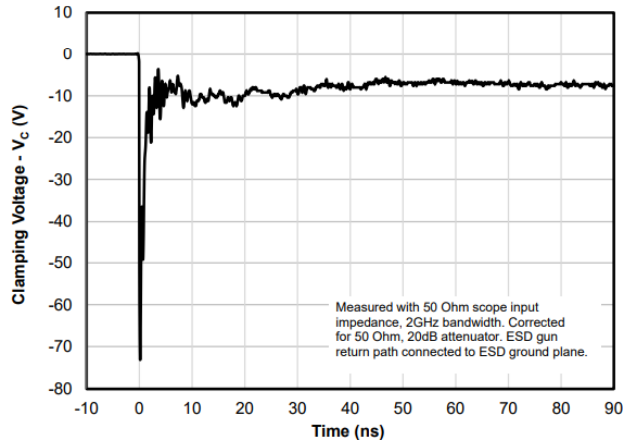
Positive Surge Clamping Voltage (8/20μs)
(Between any I/O and Ground)



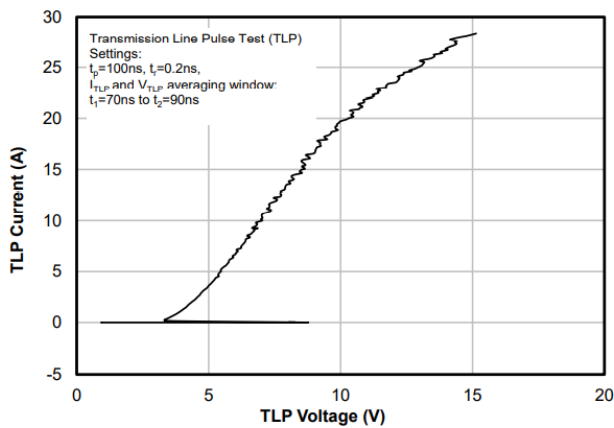
ESD Clamping (+8kV Contact per IEC 61000-4-2)
(Between any I/O and Ground)



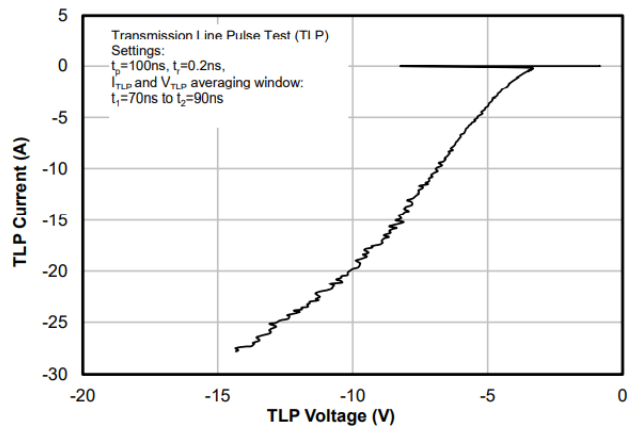
ESD Clamping (-8kV Contact per IEC 61000-4-2)
(Between any I/O and Ground)



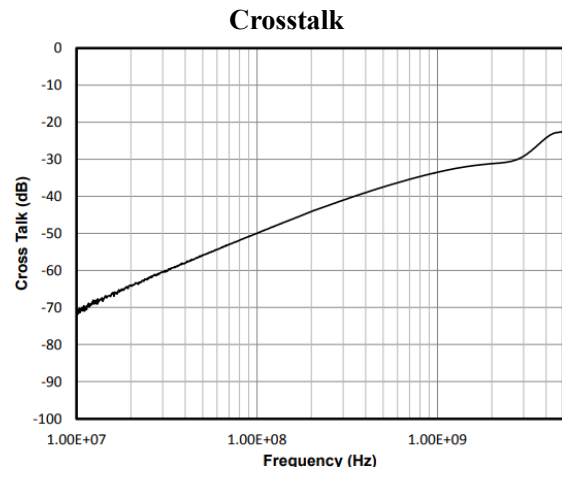
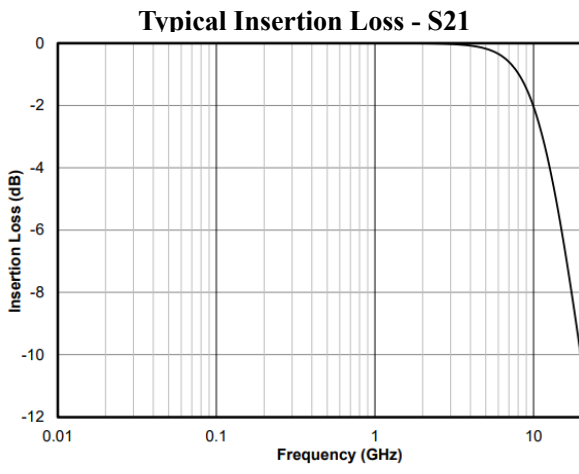
Positive TLP Clamping Voltage
(tperiod=100ns, tr=0.2ns)



Negative TLP Clamping Voltage
(tperiod=100ns, tr=0.2ns)



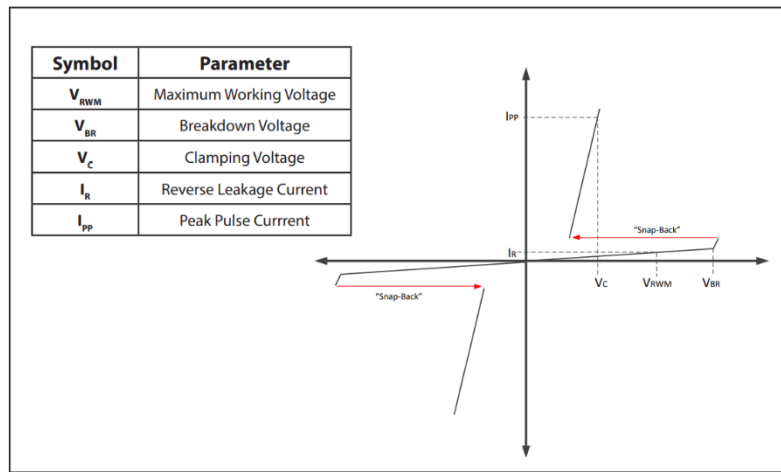
Typical Characteristics



Application Information

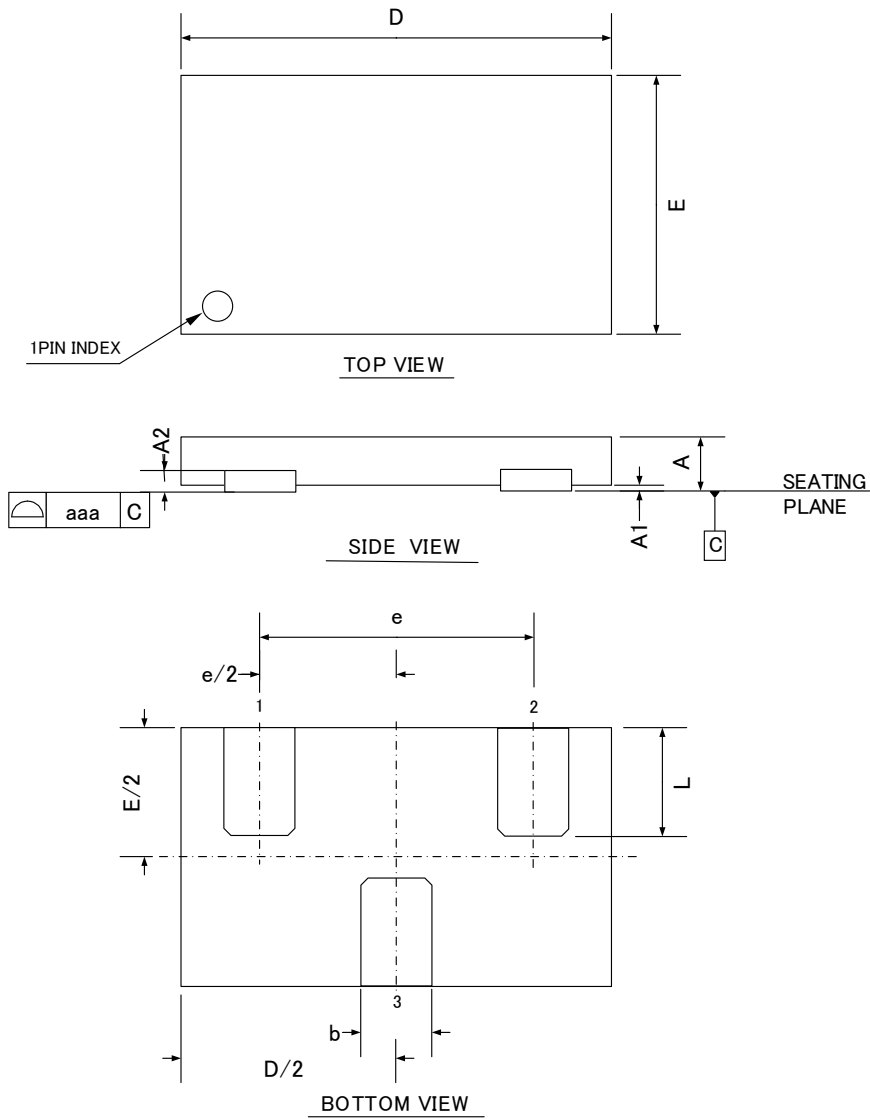
Device Operation

This device utilizes a multi-junction structure that is designed to switch to a low voltage state when triggered by ESD, EOS, or other transient events. During normal operation, the device will present a high impedance to the circuit for voltage up to the working voltage (V_{RWM}) of the device. When the voltage across the device terminals exceeds the breakdown voltage (V_{BR}), avalanche breakdown occurs in the blocking junction causing the device to “snap-back” or switch to a low impedance on-state. This has the advantage of lowering the overall clamping voltage (V_C) as ESD peak pulse current (I_{PP}) flows through the device. Once the current subsides, the device will return to a high impedance off-state. Since this device is bidirectional, it will behave the same way for positive or negative polarity transient events



Characteristic Curve

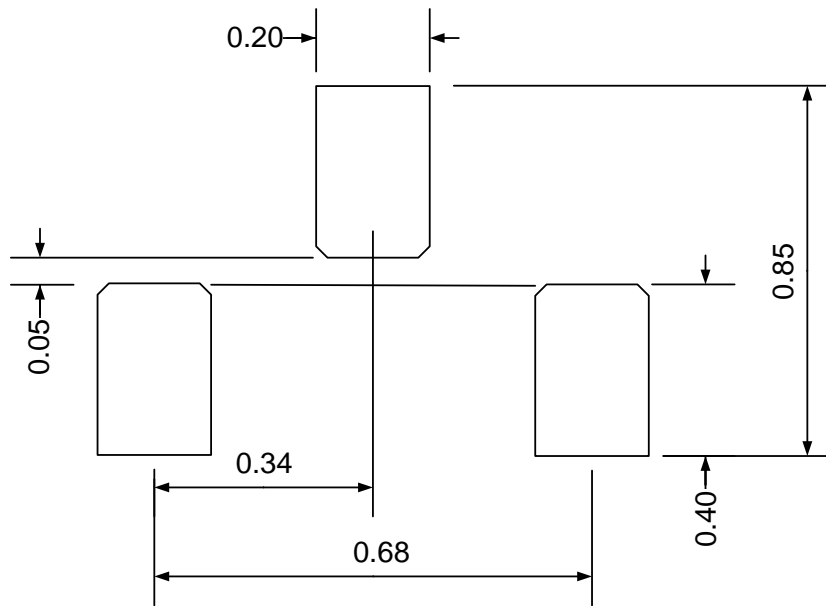
Package



Unit : mm

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	0.37	0.40	0.43
A1	Standoff	0.00	0.02	0.05
A2	-	(0.13)		
b	Terminal Width	0.175	0.20	0.225
D	Body Length	0.90	1.00	1.10
E	Body Width	0.50	0.60	0.70
e	Pitch	0.68 BSC		
L	Length	0.225	0.25	0.275
aaa	Coplanarity	0.08		

Land Pattern



(Note)

Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjust the Land Pattern at your own risk.

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.
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