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<i>Application Note</i>
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<i>THCV242A_RegisterMap_Rev4.05_E</i>
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# **THCV242A/THCV242A-P/THCV242A-Q**

## **Register Map**

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## Register Map

THCV242A/THCV242A-P/THCV242A-Q registers outline

Address	comment
0x0000 - 0x010F	Sub-Link and 2-wire serial I/F registers
0x1000 - 0x100F	GPIO/ERR/INT pin registers
0x1010 - 0x103F	Main-Link registers
0x1100 - 0x110C	Pre-processing registers
0x1200 - 0x120C	
0x1500 - 0x1505	Data Stream Handling registers
0x1600 - 0x161F	MIPI CSI-2 output registers
0x1700 - 0x170F	Software reset and power down registers
0x1710 - 0x173F	Interrupt registers
0x1740 - 0x175F	Other registers (read only registers, etc)
other	Reserved

## Sub-Link and 2-wire serial I/F registers

Address	bit	Register Name	width	R/W	Init	Description
0x0000	[7:0]	reserved	8	-	-	-
0x0001	[7:1]	reserved	7	-	-	-
	[0]	R_SLINK_RST	1	W	-	Sub-Link Soft Reset 0x1: Reset 0x0001[0] Sub-Link reset does not includes 2-wire slave controller so that 0x0001[0] reset write access does not cause 2-wire slave abort and reaction to 2-wire master is normal ACK. Function is a little different from 0x1701[1].
0x0002	[7:0]	reserved	8	-	-	-
0x0003	[7:0]	reserved	8	-	-	-
0x0004	[7:3]	reserved	5	-	-	-
	[2:0]	R_SLINK_MODE	3	RW	3'h1	Sub-Link basic protocol setting as Sub-Link Master 0x1: 2-wire Set & Trigger mode1 0x3: 2-wire Pass Through mode1 Other: Reserved
0x0005	[7:0]	reserved	8	-	-	-
0x0006	[7:0]	reserved	8	-	-	-
0x0007	[7:0]	reserved	8	-	-	-
0x0008	[7:1]	reserved	7	-	-	-
	[0]	R_CKSUM_EN	1	RW	1'h0	Internal Register AutoCheckSum Enable 0x0: Disable 0x1: Enable
0x0009	[7:0]	R_CKSUM_TIM	8	RW	8'h13	<this registers is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum check interval =1024x64x(R_CKSUM_TIM<7:0>+1) x tOSC
0x000A	[7:0]	R_CKSUM_VAL	8	RW	8'h00	<this registers is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum expected target value
0x000B	[7:0]	R_CKSUM_RVAL	8	R	-	<this registers is valid only when 0x0008[0]=0x1> Internal Register AutoCheckSum read value
0x000C	[7:0]	reserved	8	-	-	-
0x000D	[7:0]	reserved	8	-	-	-
0x000E	[7:0]	reserved	8	-	-	-
0x000F	[7:0]	reserved	8	-	-	-
0x0010	[7:4]	R_SLINK_EN	4	RW	4'h0	Sub-Link Enable (*each bit setting) [7] ReservedL (must be set 0x0) [6] ReservedL (must be set 0x0) [5] Sub-Link Enable for Lane1 (*) [4] Sub-Link Enable for Lane0 (*) 0x0: Sub-Link Disable 0x1: Sub-Link Enable
	[3:0]	R_SLINK_POL_EN	4	RW	4'hF	Sub-Link Polling Enable (*each bit setting) [3] ReservedL (must be set 0x0) [2] ReservedL (must be set 0x0) [1] Sub-Link Polling Enable for Lane1 (*) [0] Sub-Link Polling Enable for Lane0 (*) 0x0: Polling Disable 0x1: Polling Enable
0x0011	[7:4]	reservedX	4	RW	4'hF	must be left 0xF (default setting)
	[3:0]	R_SLINK_WD_EN	4	RW	4'hF	Sub-Link Watch Dog Timer (WDT) Enable (*each bit setting) [3] ReservedL (must be set 0x0) [2] ReservedL (must be set 0x0) [1] Sub-Link WDT Enable for Lane1 (*) [0] Sub-Link WDT Enable for Lane0 (*) 0x0: WDT Disable 0x1: WDT Enable
0x0012	[7:0]	reserved	8	-	-	-
0x0013	[7:0]	reserved	8	-	-	-
0x0014	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0015	[7:5]	reserved	3	-	-	-
	[4]	R_SLINK_PHASE_EN	1	RW	1'h0	Enable of shifting the Sub-Link 2WIRE output timing 0x0: Disable 0x1: Enable The 2WIRE output timing of Sub-Link Lane1 is delayed by 4xtOSC from Lane0.
	[3:1]	reserved	3	-	-	-
	[0]	R_SLINK_POL_COPY_EN	1	RW	1'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Sub-Link Polling Copy Distribution 0x0: Disable Inputted data from GPIO0, GPIO1 are sent via Sub-Link Lane0. Inputted data from GPIO2, GPIO3 are sent via Sub-Link Lane1. 0x1: Enable Inputted data from GPIO0, GPIO1 are copied and sent via all Sub-Link lanes
0x0016	[7:6]	reserved	2	-	-	-
	[5:4]	R_POL_TIM_CLR_EN	2	RW	2'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Polling Timer Clear/Mask setting 0x1: The polling timer is cleared when the inputted GPIO changes 0x2: The polling timer masked when inputted GPIO signal is high, and the polling transmission is outputted after inputted GPIO signal is falling.
	[3]	reserved	1	-	-	-
0x0017	[2:0]	R_GPI_TRG_SEL	3	RW	3'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Polling Timer Clear/Mask GPIO signal select 0x0: GPIO0 (this setting is valid only when 0x1004[3:0]=0x3) 0x1: GPIO1 (this setting is valid only when 0x1004[7:4]=0x3) Other: Reserved
	[7:6]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[5:4]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[3:2]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
0x0018	[1:0]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[7:6]	R_RES_GP3_LN_SEL	2	RW	2'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> <this register is valid only when 0x1003[7:4]=0x4> Select the Source Sub-Link lane when GPIO3 is as Through GPO mode. 0x0: Sub-Link Lane0 0x1: Sub-Link Lane1 other: Reserved
	[5:4]	R_RES_GP2_LN_SEL	2	RW	2'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> <this register is valid only when 0x1003[3:0]=0x4> Select the Source Sub-Link lane when GPIO2 is as Through GPO mode. 0x0: Sub-Link Lane0 0x1: Sub-Link Lane1 Other: Reserved
	[3:2]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
0x0019	[1:0]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[7:4]	ReservedL	4	RW	4'h0	must be left 0x0 (default setting)
	[3:2]	R_LOCKN_LN1_SEL	2	RW	2'h0	<This register is valid when 0x0010[3:0]=0x1, 0x2 or 0x3> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane1 0x0: LOCKN0 and HTPDN0 (*1)(*2) 0x1: "LOCKN0   LOCKN1" and "HTPDN0   HTPDN1" (*3)(*4)(*5) 0x2: Reserved 0x3: Always LOW as LOCKN and always LOW as HTPDN  (*1) LOCKN0: LOCKN signal of V-by-One(R) HS Lane0 (RX0P/RX0N) (*2) HTPDN0: HTPDN signal of V-by-One(R) HS Lane0 (RX0P/RX0N) (*3) LOCKN1: LOCKN signal of V-by-One(R) HS Lane1 (RX1P/RX1N) (*4) HTPDN1: HTPDN signal of V-by-One(R) HS Lane1 (RX1P/RX1N) (*5) The symbol " " means logical OR.
	[1:0]	R_LOCKN_LN0_SEL	2	RW	2'h0	<This register is valid when 0x0010[3:0]=0x1, 0x2 or 0x3> Select the source signal to be transmitted as LOCKN and HTPDN via Sub-Link Lane0 0x0: LOCKN0 and HTPDN0 (*1)(*2) 0x1: "LOCKN0   LOCKN1" and "HTPDN0   HTPDN1" (*3)(*4)(*5) 0x2: Reserved 0x3: Always LOW as LOCKN and always LOW as HTPDN Should be set 0x01 when V-by-One(R) HS 2lane mode (0x1501[4:0]=0x08)  (*1) LOCKN0: LOCKN signal of V-by-One(R) HS Lane0 (RX0P/RX0N) (*2) HTPDN0: HTPDN signal of V-by-One(R) HS Lane0 (RX0P/RX0N) (*3) LOCKN1: LOCKN signal of V-by-One(R) HS Lane1 (RX1P/RX1N) (*4) HTPDN1: HTPDN signal of V-by-One(R) HS Lane1 (RX1P/RX1N) (*5) The symbol " " means logical OR.

Address	bit	Register Name	width	R/W	Init	Description
0x001A	[7:5]	reserved	3	-	-	-
	[4]	R_SLINK_POL_OFSET_EN	1	RW	1'h0	<this regiseter is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Enable of shifting the Sub-Link Polling output timing 0x0: Disable 0x1: Enable The Polling output timing of Sub-Link Lane1 is delayed by Sub-Link Polling interval x 1/4 from the Sub-Link Lane0.
	[3:2]	reserved	2	-	-	-
	[1:0]	R_SLINK_POL_TIM_UP	2	RW	2'h0	<this regiseter is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Sub-Link Polling interval setting (min. 0x018, about 20us)
0x001B	[7:0]	R_SLINK_POL_TIM_DN	8	RW	8'h7C	<this regiseter is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> Sub-Link Polling interval time=64x(256xR_SLINK_POL_TIM_UP<1:0> +R_SLINK_POL_TIM_DN<7:0>+1)xTOSC *No Polling when R_SLINK_POL_TIM_UP=0x0 and R_SLINK_POL_TIM_DN=0x0
0x001C	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_SSR_TIM_UP	2	RW	2'h0	Sub-Link SSR interval setting
0x001D	[7:0]	R_SLINK_SSR_TIM_DN	8	RW	8'hF9	Sub-Link SSR interval time=64x(256xR_SLINK_SSR_TIM_UP<1:0> +R_SLINK_SSR_TIM_DN<7:0>+1)xTOSC *No SSR when R_SLINK_SSR_TIM_UP=0x0 and R_SLINK_SSR_TIM_DN=0x0
0x001E	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_WD_TIM_UP	2	RW	2'h0	<this regiseter is valid when 0x0011[3:0]=0x1 or 0x2 or 0x3> Sub-Link Watch Dog Timer (WDT) time parameter
0x001F	[7:0]	R_SLINK_WD_TIM_DN	8	RW	8'hBB	<this regiseter is valid when 0x0011[3:0]=0x1 or 0x2 or 0x3> Sub-Link WDT time =64x(256xR_SLINK_WD_TIM_UP<1:0> +R_SLINK_WD_TIM_DN<7:0>+1)xTOSC

Address	bit	Register Name	width	R/W	Init	Description
0x0020	[7:5]	reserved	3	-	-	-
	[4]	R_VS_PHASE_EN	1	RW	1'h0	<this register is valid only when 0x0020[1:0]=0x2> Enable of shifting the Internal VSYNC output timing 0x0: Disable 0x1: Enable (*) (*) 0x002E register is related for output timing
	[3:2]	reserved	2	-	-	-
	[1:0]	R_VS_MODE	2	RW	2'h0	<this register is valid when 0x0010[3:0]=0x1 or 0x2 or 0x3> multiple camera synchronization Frame VSYNC supply mode setting 0x1: Select external VSYNC signal from EXTSYNC pin (*) 0x2: Select internal VSYNC signal and output for EXTSYNC pin (**) Other: Disable (*) 0x1007 register is related to this mode (**) set this mode after setting both 0x0021 and 0x0023 - 0x002E registers
0x0021	[7:5]	reserved	3	-	-	-
	[4]	ReservedL	1	RW	1'h0	must be left 0x0 (default setting)
	[3:1]	reserved	3	-	-	-
	[0]	R_VS_POL	1	RW	1'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC Pulse Polarity 0x0: Low Pulse 0x1: High Pulse
0x0022	[7]	reserved	1	-	-	-
	[6:4]	R_VS_GPI_SEL	3	RW	3'h0	<this register is valid when 0x0020[1:0]=0x1 or 0x2> Select a assignment bit for Frame VSYNC signal to send 0x0: a bit of Sub-Link for GPIO0 0x1: a bit of Sub-Link for GPIO1 Other: Reserved
	[3:2]	ReservedL	2	RW	2'h0	Must be set 0x0
	[1:0]	R_VS_LANE_SEL	2	RW	2'h0	<this register is valid when 0x0020[1:0]=0x1 or 0x2> Select Sub-Link Lane for Frame VSYNC signal to send (* each bit setting) [0]:Sub-Link Lane0 (*) [1]:Sub-Link Lane1 (*) 0x0: no send 0x1: send Frame VSYNC signal
0x0023	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_LINE_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by oscillator setting
0x0024	[7:0]	R_VSOSC_LINE_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by oscillator = (256xR_VSOSC_LINE_UP<3:0> +R_VSOSC_LINE_DN<7:0>+1)xOSC *Clock / line is 1 when R_VSOSC_LINE_UP=0x0 and R_VSOSC_LINE_DN=0x0
0x0025	[7:0]	R_VSOSC_WIDTH	8	RW	8'h00	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse width line number by oscillator setting Line Number = R_VSOSC_WIDTH + 1 (e.g. 0x00 for 1line)
0x0026	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_TIM_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number by oscillator setting
0x0027	[7:0]	R_VSOSC_TIM_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number by oscillator = (256xR_VSOSC_TIM_UP<3:0> +R_VSOSC_TIM_DN<7:0>+1)xOSC *Interval line is 2 when R_VSOSC_TIM_UP=0x0 and R_VSOSC_TIM_DN=0x0

Address	bit	Register Name	width	R/W	Init	Description
0x0028	[7:2]	reserved	6	-	-	-
	[1:0]	R_VS_PCLK_SEL	2	RW	2'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC generation base pixel clock domain select 0x0: select source clock (CLK_I) from Main-Link Lane0 0x1: select source clock (CLK_I) from Main-Link Lane1 Other: Reserved
0x0029	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_LINE_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by base pixel clock setting
0x002A	[7:0]	R_VSP_LINE_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC clock number / line by base pixel clock = (256x R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)×CLK_I *Clock / line is 1 when R_VSP_LINE_UP=0x0 and R_VSP_LINE_DN=0x0
0x002B	[7:0]	R_VSP_WIDTH	8	RW	8'h04	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse width line number by base pixel clock setting Line Number = R_VSP_WIDTH + 1 (e.g. 0x00 for 1line)
0x002C	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_TIM_UP	4	RW	4'h0	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number setting
0x002D	[7:0]	R_VSP_TIM_DN	8	RW	8'h0F	<this register is valid only when 0x0020[1:0]=0x2> Internal VSYNC pulse interval line number = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) Internal VSYNC pulse interval frame period by base pixel clock = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+0x1)× (256×R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+0x1)×CLK_I *Interval line is 2 when R_VSP_TIM_UP=0x0 and R_VSP_TIM_DN=0x0 *For setting or reset of this register, R_VS_MODE is supposed to be disable
0x002E	[7:0]	R_VS_PHASE_WIDTH	8	RW	8'h01	<this register is valid only when 0x0020[1:0]=0x2> The internal VSYNC output timing of Sub-Link Lane1 is delayed by "16 × R_VS_PHASE_WIDTH × CLK_I" from Sub-Link Lane0. (e.g. 0x00 is 16×CLK_I)
0x002F	[7:0]	reserved	8	-	-	-



Address	bit	Register Name	width	R/W	Init	Description
0x0030	[7:0]	R_2WIRE_SADR	8	RW	8'h00	2-wire slave device address setting [7] 2-wire slave device address control 0x0: 2-wire slave device addr. is set by AIN1 and AIN0 pin 0x1: 2-wire slave device addr. is set by following register [6:0]  <this register is valid when 0x0030[1:0]=0x1> [6:0] 2-wire slave device address value for register control
0x0031	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIREPT_MODE	2	RW	2'h0	<this register is valid only when 0x0004[2:0]=0x3> Sub-Link 2WIRE Pass Through mode setting  [1]Pass Through processing protocol on Sub-Link Slave 0x0: Reserved 0x1: Divided Write & Divided Read Transaction address and data Byte number are set as R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE.  [0]Pass Through 2WIRE device address processing 0x0: Address rename (rule as R_2WIREPT1_PASS_ADDRxy0/1. x is Lane0 or Lane1, y=<3:0>) 0x1: All Through (exception definition of address to ignore as R_2WIREPT2_NOPASS_ADDRz. x is Lane0 or Lane1, z=<7:0>)
0x0032	[7]	reserved	1	-	-	-
	[6:4]	R_2WIREPT_WA_BYTE	3	RW	3'h0	<this register is valid only when 0x0031[1]=0x1> Sub-Link 2WIRE Pass Through Divided Write/Read Sub Address (Word Address) Byte number setting Byte Number = R_2WIREPT_WA_BYTE + 1 0x0: 1Byte (= 8bit) sub address 0x1: 2Byte (=16bit) sub address Other: Reserved
	[3:0]	R_2WIREPT_DATA_BYTE	4	RW	4'h0	Sub-Link 2WIRE Pass Through Divided Write/Read data Byte number per a transaction setting, Byte Number = R_2WIREPT_DATA_BYTE + 1 (e.g. 0x2 for 3Byte per a transaction) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < d14 is required.
0x0033	[7:0]	reserved	8	-	-	-
0x0034	[7:0]	reserved	8	-	-	-
0x0035	[7:0]	reserved	8	-	-	-
0x0036	[7:0]	reserved	8	-	-	-
0x0037	[7:0]	reserved	8	-	-	-
0x0038	[7:0]	reserved	8	-	-	-
0x0039	[7:0]	reserved	8	-	-	-
0x003A	[7:0]	reserved	8	-	-	-
0x003B	[7:5]	reserved	3	-	-	-
	[4]	R_2WIRE_WD_EN	1	RW	1'h1	2-wire I/F Watch Dog Timer (WDT) Enable 0x0: Disable 0x1: Enable
	[3:1]	reserved	3	-	-	-
	[0]	R_2WIRE_WD_OFFSET	1	RW	1'h1	<this register is valid only when 0x003B[4]=0x1> 2-wire I/F WDT Offset Time 0x1: 0x7FF (=d2047) 0x0: 0x3FF (=d1023)
0x003C	[7:0]	R_2WIRE_WD_TIM	8	RW	8'hFF	<this register is valid only when 0x003B[4]=0x1> 2-wire I/F WDT time =64x{(R_2WIRE_WD_TIM<7:0>+1)}x{2WIRE_WDT_OffsetTime}xtOSC
0x003D	[7:0]	reserved	8	-	-	-
0x003E	[7:0]	reserved	8	-	-	-
0x003F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0040	[7:0]	R_2WIREPT1_PASS_ADR000	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #0
0x0041	[7:0]	R_2WIREPT1_PASS_ADR001	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #0
0x0042	[7:0]	R_2WIREPT1_PASS_ADR010	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #1
0x0043	[7:0]	R_2WIREPT1_PASS_ADR011	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #1
0x0044	[7:0]	R_2WIREPT1_PASS_ADR020	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #2
0x0045	[7:0]	R_2WIREPT1_PASS_ADR021	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #2
0x0046	[7:0]	R_2WIREPT1_PASS_ADR030	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane0 #3
0x0047	[7:0]	R_2WIREPT1_PASS_ADR031	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane0 #3
0x0048	[7:0]	R_2WIREPT2_NOPASS_ADR00	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #0
0x0049	[7:0]	R_2WIREPT2_NOPASS_ADR01	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #1
0x004A	[7:0]	R_2WIREPT2_NOPASS_ADR02	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #2
0x004B	[7:0]	R_2WIREPT2_NOPASS_ADR03	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #3
0x004C	[7:0]	R_2WIREPT2_NOPASS_ADR04	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #4
0x004D	[7:0]	R_2WIREPT2_NOPASS_ADR05	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #5
0x004E	[7:0]	R_2WIREPT2_NOPASS_ADR06	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #6
0x004F	[7:0]	R_2WIREPT2_NOPASS_ADR07	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #7
0x0050	[7:0]	R_2WIREPT1_PASS_ADRIN0	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane0
0x0051	[7:0]	reserved	8	-	-	-
0x0052	[7:0]	reserved	8	-	-	-
0x0053	[7:0]	reserved	8	-	-	-
0x0054	[7:0]	reserved	8	-	-	-
0x0055	[7:0]	reserved	8	-	-	-
0x0056	[7:0]	reserved	8	-	-	-
0x0057	[7:0]	reserved	8	-	-	-
0x0058	[7:0]	reserved	8	-	-	-
0x0059	[7:0]	reserved	8	-	-	-
0x005A	[7:0]	reserved	8	-	-	-
0x005B	[7:0]	reserved	8	-	-	-
0x005C	[7:0]	reserved	8	-	-	-
0x005D	[7:0]	reserved	8	-	-	-
0x005E	[7:0]	reserved	8	-	-	-
0x005F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0060	[7:0]	R_2WIREPT1_PASS_ADR100	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #0
0x0061	[7:0]	R_2WIREPT1_PASS_ADR101	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #0
0x0062	[7:0]	R_2WIREPT1_PASS_ADR110	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #1
0x0063	[7:0]	R_2WIREPT1_PASS_ADR111	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #1
0x0064	[7:0]	R_2WIREPT1_PASS_ADR120	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #2
0x0065	[7:0]	R_2WIREPT1_PASS_ADR121	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #2
0x0066	[7:0]	R_2WIREPT1_PASS_ADR130	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through received "before rename" address for Lane1 #3
0x0067	[7:0]	R_2WIREPT1_PASS_ADR131	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through "after renamed" address to send for Lane1 #3
0x0068	[7:0]	R_2WIREPT2_NOPASS_ADR10	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #0
0x0069	[7:0]	R_2WIREPT2_NOPASS_ADR11	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #1
0x006A	[7:0]	R_2WIREPT2_NOPASS_ADR12	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #2
0x006B	[7:0]	R_2WIREPT2_NOPASS_ADR13	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #3
0x006C	[7:0]	R_2WIREPT2_NOPASS_ADR14	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #4
0x006D	[7:0]	R_2WIREPT2_NOPASS_ADR15	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #5
0x006E	[7:0]	R_2WIREPT2_NOPASS_ADR16	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #6
0x006F	[7:0]	R_2WIREPT2_NOPASS_ADR17	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x1> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #7
0x0070	[7:0]	R_2WIREPT1_PASS_ADRIN1	8	RW	8'h00	<this registers is valid only when 0x0031[0]=0x0> [7] ReservedL (must be set 0x0) [6:0] 2WIRE Pass Through counterpart Sub-Link Slave internal register access dedicated address for Lane1
0x0071	[7:0]	reserved	8	-	-	-
0x0072	[7:0]	reserved	8	-	-	-
0x0073	[7:0]	reserved	8	-	-	-
0x0074	[7:0]	reserved	8	-	-	-
0x0075	[7:0]	reserved	8	-	-	-
0x0076	[7:0]	reserved	8	-	-	-
0x0077	[7:0]	reserved	8	-	-	-
0x0078	[7:0]	reserved	8	-	-	-
0x0079	[7:0]	reserved	8	-	-	-
0x007A	[7:0]	reserved	8	-	-	-
0x007B	[7:0]	reserved	8	-	-	-
0x007C	[7:0]	reserved	8	-	-	-
0x007D	[7:0]	reserved	8	-	-	-
0x007E	[7:0]	reserved	8	-	-	-
0x007F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0080	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0081	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0082	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0083	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0084	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0085	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0086	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0087	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0088	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0089	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008A	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008B	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008C	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008D	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008E	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x008F	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0090	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x0091	[7:0]	reserved	8	-	-	-
0x0092	[7:0]	reserved	8	-	-	-
0x0093	[7:0]	reserved	8	-	-	-
0x0094	[7:0]	reserved	8	-	-	-
0x0095	[7:0]	reserved	8	-	-	-
0x0096	[7:0]	reserved	8	-	-	-
0x0097	[7:0]	reserved	8	-	-	-
0x0098	[7:0]	reserved	8	-	-	-
0x0099	[7:0]	reserved	8	-	-	-
0x009A	[7:0]	reserved	8	-	-	-
0x009B	[7:0]	reserved	8	-	-	-
0x009C	[7:0]	reserved	8	-	-	-
0x009D	[7:0]	reserved	8	-	-	-
0x009E	[7:0]	reserved	8	-	-	-
0x009F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x00A0	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A1	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A2	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A3	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A4	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A5	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A6	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A7	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A8	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00A9	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AA	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AB	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AC	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AD	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AE	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00AF	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00B0	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x00B1	[7:0]	reserved	8	-	-	-
0x00B2	[7:0]	reserved	8	-	-	-
0x00B3	[7:0]	reserved	8	-	-	-
0x00B4	[7:0]	reserved	8	-	-	-
0x00B5	[7:0]	reserved	8	-	-	-
0x00B6	[7:0]	reserved	8	-	-	-
0x00B7	[7:0]	reserved	8	-	-	-
0x00B8	[7:0]	reserved	8	-	-	-
0x00B9	[7:0]	reserved	8	-	-	-
0x00BA	[7:0]	reserved	8	-	-	-
0x00BB	[7:0]	reserved	8	-	-	-
0x00BC	[7:0]	reserved	8	-	-	-
0x00BD	[7:0]	reserved	8	-	-	-
0x00BE	[7:0]	reserved	8	-	-	-
0x00BF	[7:0]	reserved	8	-	-	-
0x00C0	[7:0]	reserved	8	-	-	-
0x00C1	[7:0]	reserved	8	-	-	-
0x00C2	[7:0]	reserved	8	-	-	-
0x00C3	[7:0]	reserved	8	-	-	-
0x00C4	[7:0]	reserved	8	-	-	-
0x00C5	[7:0]	reserved	8	-	-	-
0x00C6	[7:0]	reserved	8	-	-	-
0x00C7	[7:0]	reserved	8	-	-	-
0x00C8	[7:0]	reserved	8	-	-	-
0x00C9	[7:0]	reserved	8	-	-	-
0x00CA	[7:0]	reserved	8	-	-	-
0x00CB	[7:0]	reserved	8	-	-	-
0x00CC	[7:0]	reserved	8	-	-	-
0x00CD	[7:0]	reserved	8	-	-	-
0x00CE	[7:0]	reserved	8	-	-	-
0x00CF	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x00D0	[7:0]	R_2WIRE_DATA0	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #0
0x00D1	[7:0]	R_2WIRE_DATA1	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #1
0x00D2	[7:0]	R_2WIRE_DATA2	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #2
0x00D3	[7:0]	R_2WIRE_DATA3	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #3
0x00D4	[7:0]	R_2WIRE_DATA4	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #4
0x00D5	[7:0]	R_2WIRE_DATA5	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #5
0x00D6	[7:0]	R_2WIRE_DATA6	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #6
0x00D7	[7:0]	R_2WIRE_DATA7	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #7
0x00D8	[7:0]	R_2WIRE_DATA8	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #8
0x00D9	[7:0]	R_2WIRE_DATA9	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #9
0x00DA	[7:0]	R_2WIRE_DATA10	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #10
0x00DB	[7:0]	R_2WIRE_DATA11	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #11
0x00DC	[7:0]	R_2WIRE_DATA12	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #12
0x00DD	[7:0]	R_2WIRE_DATA13	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #13
0x00DE	[7:0]	R_2WIRE_DATA14	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #14
0x00DF	[7:0]	R_2WIRE_DATA15	8	RW	8'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote write/read data #15
0x00E0	[7:1]	R_2WIRE_DEVADR	7	RW	7'h00	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access target device address. if target addr. = self addr.; access to Sub-Link slave internal registers, else; access to remote side 2-wire serial slave devices externally connected to Sub-Link slave
	[0]	R_2WIRE_WR	1	RW	1'h0	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access write or read select 0x0: Write 0x1: Read
0x00E1	[7]	reserved	1	-	-	-
	[6:4]	R_2WIRE_WADR_BYTE	3	RW	3'h0	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote device's sub address (Word Address, register address) Byte width. Sub Address Byte width = R_2WIRE_WADR_BYTE<2:0>+1 0x0: 1Byte (= 8bit) sub address 0x1: 2Byte (=16bit) sub address Other : Reserved
	[3:0]	R_2WIRE_DATA_BYTE	4	RW	4'h0	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F remote access data Byte number. Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3Byte burst) [Write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd16 [Read rule] R_2WIRE_DATA_BYTE < 'd16

Address	bit	Register Name	width	R/W	Init	Description
0x00E2	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_CLKSEN	1	RW	1'h0	<this register is valid only when 0x0004[2:0]=0x1> 2-wire serial I/F local response clock stretching Enable 0x0: Sub-Link Master (2-wire slave) No clock stretching 0x1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode (R_SLINK_MODE=0x3) forces clock stretching Enable
0x00E3	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIRE_RD_LANE_SEL	2	RW	2'h0	<this register is valid when 0x0004[2:0]=0x1 or 0x3> Sub-Link read transaction lane select 0x0: Read from Sub-Link Lane0 0x1: Read from Sub-Link Lane1 Other: Reserved
0x00E4	[7:4]	reserved	4	-	-	-
	[3:0]	R_2WIRE_WR_LANE_SEL	4	RW	4'hF	<this register is valid only when 0x0004[2:0]=0x1> Sub-Link Write transaction lane select (multiple lanes can be written at the same time) (*each bit setting) [3] ReservedL (must be set 0x0) [2] ReservedL (must be set 0x0) [1] Write for Sub-Link Lane1 (*) [0] Write for Sub-Link Lane0 (*) 0x0: Disable 0x1: Enable
0x00E5	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_START	1	W	-	<this register is valid only when 0x0004[2:0]=0x1> 0x1: 2-wire serial I/F remote access start trigger
0x00E6	[7:0]	reserved	8	-	-	-
0x00E7	[7:0]	reserved	8	-	-	-
0x00E8	[7:0]	reserved	8	-	-	-
0x00E9	[7:0]	reserved	8	-	-	-
0x00EA	[7:0]	reserved	8	-	-	-
0x00EB	[7:0]	reserved	8	-	-	-
0x00EC	[7:0]	reserved	8	-	-	-
0x00ED	[7:0]	reserved	8	-	-	-
0x00EE	[7:0]	reserved	8	-	-	-
0x00EF	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x00F0	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_FBET_LANE_SEL	2	RW	2'h0	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET Lane select for error count 0x0: Select Sub-Link Lane0 for error count 0x1: Select Sub-Link Lane1 for error count Other: Reserved
0x00F1	[7:1]	reserved	7	-	-	-
	[0]	R_SLINK_FBETERR_CLR	1	W	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count clear 0x1: Clear
0x00F2	[7:0]	R_SLINK_FBETERR_NUM_UP	8	R	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count parameter
0x00F3	[7:0]	R_SLINK_FBETERR_NUM_DN	8	R	-	<this register is valid only when 0x1035[4]=0x1> Sub-Link FieldBET error count =256xR_SLINK_FBETERR_NUM_UP<7:0> +R_SLINK_FBETERR_NUM_DN<7:0>
0x00F4	[7:0]	reserved	8	-	-	-
0x00F5	[7:0]	reserved	8	-	-	-
0x00F6	[7:0]	reserved	8	-	-	-
0x00F7	[7:0]	reserved	8	-	-	-
0x00F8	[7:0]	reserved	8	-	-	-
0x00F9	[7:0]	reserved	8	-	-	-
0x00FA	[7:0]	reserved	8	-	-	-
0x00FB	[7:0]	reserved	8	-	-	-
0x00FC	[7:0]	reserved	8	-	-	-
0x00FD	[7:0]	reserved	8	-	-	-
0x00FE	[7:0]	reserved	8	-	-	-
0x00FF	[7:0]	reserved	8	-	-	-



Address	bit	Register Name	width	R/W	Init	Description
0x0100	[7:0]	R_TUNING_ENABLE1	8	RW	8h00	Tuning registers access Enable (1/2) 0x03: Enable (0x0109 - 0x010E registers are able to set) Other: Disable
0x0101	[7]	ReservedL	1	RW	1'h0	must be left 0x0 (default setting)
	[6]	ReservedL	1	RW	1'h0	must be left 0x0 (default setting)
	[5]	R_BDCZ_HYS1	1	RW	1'h0	Sub-Link Lane1 Hysteresis level select 0x0: 50mV 0x1: 175mV
	[4]	R_BDCZ_HYS0	1	RW	1'h0	Sub-Link Lane0 Hysteresis level select 0x0: 50mV 0x1: 175mV
	[3]	ReservedH	1	RW	1'h1	must be left 0x1 (default setting)
	[2]	ReservedH	1	RW	1'h1	must be left 0x1 (default setting)
	[1]	R_BDCZ_TERMEN1	1	RW	1'h1	Sub-Link Lane1 Termination Enable 0x0: Disable 0x1: Enable
0x0102	[7:6]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[5:4]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[3:2]	R_BDCZ_TERM_TX1	2	RW	2'h0	Sub-Link Lane1 Tx Termination select 0x0: 200ohm 0x1: 100ohm 0x2: 50ohm 0x3: Reserved
	[1:0]	R_BDCZ_TERM_TX0	2	RW	2'h0	Sub-Link Lane0 Tx Termination select 0x0: 200ohm 0x1: 100ohm 0x2: 50ohm 0x3: Reserved
0x0103	[7:6]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[5:4]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[3:2]	R_BDCZ_DRIVE_TX1	2	RW	2'h0	Sub-Link Lane1 Tx Drive current select 0x0: 3mA 0x1: 6mA 0x2: 12mA 0x3: Reserved
	[1:0]	R_BDCZ_DRIVE_TX0	2	RW	2'h0	Sub-Link Lane0 Tx Drive current select 0x0: 3mA 0x1: 6mA 0x2: 12mA 0x3: Reserved
0x0104	[7:6]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[5:4]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[3:2]	R_BDCZ_TERM_RX1	2	RW	2'h0	Sub-Link Lane1 Rx Termination select 0x0: 200ohm 0x1: 100ohm 0x2: 50ohm 0x3: Reserved
	[1:0]	R_BDCZ_TERM_RX0	2	RW	2'h0	Sub-Link Lane0 Rx Termination select 0x0: 200ohm 0x1: 100ohm 0x2: 50ohm 0x3: Reserved
0x0105	[7:6]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[5:4]	ReservedL	2	RW	2'h0	must be left 0x0 (default setting)
	[3:2]	R_BDCZ_DRIVE_RX1	2	RW	2'h0	Sub-Link Lane1 Rx Drive current select 0x0: 3mA 0x1: 6mA 0x2: 12mA 0x3: Reserved
	[1:0]	R_BDCZ_DRIVE_RX0	2	RW	2'h0	Sub-Link Lane0 Rx Drive current select 0x0: 3mA 0x1: 6mA 0x2: 12mA 0x3: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0106	[7:0]	reserved	8	-	-	-
0x0107	[7:0]	reserved	8	-	-	-
0x0108	[7:0]	reserved	8	-	-	-
0x0109	[7:0]	ReservedX	8	RW	8'h09	[Tuning register] must be left 0x09 (default setting)
0x010A	[7:0]	R_SLINK_DATA_WIDTH	8	RW	8'h0F	[Tuning register] Sub-Link clock pattern unit period = R_SLINK_DATA_WIDTH<7:0>+1 must be set to 0x15 (default 0x0F is supposed to be changed)
0x010B	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x010C	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x010D	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x010E	[7:0]	ReservedL	8	RW	8'h00	must be left 0x00 (default setting)
0x010F	[7:0]	R_TUNING_ENABLE2	8	RW	8'h00	Tuning registers access Enable (2/2) 0x25: Enable (0x0109 - 0x010E registers are able to set) Other: Disable

## GPIO/ERR/INT pin registers

Address	bit	Register Name	width	R/W	init	Description
0x1000	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_DS	1	R/W	1'h1	CMOS I/O Drivability for 2WIRE Pin (SCL/SDA and GPIO on Second 2WIRE Mode) 0x0: Normal Drive 0x1: Strong Drive
0x1001	[7:4]	R_GPIO7_MODE	4	R/W	4'h0	GPIO7 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO6_MODE	4	R/W	4'h0	GPIO6 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
0x1002	[7:4]	R_GPIO5_MODE	4	R/W	4'h0	GPIO5 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO4_MODE	4	R/W	4'h0	GPIO4 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
0x1003	[7:4]	R_GPIO3_MODE	4	R/W	4'h0	GPIO3 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO2_MODE	4	R/W	4'h0	GPIO2 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved

Address	bit	Register Name	width	R/W	init	Description
0x1004	[7:4]	R_GPIO1_MODE	4	R/W	4'h0	GPIO1 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
	[3:0]	R_GPIO0_MODE	4	R/W	4'h0	GPIO0 I/O Mode 0x0: Disable 0x1: Programmable GPO (Output Low) 0x2: Programmable GPO (Output High) 0x3: Through GPI Mode 0x4: Through GPO Mode 0x5: Second 2WIRE Mode (SCL) 0x6: Second 2WIRE Mode (SDA) Other: Reserved
0x1005	[7:4]	R_ERR1_MODE	4	R/W	4'h0	ERR1 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
	[3:0]	R_ERR0_MODE	4	R/W	4'h0	ERR0 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
0x1006	[7:4]	R_INT1_MODE	4	R/W	4'h0	INT1 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
	[3:0]	R_INT0_MODE	4	R/W	4'h0	INT0 I/O Mode 0x0: Disable 0x1: OpenDrain Output Mode 0x2: Push/Pull Output Mode Other: Reserved
0x1007	[7:4]	reserved	4	-	-	-
	[3:0]	R_EXTSYNC_MODE	4	R/W	4'h0	EXTSYNC I/O Mode 0x0: Disable 0x1: Normal Mode (Controlled by Sub-Link Register) Other: Reserved

Address	bit	Register Name	width	R/W	init	Description
0x1008	[7:4]	R_FLT_GPIO7	4	R/W	4'h7	GPIO7 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
	[3:0]	R_FLT_GPIO6	4	R/W	4'h7	GPIO6 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
0x1009	[7:4]	R_FLT_GPIO5	4	R/W	4'h7	GPIO5 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
	[3:0]	R_FLT_GPIO4	4	R/W	4'h7	GPIO4 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
0x100A	[7:4]	R_FLT_GPIO3	4	R/W	4'h7	GPIO3 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
	[3:0]	R_FLT_GPIO2	4	R/W	4'h7	GPIO2 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
0x100B	[7:4]	R_FLT_GPIO1	4	R/W	4'h7	GPIO1 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
	[3:0]	R_FLT_GPIO0	4	R/W	4'h7	GPIO0 I/O Filter Length 0x0: Filter Disable N: Filter Enable and Filter Length is NxtOSC
0x100C	[7:0]	R_ERR1_SEL	8	R/W	8'h00	ERR1 Pin Output Signal Select. Refer to Table 1.
0x100D	[7:0]	R_ERR0_SEL	8	R/W	8'h00	ERR0 Pin Output Signal Select. Refer to Table 1.
0x100E	[7:0]	reserved	8	-	-	-
0x100F	[7:0]	reserved	8	-	-	-

**Table 1.** IC Internal selectable Error / status signal (1/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x00	0 Fixed	
0x01	1 Fixed	
0x02	Vx1_LOCKN_ALL	OR operated of all operating lanes, LOCKN signal
0x03	Vx1_HTPDN_ALL	OR operated of all operating lanes, HTPDN signal
0x04	Vx1_FBETOUT_LATCH_ALL	OR operated of all operating lanes, field-bet latched result
0x05	Vx1_FBETOUT_REAL_ALL	OR operated of all operating lanes, field-bet real result
0x06	Vx1_PERR_ALL	OR operated of all operating lanes, protocol error
0x07	MLINK_CRCERR_ALL	OR operated of all operating lanes, crc error
0x08	Vx1_CLOCKSTP_ALL	clock stop detector of all lanes
0x09	MLINK_VDSK_OK_ALL	Vsync synchronization OK flag of all lanes
0x0A	MLINK_VDSK_NG_ALL	Vsync synchronization NG flag of all lanes
0x0B	MLINK_DSHNDLRERR_ALL	Data Stream Handler Error of all lanes
0x0C	Reserved	
0x0D	SLINK_PERR_ALL	OR operated of all operating lanes, protocol error
0x0E	SLINK_TMOUT_ALL	OR operated of all operating lanes, time out error
0x0F	SLINK_FBETOUT	OR operated of all operating lanes, sub-link field-bet result
0x10	Vx1_LOCKN0	lane0 LOCKN signal
0x11	Vx1_LOCKN1	lane1 LOCKN signal
0x12	Reserved	
0x13	Reserved	
0x14	Vx1_HTPDN0	lane0 HTPDN signal
0x15	Vx1_HTPDN1	lane1 HTPDN signal
0x16	Reserved	
0x17	Reserved	
0x18	Vx1_BETOUT_LATCH0	lane0 field-bet latched result
0x19	Vx1_BETOUT_LATCH1	lane1 field-bet latched result
0x1A	Reserved	
0x1B	Reserved	
0x1C	Vx1_BETOUT_REAL0	lane0 field-bet real result
0x1D	Vx1_BETOUT_REAL1	lane1 field-bet real result
0x1E	Reserved	
0x1F	Reserved	

## IC Internal selectable Error / status signal (2/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x20	Vx1_PERR0	lane0, protocol error
0x21	Vx1_PERR1	lane1, protocol error
0x22	Reserved	
0x23	Reserved	
0x24	MLINK_CRCERR0	lane0, crc error
0x25	MLINK_CRCERR1	lane1, crc error
0x26	Reserved	
0x27	Reserved	
0x28	MLINK_VSYNC0	lane0, Vsync signal
0x29	MLINK_VSYNC1	lane1, Vsync signal
0x2A	Reserved	
0x2B	Reserved	
0x2C	MLINK_HSYNC0	lane0, Hsync signal
0x2D	MLINK_HSYNC1	lane1, Hsync signal
0x2E	Reserved	
0x2F	Reserved	
0x30	MLINK_DE0	lane0, DE signal
0x31	MLINK_DE1	lane1, DE signal
0x32	Reserved	
0x33	Reserved	
0x34	MLINK_CLK0	lane0, clock signal
0x35	MLINK_CLK1	lane1, clock signal
0x36	Reserved	
0x37	Reserved	
0x38	MIPI_BYTECLK	CSI byte clock signal
0x39	OSCCLK	internal oscillator clock signal
0x3A	Reserved	
0x3B	Reserved	
0x3C	Reserved	
0x3D	Reserved	
0x3E	Reserved	
0x3F	Reserved	

## IC Internal selectable Error / status signal (3/3)

R_ERR1/0_SEL[7:0]	Error signal	Description
0x40	MLINK_FS0	lane0, Frame Start
0x41	MLINK_FS1	lane1, Frame Start
0x42	Reserved	
0x43	Reserved	
0x44	MLINK_FE0	lane0, Frame End
0x45	MLINK_FE1	lane1, Frame End
0x46	Reserved	
0x47	Reserved	
0x48	MLINK_VDSK_NG0	lane0, Vsync synchronization NG flag
0x49	MLINK_VDSK_NG1	lane1, Vsync synchronization NG flag
0x4A	Reserved	
0x4B	Reserved	
0x4C	TOP_CKSUM_ERR	register checksum error
0x4D	Reserved	
0x4E	Reserved	
0x4F	Reserved	
0x50	Reserved	
0x51	Reserved	
0x52	Reserved	
0x53	Reserved	
0x54	SLINK_PERR0	lane0, protocol error
0x55	SLINK_PERR1	lane1, protocol error
0x56	Reserved	
0x57	Reserved	
0x58	SLINK_TMOUT0	lane0, time out error
0x59	SLINK_TMOUT1	lane1, time out error
0x5A	Reserved	
0x5B	Reserved	

Main-link registers

Address	bit	Register Name	width	R/W	init	Description
0x1010	[7:6]	R_MLINK_NHSEL0	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane0) 0x2: V-by-One® HS standard mode Other: Reserved
	[5:4]	R_MLINK_COLO	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane0) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved  * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1
	[3]	reserved	1	-	-	-
	[2]	R_MLINK_AOCEN0	1	R/W	1'h0	V-by-One® Auto Offset Cancel Enable (for Lane0) 0x0: Disable 0x1: Enable
	[1]	ReservedL	1	R/W	1'h0	must be left 0x0 (default setting)
	[0]	R_MLINK_AEQEN0	1	R/W	1'h0	V-by-One® Adaptive Equalizer Setting (for Lane0) 0x0: Static Equalizer Mode (0x1011[6:4] register is to control) 0x1: Adaptive Equalizer Mode for Strength Control (CTLC)
	[7]	reserved	1	-	-	-
0x1011	[6:4]	R_MLINK_LEQCTLC0	3	R/W	3'h0	<this register is valid only when 0x1010[0]=0> V-by-One® Main-Link Equalizer strength Control setting (for Lane0) 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3]	reserved	1	-	-	-
	[2:0]	R_MLINK_LEQCTRL0	3	R/W	3'h0	V-by-One® Main-Link Equalizer baseline Raise setting (for Lane0) 0x0 (0b000): base gain level0 (the lowest) 0x1 (0b001): base gain level1 0x3 (0b011): base gain level2 0x2 (0b010): base gain level3 0x6 (0b110): base gain level4 0x7 (0b111): base gain level5 0x5 (0b101): base gain level6 0x4 (0b100): base gain level7 (the highest)



Address	bit	Register Name	width	R/W	init	Description
0x1012	[7:5]	reserved	3	-	-	-
	[4]	R_RGB565_ON_L0	1	R/W	1'h0	<this regiseter is valid only when 0x1012[3:0]=0x1> Main-Link Input Data Format Setting2 for all lane 0x0: RGB888 0x1: RGB565
	[3:0]	R_VX1_LANE_FMT0	4	R/W	4'h0	Main-Link Input Data Format Setting for all lane 0x0: MPRF (Main-Link PRivate Format) 0x1: RGB888 or RGB565 0x2: YUV422 - Normal Mode1 0x3: YUV422 - Normal Mode2 0x4: YUV422 - Normal Mode3 0x5: YUV422 - Demux Mode1 0x6: YUV422 - Demux Mode2 0x7: RAW8 - Normal Mode1 0x8: RAW8 - Normal Mode2 0x9: RAW8 - Demux Mode1 0xA: RAW10 - Normal Mode1 0xB: RAW10 - Demux Mode1 0xC: RAW10 - Demux Mode2 0xD: RAW12 - Normal Mode1 0xE: RAW12 - Demux Mode1 0xF: RAW12 - Demux Mode2
0x1013	[7:1]	ReservedL	7	R/W	7'h00	must be left 0x00 (default setting)
	[0]	R_NONUSE_LSLE	1	R/W	1'h0	Line start and Line end code use or non-use setting for all Main-Link lane 0x0: When a system is used mipi line start and line end, must be set 0x0 (*) 0x1: When a system is not use mipi line start and line end, must be set 0x1 (*) When 0x1013[0] = 0x0, 0x1606[1:0] must be set 0x3.

Address	bit	Register Name	width	R/W	init	Description
0x1014	[7:6]	R_MLINK_NHSEL1	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for Lane1) 0x2: V-by-One® HS standard mode Other: Reserved
	[5:4]	R_MLINK_COL1	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for Lane1) 0x1: 3Byte mode 0x2: 4Byte mode Other: Reserved  * use case setting example MPRF : 0x2 RGB888 or RGB565 : 0x1 YUV422 - Normal Mode1 : 0x1 YUV422 - Normal Mode2 : 0x1 YUV422 - Normal Mode3 : 0x1 YUV422 - Demux Mode1 : 0x2 YUV422 - Demux Mode2 : 0x2 RAW8 - Normal Mode1 : 0x1 RAW8 - Normal Mode2 : 0x1 RAW8 - Demux Mode1 : 0x2 RAW10 - Normal Mode1 : 0x1 RAW10 - Demux Mode1 : 0x2 RAW10 - Demux Mode2 : 0x1 RAW12 - Normal Mode1 : 0x1 RAW12 - Demux Mode1 : 0x2 RAW12 - Demux Mode2 : 0x1
	[3]	reserved	1	-	-	-
	[2]	R_MLINK_AOCEN1	1	R/W	1'h0	V-by-One® Auto Offset Cancel Enable (for Lane1) 0x0: Disable 0x1: Enable
	[1]	ReservedL	1	R/W	1'h0	must be left 0x0 (default setting)
	[0]	R_MLINK_AEQEN1	1	R/W	1'h0	V-by-One® Adaptive Equalizer Setting (for Lane1) 0x0: Static Equalizer Mode (0x1015[6:4] register is to control) 0x1: Adaptive Equalizer Mode for Strength Control (CTLC)
	[3]	reserved	1	-	-	-
0x1015	[7]	reserved	1	-	-	-
	[6:4]	R_MLINK_LEQCTLC1	3	R/W	3'h0	<this regiseter is valid only when 0x1014[0]=0> V-by-One® Main-Link Equalizer strength Control setting (for Lane1) 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3]	reserved	1	-	-	-
	[2:0]	R_MLINK_LEQCTLR1	3	R/W	3'h0	V-by-One® Main-Link Equalizer baseline Raise setting (for Lane1) 0x0 (0b000): base gain level0 (the lowest) 0x1 (0b001): base gain level1 0x3 (0b011): base gain level2 0x2 (0b010): base gain level3 0x6 (0b110): base gain level4 0x7 (0b111): base gain level5 0x5 (0b101): base gain level6 0x4 (0b100): base gain level7 (the highest)
0x1016	[7:0]	reserved	8	-	-	-
0x1017	[7:0]	ReservedX	8	R/W	8'h00	must be left 0x00 (default setting)

Address	bit	Register Name	width	R/W	init	Description
0x1018	[7:0]	ReservedX	8	R/W	8'h90	must be left 0x90 (default setting)
0x1019	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x101A	[7:0]	reserved	8	-	-	-
0x101B	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x101C	[7:0]	ReservedX	8	R/W	8'h90	must be left 0x90 (default setting)
0x101D	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x101E	[7:0]	reserved	8	-	-	-
0x101F	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x1020	[7:5]	reserved	3	-	-	-
	[4:0]	ReservedL	4	R/W	4'h0	must be left 0x0 (default setting)
0x1021	[7:0]	R_PLL_SETTING[47:40]	8	R/W	8'h00	PLL setting value, Feedback Divider value (integer part)
0x1022	[7:3]	R_PLL_SETTING[39:35]	5	-	5'h00	PLL setting value (Must be set 0x00)
	[2:0]	R_PLL_SETTING[34:32]	3	R/W	3'h0	PLL setting value, Reference Divider value
0x1023	[7]	R_PLL_SETTING[31]	1	-	1'h0	PLL setting value (Must be set 0x0)
	[6:4]	R_PLL_SETTING[30:28]	3	R/W	3'h0	PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2)
	[3]	R_PLL_SETTING[27]	1	-	1'h0	PLL setting value (Must be set 0x0)
	[2:0]	R_PLL_SETTING[26:24]	3	R/W	3'h0	PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2)
0x1024	[7:0]	R_PLL_SETTING[23:16]	8	R/W	8'h00	PLL setting value, Feedback Divider value (decimal part MSB)
0x1025	[7:0]	R_PLL_SETTING[15:8]	8	R/W	8'h00	PLL setting value, Feedback Divider value (decimal part)
0x1026	[7:0]	R_PLL_SETTING[7:0]	8	R/W	8'h00	PLL setting value, Feedback Divider value (decimal part LSB)
0x1027	[7:4]	reserved	4	-	-	-
	[3]	ReservedL	1	R/W	1'h0	must be left 0x0 (default setting)
	[2]	ReservedH	1	R/W	1'h0	Must be set 0x1
	[1]	ReservedH	1	R/W	1'h0	Must be set 0x1
	[0]	ReservedH	1	R/W	1'h0	Must be set 0x1
0x1028	[7:2]	reserved	6	-	-	-
	[1:0]	R_CSILANENUM_SEL	2	R/W	2'h0	MIPI CSI total active Lane number Setting 0x0:CSI 4 lane mode (**) 0x1:Reserved 0x2:CSI 2 lane mode 0x3:CSI 1 lane mode (* ) 0x1605 register is related to this register (**) For MIPI 2PORT2LANE, total 4 lane (0x0) setting is required to be set.
0x1029	[7:0]	reserved	8	-	-	-
0x102A	[7:0]	reserved	8	-	-	-
0x102B	[7:0]	reserved	8	-	-	-
0x102C	[7:0]	reserved	8	-	-	-
0x102D	[7:0]	reserved	8	-	-	-
0x102E	[7:0]	reserved	8	-	-	-
0x102F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x1030	[7:5]	reserved	3	-	-	-
	[4]	R_VX1_CLK_DETEN	1	R/W	1'h0	Main-Link Clock Stop Detection Enable 0x0: Disable 0x1: Enable
	[3:0]	R_VX1_CLK_SEL	4	R/W	4'h0	Main-Link Master Clock Select [3]Main Mode <0x1030[3] register is valid only when 0x1030[4]=0x1> 0x0: Fixed Mode 0x1: Auto Detection Mode  [2] All Main-Link Clock Lost Status Mask 0x0: not use as interrupt factor 0x1: use as interrupt factor (this register is related to 0x1711[6] and 0x1719[6])  [1:0]Main-Link Master Clock Select <0x1030[1:0] register is valid only when 0x1030[3]=0x0> 0x0: Lane0 Main-Link Clock is Master Clock 0x1: Lane1 Main-Link Clock is Master Clock Other:Reserved
0x1031	[7:1]	reserved	7	-	-	-
	[0]	R_VDSKCHK_EN	1	R/W	1'h0	Input Vsync Deskew Check Enable 0x0: Disable 0x1: Enable
0x1032	[7:0]	R_VDSKCHK_LINEPIX[15:8]	8	R/W	8'h0	<this register is valid only when 0x1031[0]=0x1> Limit Pixel-number for Input Vsync Deskew MSB
0x1033	[7:0]	R_VDSKCHK_LINEPIX[7:0]	8	R/W	8'h0	<this register is valid only when 0x1031[0]=0x1> Limit Pixel-number for Input Vsync Deskew LSB
0x1034	[7:0]	R_VDSKCHK_LINEUM	8	R/W	8'h0	<this register is valid only when 0x1031[0]=0x1> Limit Line-number for Input Vsync Deskew Limit Number = R_VDSKCHK_LINEPIX*R_VDSKCHK_LINEUM
0x1035	[7:6]	reserved	2	-	-	-
	[5:4]	R_SBET_MODE	2	R/W	2'h0	Sub-Link Field BET Mode Select [5] BETOUT select 0x0: Raw BETOUT output 0x1: Latched BETOUT output  [4] Sub-Link Field BET Enable 0x0: Disable 0x1: Enable
	[3]	ReservedL	1	R/W	1'h0	must be left 0x0 (default setting)
	[2]	ReservedL	1	R/W	1'h0	must be left 0x0 (default setting)
	[1]	R_MBET_MODE1	1	R/W	1'h0	Main-Link Field BET Mode Enable (for Lane1) 0x0: Disable 0x1: Enable
	[0]	R_MBET_MODE0	1	R/W	1'h0	Main-Link Field BET Mode Enable (for Lane0) 0x0: Disable 0x1: Enable
0x1036	[7:0]	reserved	8	-	-	-
0x1037	[7:0]	reserved	8	-	-	-
0x1038	[7:0]	reserved	8	-	-	-
0x1039	[7:0]	reserved	8	-	-	-
0x103A	[7:0]	reserved	8	-	-	-
0x103B	[7:0]	reserved	8	-	-	-
0x103C	[7:0]	reserved	8	-	-	-
0x103D	[7:0]	reserved	8	-	-	-
0x103E	[7:0]	reserved	8	-	-	-
0x103F	[7:0]	reserved	8	-	-	-

## Pre-processing registers

Address	bit	Register Name	width	R/W	Init	Description
0x1100	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN0	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane0 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1101	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN0	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane0 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1102	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN0	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane0 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1103	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE0	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane0 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1104	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POLO	1	R/W	1'h0	<this register is valid only when 0x1103[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane0 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1105	[7:0]	R_VX1_WC_LOW0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane0
0x1106	[7:0]	R_VX1_WC_UP0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane0
0x1107	[7:0]	R_VX1_DATAID0	8	R/W	8'h00	<this register is valid only when 0x1100[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane0  * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1108	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC0	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane0 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1109	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x110A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR0	1	RC	1'h0	CRC error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x110B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR0	1	RC	1'h0	ECC single error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x110C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR0	1	RC	1'h0	ECC double error register for Main-Link Lane0 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

Address	bit	Register Name	width	R/W	Init	Description
0x1200	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_PH_EN1	1	R/W	1'h0	MIPI Packet Header mode select for Main-Link Lane1 0x0: Packet Header is generated by register settings 0x1: Packet Header is through from Main-Link input stream
0x1201	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_CRC_EN1	1	R/W	1'h0	Main-Link CRC mode select for Main-Link Lane1 0x0: Main-Link input stream does not have CRC data 0x1: Main-Link input stream has CRC data
0x1202	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_SP_EN1	1	R/W	1'h0	MIPI Short Packet mode select for Main-Link Lane1 0x0: Main-Link input stream does not have Short Packet 0x1: Short Packet is through from Main-Link input stream
0x1203	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VVALID_MODE1	1	R/W	1'h0	MIPI Frame Start & Frame End (FS/FE) mode select for Main-Link Lane1 0x0: FS/FE data are through from Main-Link input stream 0x1: FS/FE data are generated based on the timing of the VSYNC signal
0x1204	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_VSYNC_POL1	1	R/W	1'h0	<this register is valid only when 0x1203[0]=0x1> Polarity setting of VSYNC signal to generate FS/FE for Main-Link Lane1 0x0: use Low pulse VSYNC signal (FE: Falling timing, FS: Rising timing) 0x1: use High pulse VSYNC signal (FE: Rising timing, FS: Falling timing)
0x1205	[7:0]	R_VX1_WC_LOW1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Word Count (LSB) manual setting for Main-Link Lane1
0x1206	[7:0]	R_VX1_WC_UP1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Word Count (MSB) manual setting for Main-Link Lane1
0x1207	[7:0]	R_VX1_DATAID1	8	R/W	8'h00	<this register is valid only when 0x1200[0]=0x0> MIPI Packet Header's Data ID manual setting for Main-Link Lane1  * use case setting example YUV422-8bit: 0x1E RGB888: 0x24 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C
0x1208	[7:1]	reserved	7	-	7'h00	-
	[0]	R_VX1_MASK_ECC1	1	R/W	1'h0	Masking and Ignoring both MIPI short packet and MIPI long packet when ECC double error is detected for Main-Link Lane1 0x0: Disable 0x1: Mask Processing when ECC double error is detected
0x1209	[7:1]	reserved	7	-	7'h00	-
	[0]	reservedL	1	R/W	1'h0	must be left 0x0 (default setting)
0x120A	[7:1]	reserved	7	-	7'h00	-
	[0]	R_CRC_ERR1	1	RC	1'h0	CRC error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect CRC error
0x120B	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_CRCT_ERR1	1	RC	1'h0	ECC single error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC single error
0x120C	[7:1]	reserved	7	-	7'h00	-
	[0]	R_ECC_DOUBLE_ERR1	1	RC	1'h0	ECC double error register for Main-Link Lane1 (clear the error status after reading register automatically) 0x0: no error 0x1: detect ECC double error

## Data Stream Handling registers

Address	bit	Register Name	width	R/W	Init	Description
0x1501	[7:5]	reserved	3	-	3'h0	-
	[4:0]	R_MODE_NO	5	R/W	5'h00	Main-Link input data stream handling mode number 0x00: CAM A : Main-Link Lane0 -> MIPI port0 0x01: CAM A : Main-Link Lane0 -> MIPI port0 and port1 (distribution) 0x02: CAM B : Main-Link Lane1 -> MIPI port0 0x03: CAM B : Main-Link Lane1 -> MIPI port0 and port1 (distribution) 0x08: CAM A : Main-Link Lane0 and Lane1 -> MIPI port0 0x0A: CAM A : Main-Link Lane0 -> MIPI port0 CAM B : Main-Link Lane1 -> MIPI port1 0x0B: CAM A : Main-Link Lane0 -> MIPI port1 CAM B : Main-Link Lane1 -> MIPI port0 Others: Reserved
0x1502	[7:0]	R_DSH_OFTIM_0[7:0]	8	R/W	8'hED	Main-Link Data Stream Handling offset read timing (LSB) for Lane0
0x1503	[7:1]	reserved	7	-	7'h00	-
	[0]	R_DSH_OFTIM_0[8]	1	R/W	1'h0	Main-Link Data Stream Handling offset read timing (MSB) for Lane0 R_DSH_OFTIM_0[9:0] must be more than or equal to 0x064.
0x1504	[7:0]	R_DSH_OFTIM_1[7:0]	8	R/W	8'hED	Main-Link input data stream handling offset read timing (LSB) for Lane1
0x1505	[7:1]	reserved	7	-	7'h00	-
	[0]	R_DSH_OFTIM_1[8]	1	R/W	1'h0	Main-Link Data Stream Handling offset read timing (MSB) for Lane1 R_DSH_OFTIM_0[9:0] must be more than or equal to 0x064.

MIPI CSI-2 output register

Address	bit	Register Name	width	R/W	Init	Description
0x1600	[7:5]	Reserved	3	-	3'h0	-
	[4:0]	R_ANALOG	5	R/W	5'h00	[4] MIPI Power Down 0x0: Power Down 0x1: Normal operation  [3] MIPI Soft Reset 0x0: Reset 0x1: Normal operation  [2] ReservedL (must be set 0x0) [1] ReservedH (must be set 0x1) [0] ReservedL (must be set 0x0)
0x1601	[7:0]	ReservedX	8	R/W	8'h1B	must be left as default 0x1B
0x1602	[7:0]	R_TX_LANE_SEL0	8	R/W	8'hE4	MIPI Tx Lane assignment select (*each bit setting) [7:6] MTX3P/N (MTX3) (*) [5:4] MTX2P/N (MTX2) (*) [3:2] MTX1P/N (MTX1) (*) [1:0] MTX0P/N (MTX0) (*) 0x0: 1st Byte output 0x1: 2nd Byte output 0x2: 3rd Byte output (or 1st Byte on 2PORT mode) 0x3: 4th Byte output (or 2nd Byte on 2PORT mode)  * use case setting example 1PORT1LANE: 0xE4 (Port0:MTX0) 1PORT2LANE: 0xE4 (Port0:MTX0, MTX1) 1PORT4LANE: 0xE4 (Port0:MTX0, MTX1, MTX2, MTX3) 2PORT1LANE: 0x72 (Port0:MTX1, Port1:MTX0) 0x63 (Port0:MTX1, Port1:MTX2) 0x36 (Port0:MTX3, Port1:MTX0) 2PORT2LANE: 0x72 (Port0:MTX3,MTX1, Port1:MTX0,MTX2)
0x1603	[7:2]	Reserved	6	-	6'h00	-
	[1:0]	R_TX_LANE_SEL1	2	R/W	2'h0	<this register is valid when 0x1605[2:0]=0x4 or 0x5> MIPI Tx Lane assignment select for Port1 on 2PORT mode  * use case setting example 2PORT1LANE: 0x0 (Port1:MTX0) 2PORT1LANE: 0x2 (Port1:MTX2) 2PORT2LANE: 0x0 (Port1:MTX0,MTX2)
0x1604	[7:0]	ReservedX	8	R/W	8'h3F	must be left as default 0x3F



Address	bit	Register Name	width	R/W	Init	Description
0x1605	[7]	Reserved	1	-	1'h0	-
	[6:0]	R_LANE_EN	7	R/W	7'h2B	[6:5] MIPI Data lane Enable (*each bit setting) [6] Data Port1 (*) [5] Data Port0 (*) 0x0: OFF 0x1: ON  [4:3] MIPI CLK lane Enable (*each bit setting) [4] CLK Port1 (*) [3] CLK Port0 (*) 0x0: OFF 0x1: ON  [2:0] MIPI Configuration 0x0 (=0b000): 1PORT1LANE 0x1 (=0b001): 1PORT2LANE 0x3 (=0b011): 1PORT4LANE 0x4 (=0b100): 2PORT1LANE 0x5 (=0b101): 2PORT2LANE Other:Reserved  * use case setting example 1PORT1LANE: 0x28 (=0b0101_000) 1PORT2LANE: 0x29 (=0b0101_001) 1PORT4LANE: 0x2B (=0b0101_011) 2PORT1LANE: 0x7C (=0b1111_100) 2PORT2LANE: 0x7D (=0b1111_101)
0x1606	[7:2]	ReservedX	6	R/W	6'h10	must be set 0x13
	[1:0]	R_MODE_SET	2	R/W	2'h0	clock continous mode select (*each bit setting) [1] clock continous mode select for Port1 (*) [0] clock continous mode select for Port0 (*) 0x0:OFF (HS clock off and become LP mode during V-Blanking term) 0x1:ON (HS clock permanently on) (*) When 0x1013[0] = 0x0, 0x1606[1:0] must be set 0x3.
0x1607	[7:0]	ReservedX	8	R/W	8'hE4	must be left 0xE4 (default setting)
0x1608	[7:4]	Reserved	4	-	4'h0	-
	[3:0]	ReservedX	4	R/W	4'hE	must be left 0xE (default setting)

Address	bit	Register Name	width	R/W	Init	Description
0x1609	[7:0]	R_TX_CLK_PREPARE0	8	R/W	8'h04	CLK lane Prepare period setting Port0  • tCLK-PREPARE: $(8 \times R\_TX\_CLK\_PREPARE0 + 8) \times tTBIT + 13$ [ns] ~ $(8 \times R\_TX\_CLK\_PREPARE0 + 8) \times tTBIT + 33$ [ns]
0x160a	[7:0]	R_TX_CLK_ZERO0	8	R/W	8'h1D	CLK lane ZERO period setting Port0  • tCLK-PREPARE + tCLK-ZERO: $(8 \times (R\_TX\_CLK\_PREPARE0 + R\_TX\_CLK\_ZERO0) + 31.5) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_CLK\_PREPARE0 + R\_TX\_CLK\_ZERO0) + 31.5) \times tTBIT - 19$ [ns]
0x160b	[7:0]	R_TX_CLK_TRAILO	8	R/W	8'h07	CLK lane TRAIL period setting Port0  • tCLK-TRAIL: $(8 \times R\_TX\_CLK\_TRAIL0 - 6.5) \times tTBIT + 1$ [ns] ~ $(8 \times R\_TX\_CLK\_TRAIL0 - 6.5) \times tTBIT + 6$ [ns]  • tEOT(clk lane): $(8 \times R\_TX\_CLK\_TRAIL0 - 6.5) \times tTBIT + 16$ [ns] ~ $(8 \times R\_TX\_CLK\_TRAIL0 - 6.5) \times tTBIT + 34$ [ns]
0x160c	[7:0]	reservedX	8	R/W	8'h02	must be left 0x2 (default setting)
0x160d	[7:0]	R_TX_CLK_POST0	8	R/W	8'h0C	CLK lane POST period setting Port0  • tCLK-POST: $(8 \times R\_TX\_CLK\_POST0 + 22.5) \times tTBIT - 6$ [ns] ~ $(8 \times R\_TX\_CLK\_POST0 + 22.5) \times tTBIT - 1$ [ns]
0x160e	[7:0]	R_TX_THS_EXIT0	8	R/W	8'h0B	CLK and Data lane EXIT period setting Port0  • tHS-EXIT (*) (**): $(8 \times R\_TX\_THS\_EXIT0 + 80) \times tTBIT + 15$ [ns] ~ $(8 \times R\_TX\_THS\_EXIT0 + 80) \times tTBIT + 23$ [ns] (*) tHS-EXIT is depended on inputted horizontal or vertical blanking term. (**) 1port4lane (when 0x1605[2:0]=0x3)
0x160f	[7:0]	R_TX_TLPX0	8	R/W	8'h05	CLK and Data lane TLPX period setting Port0  • tLPX: $(8 \times R\_TX\_TLPX0 + 8) \times tTBIT - 2$ [ns] ~ $(8 \times R\_TX\_TLPX0 + 8) \times tTBIT + 0$ [ns]
0x1610	[7:0]	R_TX_THS_PREPARE0	8	R/W	8'h04	Data lane Prepare period setting Port0  • tHS-PREPARE: $(8 \times R\_TX\_THS\_PREPARE0 + 8) \times tTBIT + 13$ [ns] ~ $(8 \times R\_TX\_THS\_PREPARE0 + 8) \times tTBIT + 33$ [ns]
0x1611	[7:0]	R_TX_THS_ZERO0	8	R/W	8'h10	Data lane ZERO period setting Port0  • tHS-PREPARE + tHS-ZERO (for short packet): $(8 \times (R\_TX\_THS\_PREPARE0 + R\_TX\_THS\_ZERO0) + 55) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_THS\_PREPARE0 + R\_TX\_THS\_ZERO0) + 55) \times tTBIT - 19$ [ns]  • tHS-PREPARE + tHS-ZERO (for long packet) (**): $(8 \times (R\_TX\_THS\_PREPARE0 + R\_TX\_THS\_ZERO0) + 127) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_THS\_PREPARE0 + R\_TX\_THS\_ZERO0) + 127) \times tTBIT - 19$ [ns] (**) 1port4lane (when 0x1605[2:0]=0x3)
0x1612	[7:0]	R_TX_THS_TRAILO	8	R/W	8'h07	Data lane TRAIL period setting Port0  • tHS-TRAIL: $(8 \times R\_TX\_THS\_TRAIL0 - 7) \times tTBIT + 1$ [ns] ~ $(8 \times R\_TX\_THS\_TRAIL0 - 7) \times tTBIT + 6$ [ns]  • tEOT(data lane): $(8 \times R\_TX\_THS\_TRAIL0 - 7) \times tTBIT + 16$ [ns] ~ $(8 \times R\_TX\_THS\_TRAIL0 - 7) \times tTBIT + 34$ [ns]
0x1613	[7:0]	reservedX	8	R/W	8'h40	must be left 0x40 (default setting)

Address	bit	Register Name	width	R/W	Init	Description
0x1614	[7:0]	R_TX_CLK_PREPARE1	8	R/W	8'h04	CLK lane Prepare period setting Port1  • tCLK-PREPARE: $(8 \times R\_TX\_CLK\_PREPARE1 + 8) \times tTBIT + 13$ [ns] ~ $(8 \times R\_TX\_CLK\_PREPARE1 + 8) \times tTBIT + 33$ [ns]
0x1615	[7:0]	R_TX_CLK_ZERO1	8	R/W	8'h1D	CLK lane ZERO period setting Port1  • tCLK-PREPARE + tCLK-ZERO: $(8 \times (R\_TX\_CLK\_PREPARE1 + R\_TX\_CLK\_ZERO1) + 31.5) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_CLK\_PREPARE1 + R\_TX\_CLK\_ZERO1) + 31.5) \times tTBIT - 19$ [ns]
0x1616	[7:0]	R_TX_CLK_TRAIL1	8	R/W	8'h07	CLK lane TRAIL period setting Port1  • tCLK-TRAIL: $(8 \times R\_TX\_CLK\_TRAIL1 - 6.5) \times tTBIT + 1$ [ns] ~ $(8 \times R\_TX\_CLK\_TRAIL1 - 6.5) \times tTBIT + 6$ [ns]  • tEOT(clk lane): $(8 \times R\_TX\_CLK\_TRAIL1 - 6.5) \times tTBIT + 16$ [ns] ~ $(8 \times R\_TX\_CLK\_TRAIL1 - 6.5) \times tTBIT + 34$ [ns]
0x1617	[7:0]	reservedX	8	R/W	8'h02	must be left 0x2 (default setting)
0x1618	[7:0]	R_TX_CLK_POST1	8	R/W	8'h0C	CLK lane POST period setting Port1  • tCLK-POST: $(8 \times R\_TX\_CLK\_POST1 + 22.5) \times tTBIT - 6$ [ns] ~ $(8 \times R\_TX\_CLK\_POST1 + 22.5) \times tTBIT - 1$ [ns]
0x1619	[7:0]	R_TX_THS_EXIT1	8	R/W	8'h0B	CLK and Data lane EXIT period setting Port1  • tHS-EXIT (*): $(8 \times R\_TX\_THS\_EXIT1 + 80) \times tTBIT + 15$ [ns] ~ $(8 \times R\_TX\_THS\_EXIT1 + 80) \times tTBIT + 23$ [ns] (*) tHS-EXIT is depended on inputted horizontal or vertical blanking term. (**) 1port4lane (when 0x1605[2:0]=0x3)
0x161a	[7:0]	R_TX_TLPX1	8	R/W	8'h05	CLK and Data lane TLPX period setting Port1  • tLPX: $(8 \times R\_TX\_TLPX1 + 8) \times tTBIT - 2$ [ns] ~ $(8 \times R\_TX\_TLPX1 + 8) \times tTBIT + 0$ [ns]
0x161b	[7:0]	R_TX_THS_PREPARE1	8	R/W	8'h04	Data lane Prepare period setting Port1  • tHS-PREPARE: $(8 \times R\_TX\_THS\_PREPARE1 + 8) \times tTBIT + 13$ [ns] ~ $(8 \times R\_TX\_THS\_PREPARE1 + 8) \times tTBIT + 33$ [ns]
0x161c	[7:0]	R_TX_THS_ZERO1	8	R/W	8'h10	Data lane ZERO period setting Port1  • tHS-PREPARE + tHS-ZERO (for short packet): $(8 \times (R\_TX\_THS\_PREPARE1 + R\_TX\_THS\_ZERO1) + 55) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_THS\_PREPARE1 + R\_TX\_THS\_ZERO1) + 55) \times tTBIT - 19$ [ns]  • tHS-PREPARE + tHS-ZERO (for long packet) (**): $(8 \times (R\_TX\_THS\_PREPARE1 + R\_TX\_THS\_ZERO1) + 127) \times tTBIT - 27$ [ns] ~ $(8 \times (R\_TX\_THS\_PREPARE1 + R\_TX\_THS\_ZERO1) + 127) \times tTBIT - 19$ [ns] (**) 1port4lane (when 0x1605[2:0]=0x3)
0x161d	[7:0]	R_TX_THS_TRAIL1	8	R/W	8'h07	Data lane TRAIL period setting Port1  • tHS-TRAIL: $(8 \times R\_TX\_THS\_TRAIL1 - 7) \times tTBIT + 1$ [ns] ~ $(8 \times R\_TX\_THS\_TRAIL1 - 7) \times tTBIT + 6$ [ns]  • tEOT(data lane): $(8 \times R\_TX\_THS\_TRAIL1 - 7) \times tTBIT + 16$ [ns] ~ $(8 \times R\_TX\_THS\_TRAIL1 - 7) \times tTBIT + 34$ [ns]
0x161e	[7:0]	reservedX	8	R/W	8'h40	must be left 0x40 (default setting)

Address	bit	Register Name	width	R/W	Init	Description
0x161f	[7:4]	Reserved	4	-	4'h0	-
	[3:0]	R_REQ_SEL	4	R/W	4'h0	MIPI Tx Lane Port assignment (*each bit setting) [3] MTX3P/N (MTX3) (*) [2] MTX2P/N (MTX2) (*) [1] MTX1P/N (MTX1) (*) [0] MTX0P/N (MTX0) (*) 0: Port0 1: Port1  * use case setting example 1PORT mode: 0x0 (=0b0000) 2PORT mode: 0x5 (=0b0101) (Port0:MTX3,MTX1, Port1:MTX0,MTX2)

Software reset and power down registers

Address	bit	Register Name	width	R/W	init	Description
0x1700	[7:3]	reserved	5	-	-	-
	[2]	ReservedL	1	W	-	must be set 0x0
	[1]	R_INTC_ALL1	1	W	-	Clear All Interrption factor for INT1 pin 0x1: Clear
	[0]	R_INTC_ALL0	1	W	-	Clear All Interrption factor for INT0 pin 0x1: Clear
0x1701	[7:6]	ReservedL	2	W	-	must be set 0x0
	[5:4]	R_PPRCSSR_RST	2	W	-	Software Reset for Pre-processor (*each bit setting) [5] Main-Link Lane1 (*) [4] Main-Link Lane0 (*) 0x1: Software Reset
	[3]	R_DSHNDLR_RST	1	W	-	Software Reset for Data stream handler 0x1: Software Reset (*) (* must write 0x1 for 0x1701[2] simultaneously, so write 0x3 for 0x1701[3:2])
	[2]	R_CSI_RST	1	W	-	Software Reset for MIPI-CSI2 TX 0x1: Software Reset (*) (* must write 0x1 for 0x1701[3] simultaneously, so write 0x3 for 0x1701[3:2])
	[1]	R_BDC_RST	1	W	-	Software Reset for Sub-Link 0x1: Software Reset * 0x1701[1] Sub-Link reset includes 2-wire slave controller so that 0x1701[1] reset write access cause immediate 2-wire slave abort and reaction to 2-wire master become NACK. In order to avoid NACK, for most cases, 0x0001 Sub-Link reset without 2-wire slave controller is fair enough.
0x1702	[7:1]	reserved	7	-	-	-
	[0]	R_REG_RST	1	W	-	Software Reset for Register 0x1: Software Reset
0x1703	[7:2]	reserved	6	-	-	-
	[1]	reserved	1	-	-	-
	[0]	R_PLL_PDN	1	R/W	1'h0	PLL Power Down 0x0: PowerDown 0x1: PowerOn
0x1704	[7:6]	ReservedL	2	R/W	2'h0	must be left 0x0 (default setting)
	[5:4]	R_MLINKRX_PDN	2	R/W	2'h0	Main-Link Reciver Power Down (*each bit setting) [5] Main-Link Lane1 (*) [4] Main-Link Lane0 (*) 0x0: Power Down 0x1: Power On
	[3:2]	ReservedL	2	R/W	2'h0	must be left 0x0 (default setting)
	[1:0]	R_SLINK_PDN	2	R/W	2'h0	Sub-Link Power Down (*each bit setting) [1] Sub-Link Lane1 (*) [0] Sub-Link Lane0 (*) 0x0: Power Down 0x1: Power On
0x1705	[7:0]	reserved	8	-	-	-
0x1706	[7:0]	reserved	8	-	-	-
0x1707	[7:0]	reserved	8	-	-	-
0x1708	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x1709	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x170A	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x170B	[7:0]	ReservedL	8	R/W	8'h00	must be left 0x00 (default setting)
0x170C	[7:0]	reserved	8	-	-	-
0x170D	[7:0]	reserved	8	-	-	-
0x170E	[7:0]	reserved	8	-	-	-
0x170F	[7:2]	reserved	6	-	-	-
	[1:0]	R_DSHNDLR_INTSEL	2	R/W	2'h3	Data stream Handler Interruption Detection condition teaching 0x0: Main-Link side input upstream is faster 0x1: MIPI side output downstream is faster 0x2,0x3: Both stream is the same speed

## Interrupt registers

Address	bit	Register Name	width	R/W	init	Description
0x1710	[7:0]	R_INTR_MLRX0_0	8	R	-	Interrupt to INT0 [5] Main-Link protocol error for Lane1 in normal operation (when LOCKN1=L) [4] Main-Link protocol error for Lane0 in normal operation (when LOCKN0=L) [1] Main-Link RX LOCKN=L to H detection flag for Lane1 (*) [0] Main-Link RX LOCKN=L to H detection flag for Lane0 (*) [7][6][3][2] Reserved 0x1: error status or detection flag (* this interrupt registers become 1 once after startup)
0x1711	[7:6]	R_INTR_MODE0_0	2	R	-	Interrupt to INT0 [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x1: detection flag
	[5:4]	R_INTR_DSHNDLR0_0	2	R	-	Interrupt to INT0 [5] Data Stream Handler Distribution error [4] Reserved 0x1: error status
	[3:0]	R_INTR_FMT0_0	4	R	-	Interrupt to INT0 [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L)(*) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L)(*) [3][2] Reserved 0x1: error status (* this interrupt is valid when Main-Link stream contains CRC data and R_VX1_CRC_ENn = 0x1. n=0, 1)
0x1712	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTR_CSI0_0	2	R	-	Interrupt to INT0 [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x1: error status
0x1713	[7]	reserved	1	-	-	-
	[6:0]	R_INTR_CSI1_0	7	R	-	Interrupt to INT0 [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x1: error status
0x1714	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTR_BDC2Q0_0	2	R	-	Interrupt to INT0 [1] Internal Register AutoCheckSum error flag [0] Reserved 0x1: error status
0x1715	[7:0]	R_INTR_BDC2Q1_0	8	R	-	Interrupt to INT0 [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x1: detection flag
0x1716	[7:4]	R_INTR_BDC2Q2_0	4	R	-	Interrupt to INT0 [5] Sub-Link protocol error for Lane1 (*) [4] Sub-Link protocol error for Lane0 (*) [7][6] Reserved 0x1: error status (* this interrupt is valid when R_SLINK_EN = 0x1 and R_SLINK_PDN = 0x1)
	[3:0]	R_INTR_DSHNDLR1_0	4	R	-	Interrupt to INT0 [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x1: error status
0x1717	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x1718	[7:0]	R_INTR_MLRX0_1	8	R	-	Interrupt to INT1 [5] Main-Link protocol error for Lane1 in normal operation (when LOCKN1=L) [4] Main-Link protocol error for Lane0 in normal operation (when LOCKN0=L) [1] Main-Link RX LOCKN=L to H detection flag for Lane1 (*) [0] Main-Link RX LOCKN=L to H detection flag for Lane0 (*) [7][6][3][2] Reserved 0x1: error status or detection flag (* this interrupt registers become 1 once after startup)
0x1719	[7:6]	R_INTR_MODE0_1	2	R	-	Interrupt to INT1 [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x1: detection flag
	[5:4]	R_INTR_DSHNDR0_1	2	R	-	Interrupt to INT1 [5] Data Stream Handler Distribution error [4] Reserved 0x1: error status
	[3:0]	R_INTR_FMT0_1	4	R	-	Interrupt to INT1 [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L)(*) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L)(*) [3][2] Reserved 0x1: error status (* this interrupt is valid when Main-Link stream contains CRC data and R_VX1_CRC_ENn = 0x1. n=0, 1)
0x171A	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTR_CSI0_1	2	R	-	Interrupt to INT1 [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x1: error status
0x171B	[7]	reserved	1	-	-	-
	[6:0]	R_INTR_CSI1_1	7	R	-	Interrupt to INT1 [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x1: error status
0x171C	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTR_BDC2Q0_1	2	R	-	Interrupt to INT1 [1] Internal Register AutoCheckSum error flag [0] Reserved 0x1: error status
0x171D	[7:0]	R_INTR_BDC2Q1_1	8	R	-	Interrupt to INT1 [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x1: detection flag
0x171E	[7:4]	R_INTR_BDC2Q2_1	4	R	-	Interrupt to INT1 [5] Sub-Link protocol error for Lane1 (*) [4] Sub-Link protocol error for Lane0 (*) [7][6] Reserved 0x1: error status (* this interrupt is valid when R_SLINK_EN = 0x1 and R_SLINK_PDN = 0x1)
	[3:0]	R_INTR_DSHNDR1_1	4	R	-	Interrupt to INT1 [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x1: error status
0x171F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x1720	[7:0]	R_INTC_MLRX0_0	8	W	-	Interrupt Clear for INTO [5] Main-Link protocol error for Lane1 in normal operation (when LOCKN1=L) [4] Main-Link protocol error for Lane0 in normal operation (when LOCKN0=L) [1] Main-Link RX LOCKN=L to H detection flag for Lane1 [0] Main-Link RX LOCKN=L to H detection flag for Lane0 [7][6][3][2] Reserved 0x1: clear error status or detection flag
0x1721	[7:6]	R_INTC_MODE0_0	2	W	-	Interrupt Clear for INTO [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x1: clear detection flag
	[5:4]	R_INTC_DSHNDLR0_0	2	W	-	Interrupt Clear for INTO [5] Data Stream Handler Distribution error [4] Reserved 0x1: clear error status
	[3:0]	R_INTC_FMT0_0	4	W	-	Interrupt Clear for INTO [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L) [3][2] Reserved 0x1: clear error status
0x1722	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTC_CSI0_0	2	W	-	Interrupt Clear for INTO [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x1: clear error status
0x1723	[7]	reserved	1	-	-	-
	[6:0]	R_INTC_CSI1_0	7	W	-	Interrupt Clear for INTO [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x1: clear error status
0x1724	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTC_BDC2Q0_0	2	W	-	Interrupt Clear for INTO [1] Internal Register AutoCheckSum error flag [0] Reserved 0x1: clear error status
0x1725	[7:0]	R_INTC_BDC2Q1_0	8	W	-	Interrupt Clear for INTO [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x1: clear detection flag
0x1726	[7:4]	R_INTC_BDC2Q2_0	4	W	-	Interrupt Clear for INTO [5] Sub-Link protocol error for Lane1 [4] Sub-Link protocol error for Lane0 [7][6] Reserved 0x1: clear error status
	[3:0]	R_INTC_DSHNDLR1_0	4	W	-	Interrupt Clear for INTO [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x1: clear error status
0x1727	[7:0]	reserved	8	-	-	-



Address	bit	Register Name	width	R/W	init	Description
0x1728	[7:0]	R_INTC_MLRX0_1	8	W	-	Interrupt Clear for INT1 [5] Main-Link protocol error for Lane1 in normal operation (when LOCKN1=L) [4] Main-Link protocol error for Lane0 in normal operation (when LOCKN0=L) [1] Main-Link RX LOCKN=L to H detection flag for Lane1 [0] Main-Link RX LOCKN=L to H detection flag for Lane0 [7][6][3][2] Reserved 0x1: clear error status or detection flag
0x1729	[7:6]	R_INTC_MODE0_1	2	W	-	Interrupt Clear for INT1 [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x1: clear detection flag
	[5:4]	R_INTC_DSHNDLR0_1	2	W	-	Interrupt Clear for INT1 [5] Data Stream Handler Distribution error [4] Reserved 0x1: clear error status
	[3:0]	R_INTC_FMT0_1	4	W	-	Interrupt Clear for INT1 [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L) [3][2] Reserved 0x1: clear error status
0x172A	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTC_CSI0_1	2	W	-	Interrupt Clear for INT1 [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x1: clear error status
0x172B	[7]	reserved	1	-	-	-
	[6:0]	R_INTC_CSI1_1	7	W	-	Interrupt Clear for INT1 [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x1: clear error status
0x172C	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTC_BDC2Q0_1	2	W	-	Interrupt Clear for INT1 [1] Internal Register AutoCheckSum error flag [0] Reserved 0x1: clear error status
0x172D	[7:0]	R_INTC_BDC2Q1_1	8	R	-	Interrupt Clear for INT1 [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x1: clear detection flag
0x172E	[7:4]	R_INTC_BDC2Q2_1	4	W	-	Interrupt Clear for INT1 [5] Sub-Link protocol error for Lane1 [4] Sub-Link protocol error for Lane0 [7][6] Reserved 0x1: clear error status
	[3:0]	R_INTC_DSHNDLR1_1	4	W	-	Interrupt Clear for INT1 [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x1: clear error status
0x172F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x1730	[7:0]	R_INTM_MLRX0_0	8	R/W	8'h00	Interrupt Mask for INTO [5] Main-Link protocol error for Lane1 in normal operation (when LOCKN1=L) [4] Main-Link protocol error for Lane0 in normal operation (when LOCKN0=L) [1] Main-Link RX LOCKN=L to H detection flag for Lane1 [0] Main-Link RX LOCKN=L to H detection flag for Lane0 [7][6][3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1731	[7:6]	R_INTM_MODE0_0	2	R/W	2'h0	Interrupt Mask for INTO [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
	[5:4]	R_INTM_DSHDLR0_0	2	R/W	2'h0	Interrupt Mask for INTO [5] Data Stream Handler Distribution error [4] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
	[3:0]	R_INTM_FMT0_0	4	R/W	4'h0	Interrupt Mask for INTO [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L) [3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1732	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTM_CSI0_0	2	R/W	2'h0	Interrupt Mask for INTO [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1733	[7]	reserved	1	-	-	-
	[6:0]	R_INTM_CSI1_0	7	R/W	7'h00	Interrupt Mask for INTO [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1734	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTM_BDC2Q0_0	2	R/W	2'h0	Interrupt Mask for INTO [1] Internal Register AutoChecksum error flag [0] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1735	[7:0]	R_INTM_BDC2Q1_0	8	R/W	8'h00	Interrupt Mask for INTO [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1736	[7:4]	R_INTM_BDC2Q2_0	4	R/W	4'h0	Interrupt Mask for INTO [5] Sub-Link protocol error for Lane1 [4] Sub-Link protocol error for Lane0 [7][6] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
	[3:0]	R_INTM_DSHDLR1_0	4	R/W	4'h0	Interrupt Mask for INTO [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INTO pin
0x1737	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x1738	[7:0]	R_INTM_MLRX0_1	8	R/W	8'h00	Interrupt Mask for INT1 [5] Main-Link protocol error for Lane1 [4] Main-Link protocol error for Lane0 [1] Main-Link RX LOCKN=L to H detection flag for Lane1 [0] Main-Link RX LOCKN=L to H detection flag for Lane0 [7][6][3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x1739	[7:6]	R_INTM_MODE0_1	2	R/W	2'h0	Interrupt Mask for INT1 [7] Vsync synchronization OK flag of all lanes [6] All Main-Link RX LOCKN=H detection flag 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
	[5:4]	R_INTM_DSHNDLR0_1	2	R/W	2'h0	Interrupt Mask for INT1 [5] Data Stream Handler Distribution error [4] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
	[3:0]	R_INTM_FMT0_1	4	R/W	4'h0	Interrupt Mask for INT1 [1] Main-Link RX CRC error for Lane1 in normal operation (when LOCKN1=L) [0] Main-Link RX CRC error for Lane0 in normal operation (when LOCKN0=L) [3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173A	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTM_CSI0_1	2	R/W	2'h0	Interrupt Mask for INT1 [1] MIPI CSI-2 status error for port1 [0] MIPI CSI-2 status error for port0 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173B	[7]	reserved	1	-	-	-
	[6:0]	R_INTM_CSI1_1	7	R/W	7'h00	Interrupt Mask for INT1 [6] MIPI CSI-2 general error [5][4][3][2][1][0] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173C	[7:2]	reserved	6	-	-	-
	[1:0]	R_INTM_BDC2Q0_1	2	R/W	2'h0	Interrupt Mask for INT1 [1] Internal Register AutoChecksum error flag [0] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173D	[7:0]	R_INTM_BDC2Q1_1	8	R/W	8'h00	Interrupt Mask for INT1 [5] Sub-Link Slave side 2-wire access complete flag for Lane1 [4] Sub-Link Slave side 2-wire access complete flag for Lane0 [1] Sub-Link Slave side interrupt detection flag for Lane1 [0] Sub-Link Slave side interrupt detection flag for Lane0 [7][6][3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173E	[7:4]	R_INTM_BDC2Q2_1	4	R/W	4'h0	Interrupt Mask for INT1 [5] Sub-Link protocol error for Lane1 [4] Sub-Link protocol error for Lane0 [7][6] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
	[3:0]	R_INTM_DSHNDLR1_1	4	R/W	4'h0	Interrupt Mask for INT1 [1] Data Stream Handler error2 for Lane1 [0] Data Stream Handler error2 for Lane0 [3][2] Reserved 0x0: mask interrupt factor 0x1: apply interrupt factor to INT1 pin
0x173F	[7:0]	reserved	8	-	-	-

Other registers (Read only registers, etc)

Address	bit	Register Name	width	R/W	init	Description
0x1740	[7:2]	reserved	6	-	-	-
	[1:0]	VX1_BETOUT	2	R	-	Main-Link Field-BET Result  <0x1740[1] register is valid only when 0x1035[1]=0x1> [1]:Main-Link Lane1 Field-BET Latched Result  <0x1740[0] register is valid only when 0x1035[0]=0x1> [0]:Main-Link Lane0 Field-BET Latched Result
0x1741	[7:2]	reserved	6	-	-	-
	[1:0]	VX1_CLK_SEL	2	R	-	Current selected Main-Link Master Clock Lane for PLL Source Clock 0x0:Main-Link Lane0 Clock is Master for PLL Source Clock 0x1:Main-Link Lane1 Clock is Master for PLL Source Clock Others: Reserved
0x1742	[7]	reserved	1	-	-	-
	[6:4]	LEQOC0	3	R	-	<this register is valid only when 0x1010[0]=0x1> V-by-One® Main-Link Equalizer strength Control Observation (for Lane0) 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3:0]	reserved	4	-	-	-
0x1743	[7]	reserved	1	-	-	-
	[6:4]	LEQOC1	3	R	-	<this register is valid only when 0x1014[0]=0x1> V-by-One® Main-Link Equalizer strength Control Observation (for Lane1) 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3:0]	reserved	4	-	-	-
0x1744	[7:0]	reserved	8	-	-	-
0x1745	[7:0]	reserved	8	-	-	-
0x1746	[7:0]	reserved	8	-	-	-
0x1747	[7:0]	reserved	8	-	-	-
0x1748	[7:0]	reserved	8	-	-	-
0x1749	[7:0]	reserved	8	-	-	-
0x174A	[7:0]	reserved	8	-	-	-
0x174B	[7:0]	reserved	8	-	-	-
0x174C	[7:0]	reserved	8	-	-	-
0x174D	[7:0]	reserved	8	-	-	-
0x174E	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	init	Description
0x174F	[7:6]	reserved	2	-	-	-
	[5:4]	R_MLINK_CRC_ERRCLR	2	W	-	Main-Link CRC Error Counter Clear  <0x174F[5] register is valid only when 0x1201[0]=0x1> [5] Main-Link CRC Error Counter Clear for Lane1 0x1: Clear  <0x174F[4] register is valid only when 0x1101[0]=0x1> [4] Main-Link CRC Error Counter Clear for Lane0 0x1: Clear
	[3:2]	reserved	2	-	-	-
	[1:0]	R_MLINK_BET_ERRCLR	2	W	-	Main-Link BET Error Counter Clear  <0x174F[1] register is valid only when 0x1035[1]=0x1> [1] Main-Link BET Error Counter Clear for Lane1 0x1: Clear  <0x174F[0] register is valid only when 0x1035[0]=0x1> [0] Main-Link BET Error Counter Clear for Lane0 0x1: Clear
0x1750	[7:0]	MLINK0_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1101[0]=0x1> Main-Link(Lane0) CRC Error Number (Upper Byte)
0x1751	[7:0]	MLINK0_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1101[0]=0x1> Main-Link(Lane0) CRC Error Number (Lower Byte)
0x1752	[7:0]	MLINK1_CRC_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1201[0]=0x1> Main-Link(Lane1) CRC Error Number (Upper Byte)
0x1753	[7:0]	MLINK1_CRC_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1201[0]=0x1> Main-Link(Lane1) CRC Error Number (Lower Byte)
0x1754	[7:0]	reserved	8	-	-	-
0x1755	[7:0]	reserved	8	-	-	-
0x1756	[7:0]	reserved	8	-	-	-
0x1757	[7:0]	reserved	8	-	-	-
0x1758	[7:0]	MLINK0_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[0]=0x1> Main-Link(Lane0) BET Error Number (Upper Byte)
0x1759	[7:0]	MLINK0_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[0]=0x1> Main-Link(Lane0) BET Error Number (Lower Byte)
0x175A	[7:0]	MLINK1_BET_ERRNUM[15:8]	8	R	-	<this register is valid only when 0x1035[1]=0x1> Main-Link(Lane1) BET Error Number (Upper Byte)
0x175B	[7:0]	MLINK1_BET_ERRNUM[7:0]	8	R	-	<this register is valid only when 0x1035[1]=0x1> Main-Link(Lane1) BET Error Number (Lower Byte)
0x175C	[7:0]	reserved	8	-	-	-
0x175D	[7:0]	reserved	8	-	-	-
0x175E	[7:0]	reserved	8	-	-	-
0x175F	[7:0]	reserved	8	-	-	-

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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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