THCS252

20-bits GPIO or high speed Bus signal Transceiver

General description

The THCS252 integrates Serializer and Deserializer onto a single chip, which supports general purpose input and output (GPIO) signals through two pairs of differential signal.

GPIO sampling clock is selectable from external reference clock or internal oscillator clock.

The 8B10B encoding and decoding adopted by THCS252 is easy to connect to optical / wireless communication devices with high robustness and DC balanced signal.

The built-in adaptive equalizer enables flexible cable selection.

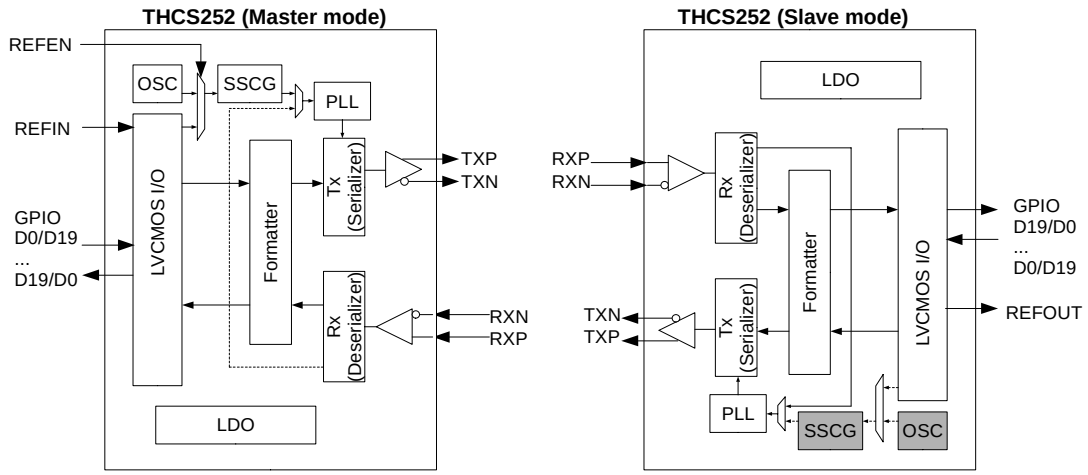
Application

The THCS252 can applicable to any systems which have many control signals between PCBs, for example Multi-function printers, Amusement machines, Factory Automation and TVs.

Features

- Support up to 20-bits GPIO
- Not required to input GPIO sampling clock in internal oscillator clock mode
- Full duplex communication by two pairs of differential signal
- Output buffer open-drain or push-pull selectable
- Support up to 8-bits low speed GPIO in low power Standby mode
- Integrated adaptive equalizer for long or lossy media
- 8B10B encoding and decoding
- Configurable digital noise filter
- Error detection and indication
- External reference clock frequency: 15-100MHz
- Spread Spectrum Clock Generator to reduce EMI
- Operating single power supply voltage: 1.7 V - 3.6 V
- Wide range IO voltage: 1.7V - 3.6V
- Operating temperature: -40°C to 85°C

Block diagram



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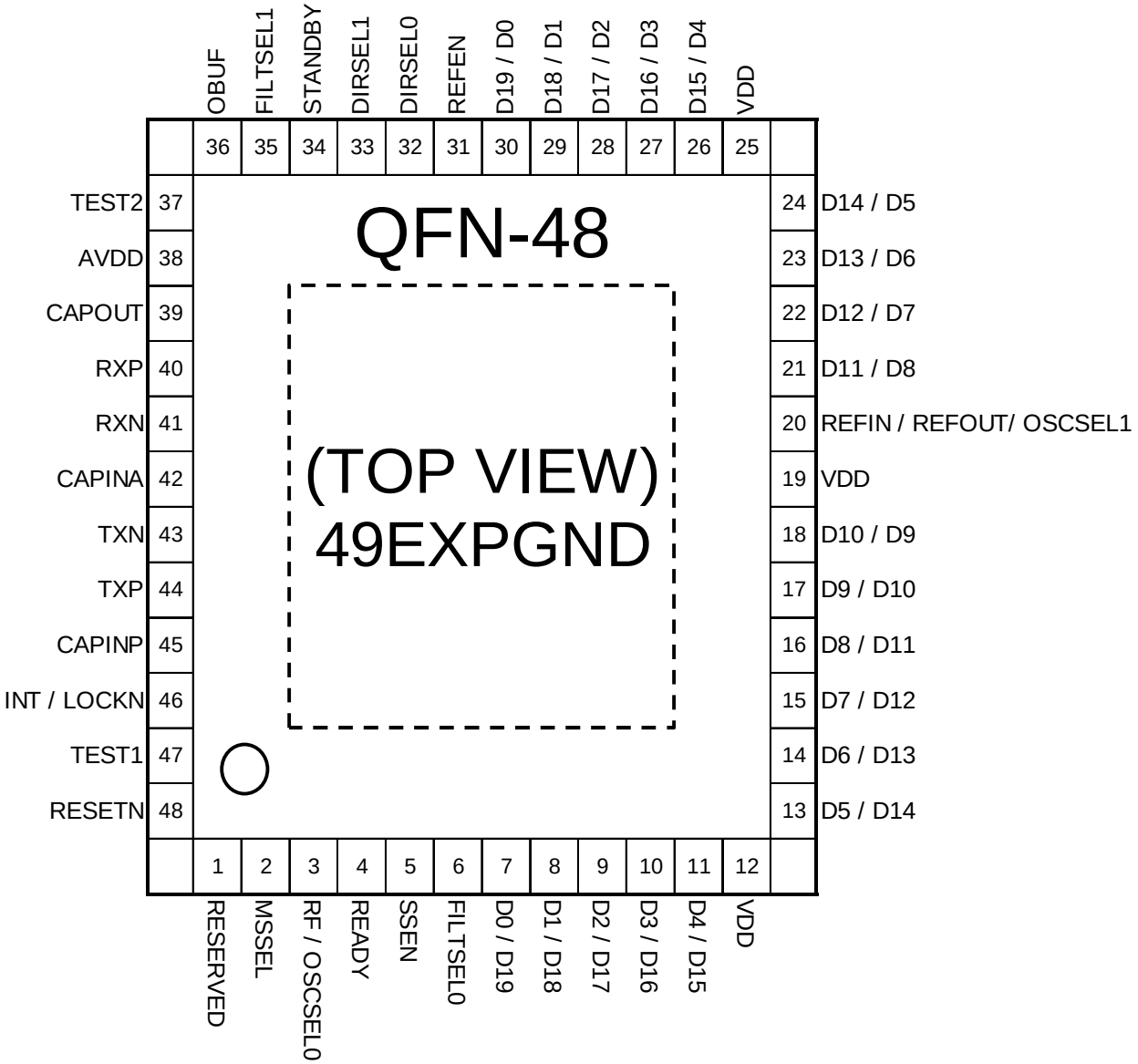
1. **Pin configuration**



2. Pin description

Pin Name	Pin No.	Type	Description	Reference
TXP	44	CO	High-speed CML signal output	-
TXN	43	CO	High-speed CML signal output	-
RXP	40	CI	High-speed CML signal input	-
RXN	41	CI	High-speed CML signal input	-
RESETN	48	IL	Chip reset 0: Chip reset 1: Chip operation	-
STANDBY	34	IL	Standby mode entry 0:Normal mode operation 1:Standby mode operation	-
MSSEL	2	IL	Master/Slave mode select 0: Master mode 1: Slave mode	-
FILTSEL1	35	IL	digital noise filter select	Table 5
DIRSEL0	32	IL	DIRSEL0: GPIO direction select	Table 2 Table 4
DIRSEL1	33	IL	DIRSEL1: GPIO direction select	Table 2 Table 4
OBUF	36	IL	Output buffer type select 0: open-drain 1: push-pull	-
REFEN	31	IL	Data sampling clock select (Master mode) 0: Internal oscillator clock 1: External reference clock	-
			CDR clock output enable (Slave mode) 0: REFOUT pin is Hi-Z state 1: CDR clock output from REFOUT pin	-
REFIN/ REFOUT/ OSCSEL1	20	B	REFIN: (Master mode) External Reference clock input	-
			REFOUT: (Slave mode) CDR clock output	-
			OSCSEL1: (Master mode) Oscillator clock frequency select	Table 9
			OSCSEL1: (Slave mode) Hi-Z	-
RF/ OSCSEL0	3	IL	RF:(Master mode) input clock edge select	Table 10 Figure 14
			RF: (Slave mode) output clock edge select	
			OSCSEL0:(Master mode) Oscillator clock frequency select	Table 9
			OSCSEL0: (Slave mode) Set to Low	
D0/ D19	7	BT	D0(Master mode): Data input	-
			D19(Slave mode): Data output	-

Pin Name	Pin No.	Type	Description	Reference
D1/ D18	8	BT	D1(Master mode): Data input D18(Slave mode): Data output	- -
D2/ D17	9	BT	D2(Master mode): Data input D17(Slave mode): Data output	- -
D3/ D16	10	BT	D3(Master mode): Data input D16(Slave mode): Data output	- -
D4/ D15	11	B	D4(Master mode): Data input D15(Slave mode): Data output	- -
D5/ D14	13	B	D5(Master mode): Data input D14(Slave mode): Data output	- -
D6/ D13	14	B	D6(Master mode): Data input D13(Slave mode): Data output	- -
D7/ D12	15	B	D7(Master mode): Data input D12(Slave mode): Data output	- -
D8/ D11	16	B	D8(Master mode): Data input D11(Slave mode): Data output	- -
D9/ D10	17	B	D9(Master mode): Data input D10(Slave mode): Data output	- -
D10/ D9	18	B	D10(Master mode): Data input/output D9(Slave mode): Data input/output	- -
D11/ D8	21	B	D11(Master mode): Data input/output D8(Slave mode): Data input/output	- -
D12/ D7	22	B	D12(Master mode): Data input/output D7(Slave mode): Data input/output	- -
D13/ D6	23	B	D13(Master mode): Data input/output D6(Slave mode): Data input/output	- -
D14/ D5	24	B	D14(Master mode): Data input/output D5(Slave mode): Data input/output	- -
D15/ D4	26	B	D15(Master mode): Data input/output D4(Slave mode): Data input/output	- -
D16/ D3	27	BT	D16(Master mode): Data input/output D3(Slave mode): Data input/output	- -
D17/ D2	28	BT	D17(Master mode): Data input/output D2(Slave mode): Data output	- -
D18/ D1	29	BT	D18(Master mode): Data output D1(Slave mode): Data input	- -
D19/ D0	30	BT	D19(Master mode): Data input/output D0(Slave mode): Data input/output	- -
SSEN	5	BL	SSEN(Master mode): SSCG PLL enable 0: SSCG PLL is disabled 1: SSCG PLL is enabled SSEN(Slave mode): Set to Low	-
FILTSEL0	6	BL	FILTSEL0: digital noise filter select	Table 5
INT/ LOCKN	46	BO	INT: Interrupt output when READY=1 0: Error occurred 1(pull-up): No Error	-

Pin Name	Pin No.	Type	Description	Reference
			LOCKN(Master mode): Lock detect input 0: Lock state 1(pull-up): Unlock state	-
			LOCKN(Slave mode): Lock detect output 0: Lock state 1(pull-up): Unlock state	-
READY	4	B	CML Link communication status 0: Unlock state 1: Lock state	-
TEST1	47	IL	TEST1 shall be tied to Ground.	-
TEST2	37	AI	TEST2 shall be tied to Ground.	-
CAPOUT	39	PWR	Decoupling capacitor Pin, 1.2V output.	Figure 9
CAPINA	42	PWR	1.2V Analog power supply input.	Figure 9
CAPINP	45	PWR	1.2V Analog power supply input.	Figure 9
VDD	12 19 25	PWR	1.7-3.6V Digital power supply input for LVCMOS I/O.	-
AVDD	38	PWR	1.7-3.6V Analog power supply input for on-chip regulator.	Figure 9
EXPGND	49	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.	-

Pin Type definition

Analog Buffer
CO : CML Output buffer
CI : CML Input buffer
AI : Analog Input buffer

LVCMOS buffer
IL : Low speed schmitt trigger LVCMOS Input buffer
B : LVCMOS Bi-directional buffer
BO : Open-drain LVCMOS Bi-directional buffer
BL : Low speed 5V tolerant schmitt trigger LVCMOS Bi-directional buffer
BT : Low speed 5V tolerant LVCMOS Bi-directional buffer

Power/Ground
PWR : Power supply
GND : Ground

3. Absolute maximum ratings

Parameter	Min	Typ	Max	Unit
Supply voltage(VDD,AVDD)	-0.3	-	4.0	V
LVCMOS input voltage	-0.3	-	VDD+0.3	V
LVCMOS output voltage	-0.3	-	VDD+0.3	V
5V tolerant Bi-directional buffer input voltage	-0.3	-	VDD+2.5	V
5V tolerant Bi-directional buffer output voltage	-0.3	-	VDD+2.5	V
Open-drain output voltage	-0.3	-	4.0	V
CML receiver input voltage	-0.3	-	CAPINA+0.3	V
CML transmitter output voltage	-0.3	-	CAPINP+0.3	V
Output current	-50	-	50	mA
Storage temperature	-55	-	125	°C
Junction temperature	-	-	125	°C
Reflow peak temperature/time	-	-	260/10	°C/sec
Theta-ja (Junction-to-Ambient)	30.8 [*1]			°C/W
Psi-jt (Junction-to-Top of Package)	2.8 [*1]			°C/W
Maximum power dissipation @+25°C	3.2 [*1]			W

"Absolute maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

*1: Thermal parameters are not guaranteed value. This value assists board and system level designers

4. Recommended operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage(VDD,AVDD)	1.7	-	3.6	V
Operating ambient temperature	-40	-	85	°C

VDD and AVDD supply voltage shall be the same voltage.

5. Electrical characteristics

5.1. Current consumption

Symbol	Parameter	Pin Type	Condition	Min	Typ	Max	Unit
Idd_w1	Normal mode current Low current use case [*1]	PWR	AVDD=3.3V VDD=3.3V	-	80	-	mA
Idd_w2	Normal mode current High current use case [*2]	PWR	AVDD=3.3V VDD=3.3V	-	300	-	mA
Idda_stby	Standby mode current	PWR	AVDD=3.3V VDD=3.3V	-	4	-	mA
Idda_slp	Sleep mode current	PWR	AVDD=3.3V VDD=3.3V	-	3	-	mA
Idda_rst	Reset mode current	PWR	AVDD=3.3V VDD=3.3V	-	3	-	mA

PWR : Power supply
*1: Master mode of Unidirectional transmission mode, 20-bits GPIO input, 100MHz of REFIN clock
*2: Slave mode of Unidirectional transmission mode, 20-bits GPIO output, 100MHz of REFOUT clock

5.2. LVCMOS/Analog input DC specifications

Symbol	Parameter	Pin Type	Condition	Min	Typ	Max	Unit
VIH	High level input voltage	B,BT, BO	1.7V≦VDD<2.0V	0.65 VDD	-	VDD	V
			2.0V≦VDD<3.0V	0.70 VDD	-	VDD	V
			3.0V≦VDD≦3.6V	2.0	-	VDD	V
		IL,BL	1.7V≦VDD≦3.6V	0.70 VDD	-	VDD	V
VIL	Low level input voltage	B,BT, BO	1.7V≦VDD<2.0V	0	-	0.35 VDD	V
			2.0V≦VDD<3.0V	0	-	0.30 VDD	V
			3.0V≦VDD≦3.6V	0	-	0.8	V
		IL,BL	1.7V≦VDD≦3.6V	0	-	0.30 VDD	V
		AI	1.7V≦VDD≦3.6V	0	-	0.15 VDD	V
VOH	High level output voltage	B,BT, BL	1.7V≦VDD<2.0V IOH=-2mA	VDD - 0.30	-	VDD	V
			2.0V≦VDD≦3.6V IOH=-4mA	VDD - 0.45	-	VDD	V
VOL	Low level output voltage [*1]	B,BT, BL	1.7V≦VDD<2.0V IOL=2mA	0	-	0.30	V
			2.0V≦VDD≦3.6V IOL=4mA	0	-	0.45	V
		BO	1.7V≦VDD≦3.6V IOL=2mA	0	-	0.27	V
IIH	Input leak current high	IL	VIN=VDD	-10	-	10	uA
IIL	Input leak current low	IL	VIN=0V	-10	-	10	uA
IOZH	Output leak current high in Hi-Z state	B,BT, BL,BO	VIN=VDD	-10	-	10	uA
IOZL	Output leak current low in Hi-Z state	B,BT, BL,BO	VIN=0V	-10	-	10	uA

AI : Analog Input buffer
IL : Low speed schmitt trigger LVCMOS Input buffer
B : LVCMOS Bi-directional buffer
BO : Open-drain LVCMOS Bi-directional buffer
BL : Low speed 5V tolerant schmitt trigger LVCMOS Bi-directional buffer
BT : Low speed 5V tolerant LVCMOS Bi-directional buffer

5.3. LVCMOS AC characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
tRSN	RESETN low time	-		3	-	-	us
tTCIP	REFIN period	-		10	-	66.6	ns
tTCH	REFIN high time	-		0.35 tTCIP	0.5 tTCIP	0.65 tTCIP	ns
tTCL	REFIN low time	-		0.35 tTCIP	0.5 tTCIP	0.65 tTCIP	ns
tTS	Data input setup to REFIN	Pin type: B	1.7V≦VDD≦3.6V	2.0	-	-	ns
		Pin type: BT	1.7V≦VDD<2.25V	25	-	-	ns
			2.25V≦VDD≦2.75V	2.5	-	-	ns
			2.75V<VDD≦3.6V	2.0	-	-	ns
tTH	Data input hold to REFIN	-		1.0	-	-	ns
tTPD	Power on to RESETN high delay	-		0	-	-	ns
tOSC	Internal oscillator clock period	OSCSEL1=0 OSCSEL0=0		41.67	50	62.5	ns
		OSCSEL1=1 OSCSEL0=0		20.84	25	31.25	ns
		OSCSEL1=1 OSCSEL0=1		10.42	12.5	15.62	ns
tDCP	Data sampling clock period	REFEN=0		-	tOSC	-	ns
		REFEN=1		-	tTCIP	-	ns
tFLTCK	Noise filter clock period	REFEN=0		10.42	12.5	15.62	ns
		REFEN=1		-	tTCIP	-	ns
tTCD	Input data to output data delay (Master mode to Slave mode)	SSEN=0	FILTSEL1=0 FILTSEL0=0	12 tDCP	-	25 tDCP	ns
			FILTSEL1=0 FILTSEL0=1	19 tDCP	-	35 tDCP	ns
			FILTSEL1=1 FILTSEL0=0	24 tDCP	-	43 tDCP	ns
			FILTSEL1=1 FILTSEL0=1	34 tDCP	-	59 tDCP	ns
		SSEN=1	FILTSEL1=0 FILTSEL0=0	57 tDCP	-	110 tDCP	ns
			FILTSEL1=0 FILTSEL0=1	64 tDCP	-	120 tDCP	ns
			FILTSEL1=1 FILTSEL0=0	69 tDCP	-	128 tDCP	ns
			FILTSEL1=1 FILTSEL0=1	79 tDCP	-	144 tDCP	ns
tRCP	REFOUT period	-		-	tDCP	-	ns
tRCH	REFOUT high time	-		-	0.5 tDCP	-	ns
tRCL	REFOUT low time	-		-	0.5 tDCP	-	ns
tDOUT	Data output period	-		-	tDCP	-	ns
tRS	Data output setup to REFOUT	-		0.45 tDCP - 0.675	-	-	ns
tRH	Data output hold to REFOUT	-		0.45 tDCP - 2.175	-	-	ns
tRCD	Input data to output data delay (Slave mode to Master mode)	FILTSEL1=0 FILTSEL0=0		12 tDCP	-	25 tDCP	ns
		FILTSEL1=0 FILTSEL0=1		19 tDCP	-	35 tDCP	ns
		FILTSEL1=1 FILTSEL0=0		24 tDCP	-	43 tDCP	ns
		FILTSEL1=1 FILTSEL0=1		34 tDCP	-	59 tDCP	ns
tRRDY	RESETN high to READY high delay	-		0	-	10	ms

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tNRDY	STANDBY low to READY high delay	-	0	-	10	ms
tSRDY	STANDBY high to READY high delay	-	0	-	10	ms
tSSKW	STANDBY high of Master mode and Slave mode skew margin	-	-400	-	+400	us
tTLH	Clock and Data output low to high transition time	Clock	-	-	2.1	ns
		Data(Pin type=B)	-	-	4.2	ns
		Data(Pin type=BT)	-	-	5.9	ns
tTHL	Clock and data output high to low transition time	Clock	-	-	2.1	ns
		Data(Pin type=B)	-	-	4.3	ns
		Data(Pin type=BT)	-	-	6.1	ns

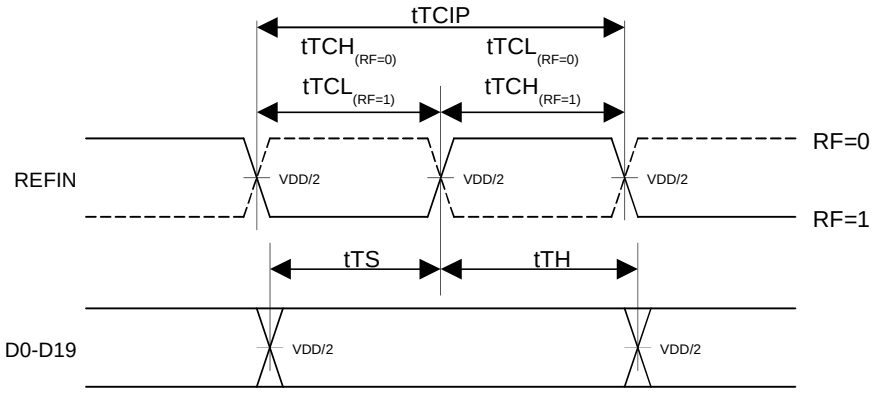


Figure 1 LVCMOS input timing diagram

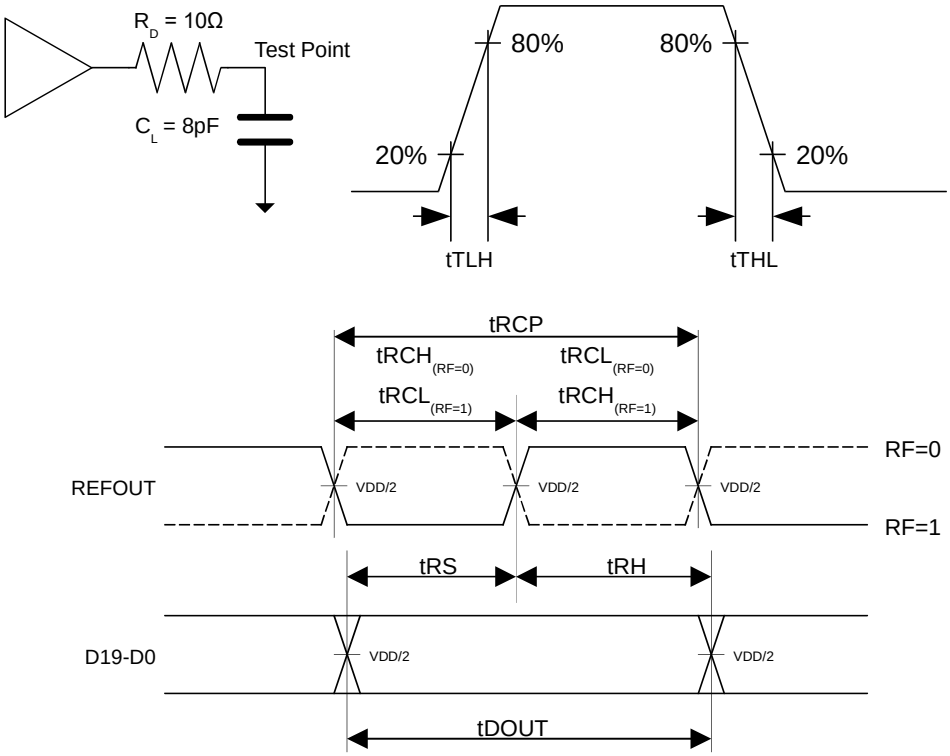


Figure 2 LVCMOS output timing diagram

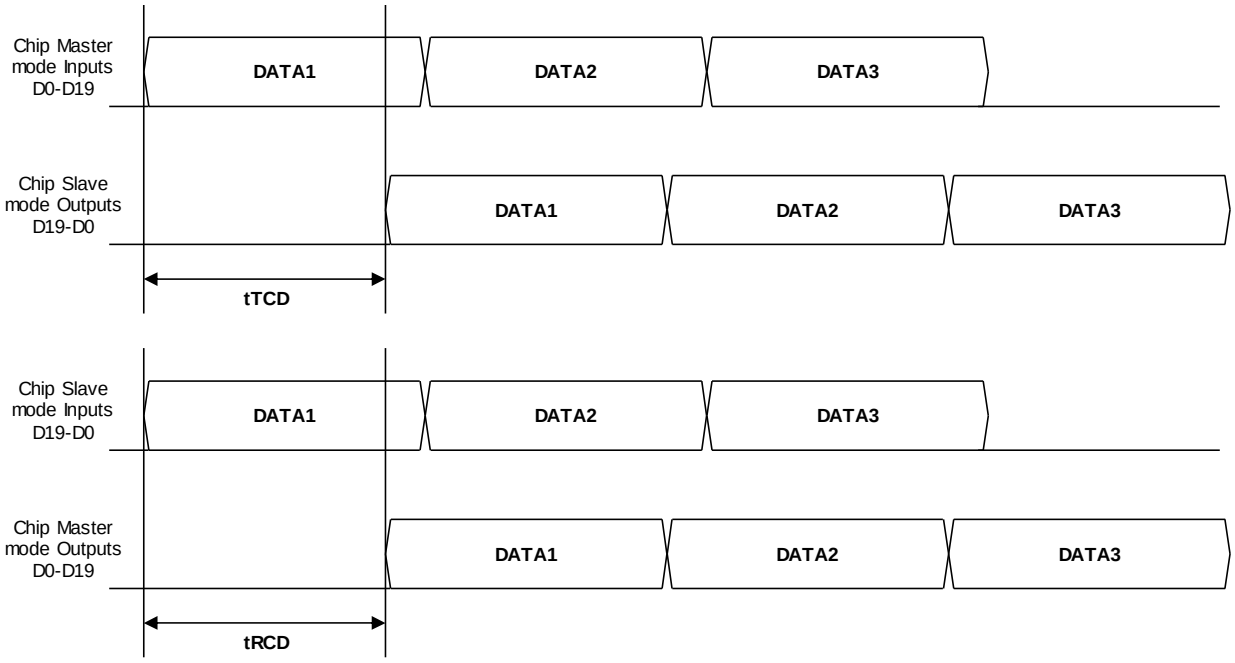


Figure 3 GPIO Input to Output delay timing diagram

5.4. CML DC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VTOD	CML differential output peak to peak signal	-	600	800	1000	mVpp
VTOC	CML common mode output voltage	-	-	1200 - 0.5 VTOD	-	mV
ITOH	CML output leak current high	RESETN=0 TXP/N=CAPINA	-30	-	30	uA
ITOS	CML output short current	RESETN=0 TXP/N=0V	-80	-	-	mA
VRTH	CML differential input high threshold	-	-	-	50	mV
VRTL	CML differential input low threshold	-	-50	-	-	mV
IRIH	CML input leak current high	RESETN=0 RXP/N=CAPINA	-10	-	10	uA
IRIL	CML input leak current low	RESETN=0 RXP/N=0V	-10	-	10	uA
IRRIH	CML input current high	RXP/N=CAPINA	-	-	2	mA
IRRIL	CML input current low	RXP/N=0V	-6	-	-	mA
RRIN	CML differential input resistance	-	80	100	120	Ω

5.5. CML AC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tTRF	CML output rise and fall time (20%-80%)	-	50	-	150	ps
tTPLL0	RESETN=1 to CML output delay	-	-	-	10	ms
tTPLL1	RESETN=0 to CML output high fix delay	-	-	-	500	ns
tTNP0	READY low to training pattern output delay	-	-	-	100	us
tTBIT	Output unit interval	-	-	tDCP÷30	-	ns
tRBIT	Input unit interval	-	250	-	2222	ps
tRPLL0	Training pattern input to LOCKN low delay	Unidirectional mode	-	-	10	ms
tRPLL1	RESETN low to LOCKN High delay	Unidirectional mode	-	-	10	us
tRLCK0	LOCKN low to data output delay	Unidirectional mode	-	-	5	ms

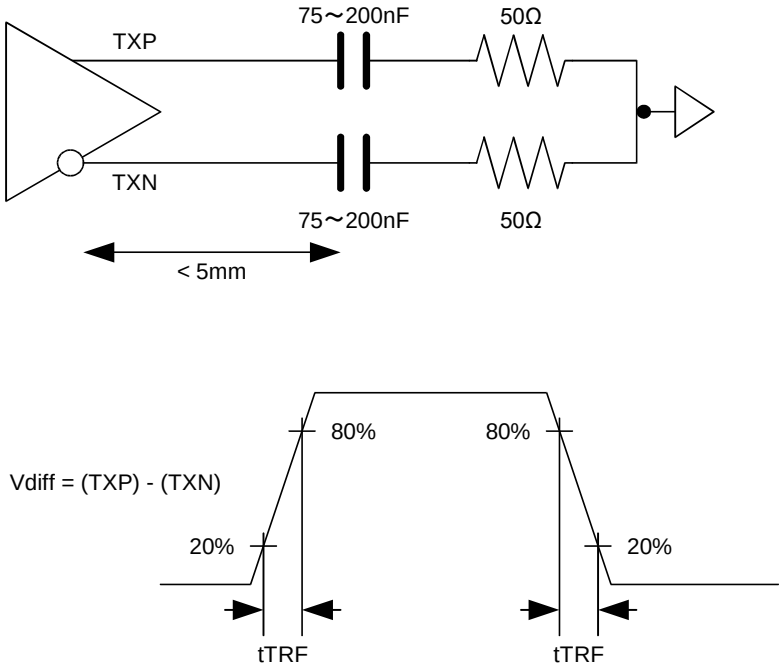


Figure 4 CML output AC characteristics diagram

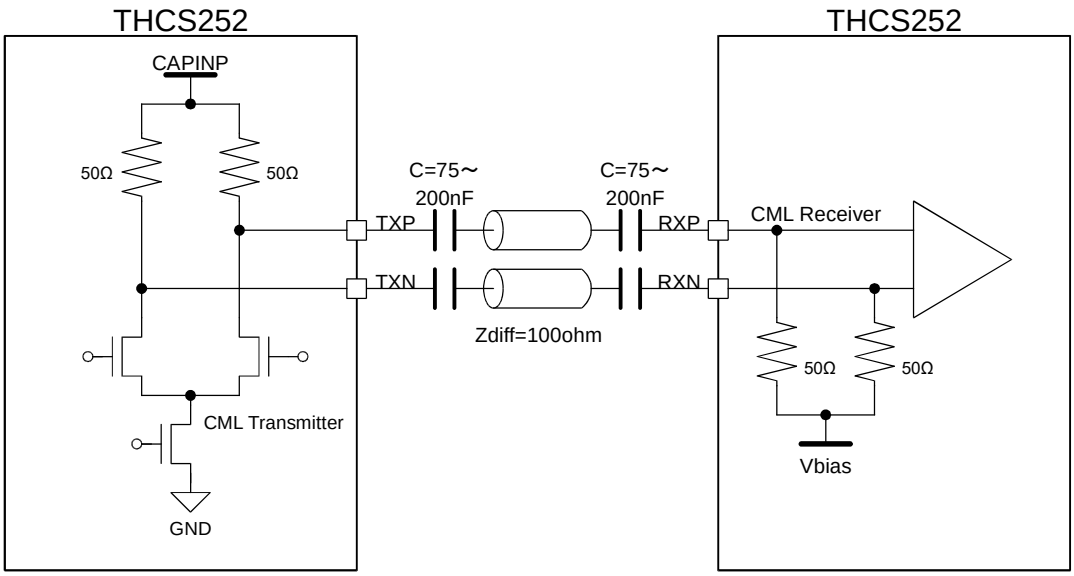
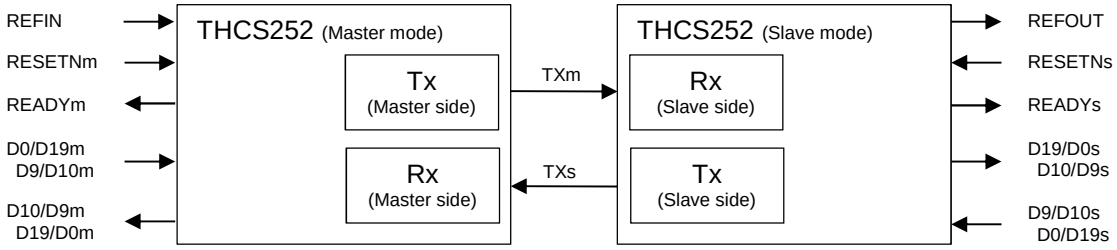


Figure 5 CML buffer equivalent circuit



DATA_WIDTH=0, DIRSEL1/0=00

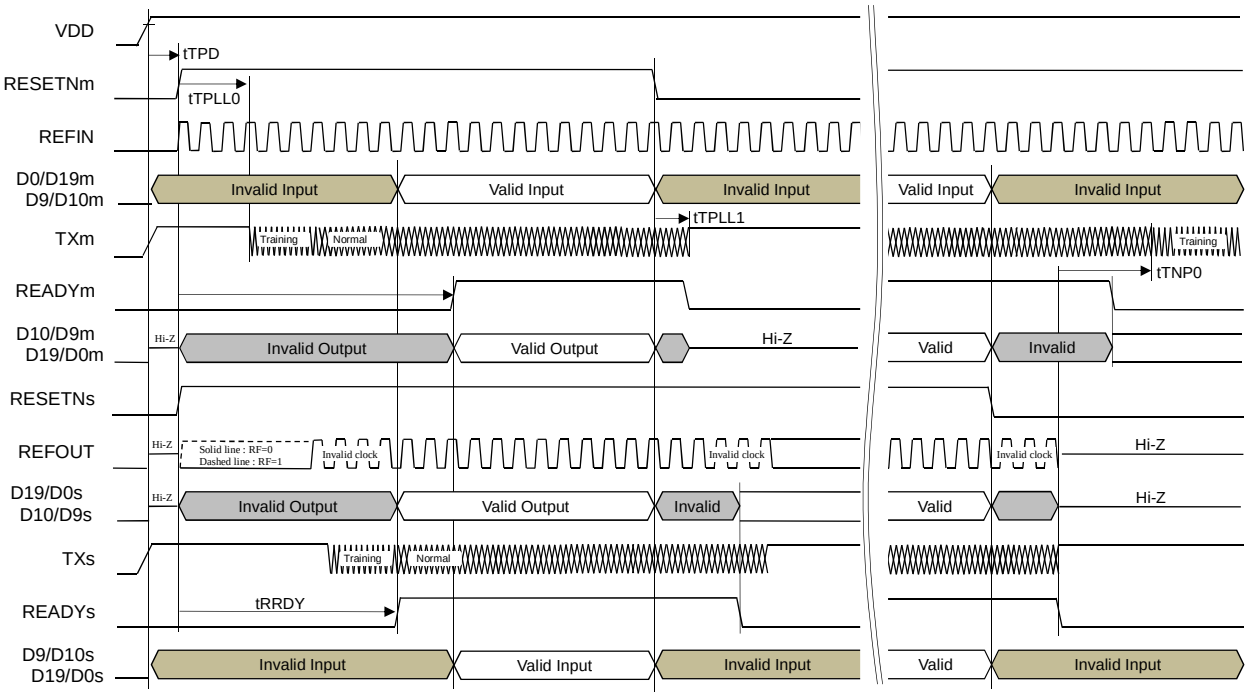


Figure 6 GPIO/CML Bi-directional mode Power on & Reset timing diagram

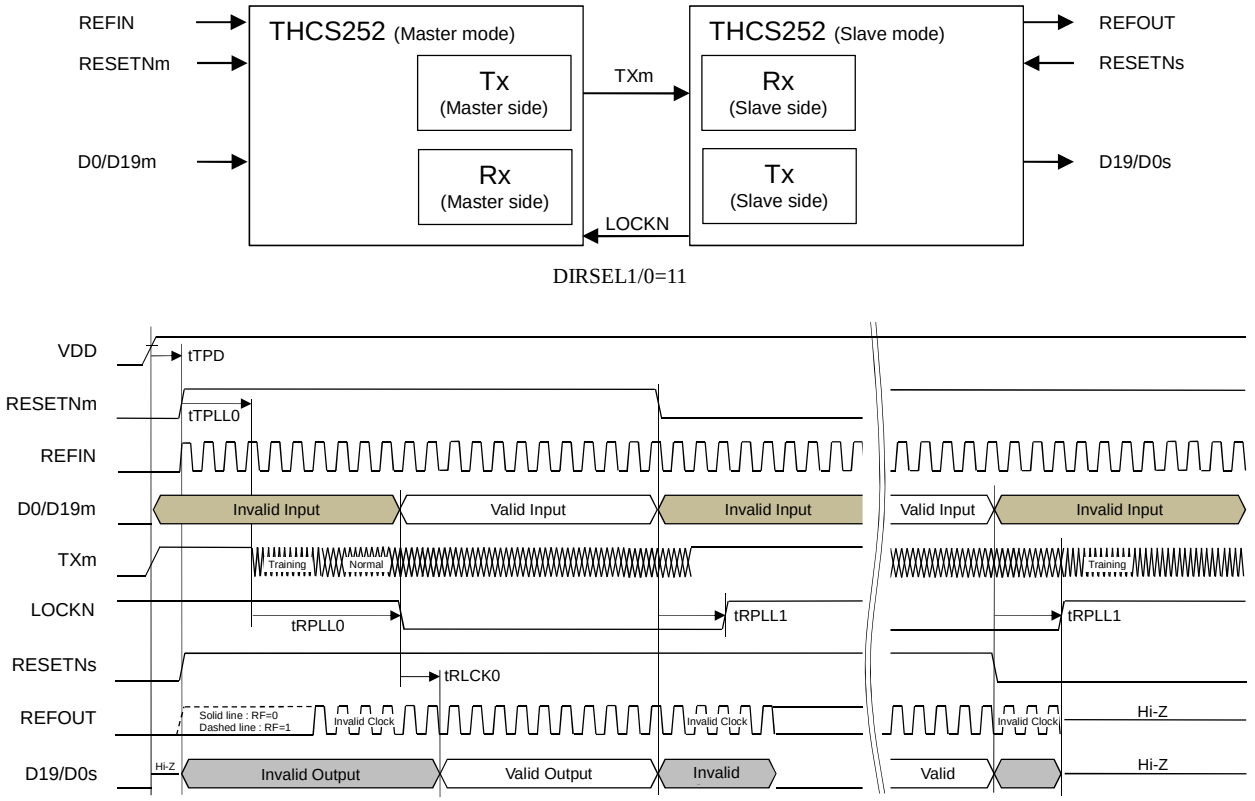


Figure 7 GPIO/CML Unidirectional mode lock & unlock timing diagram

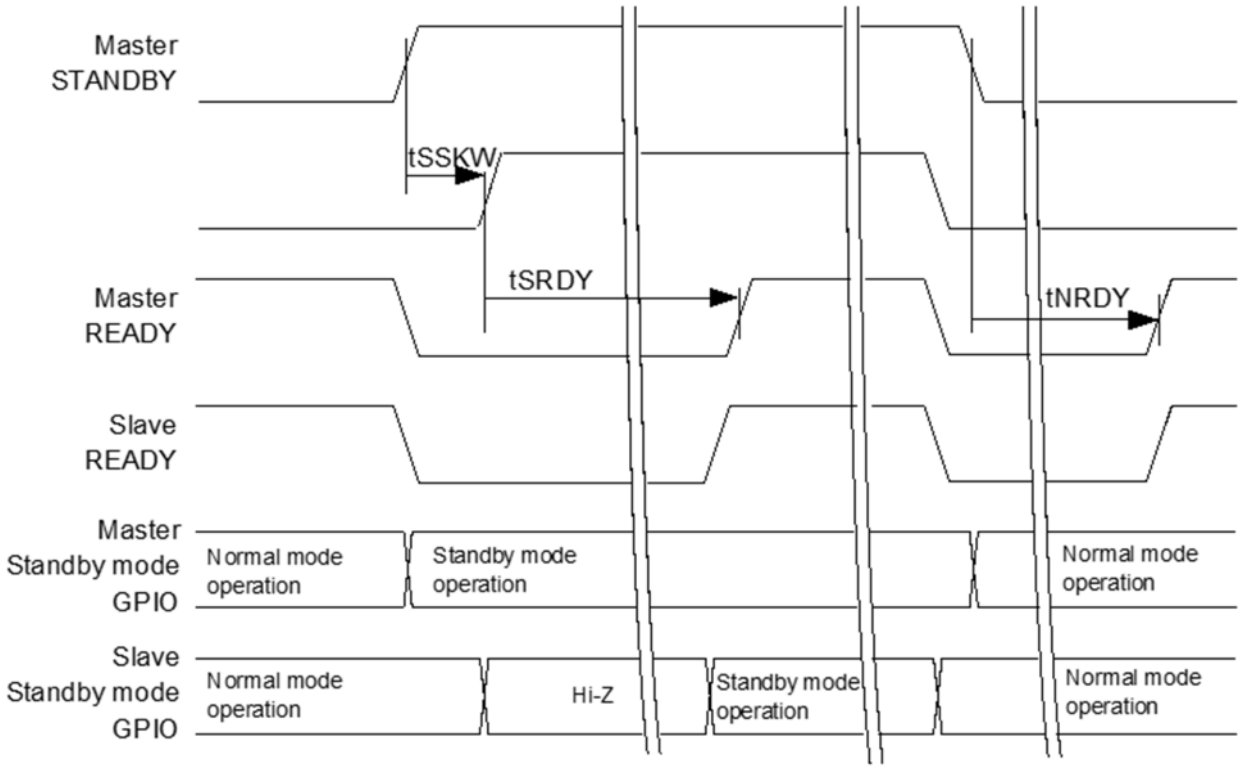
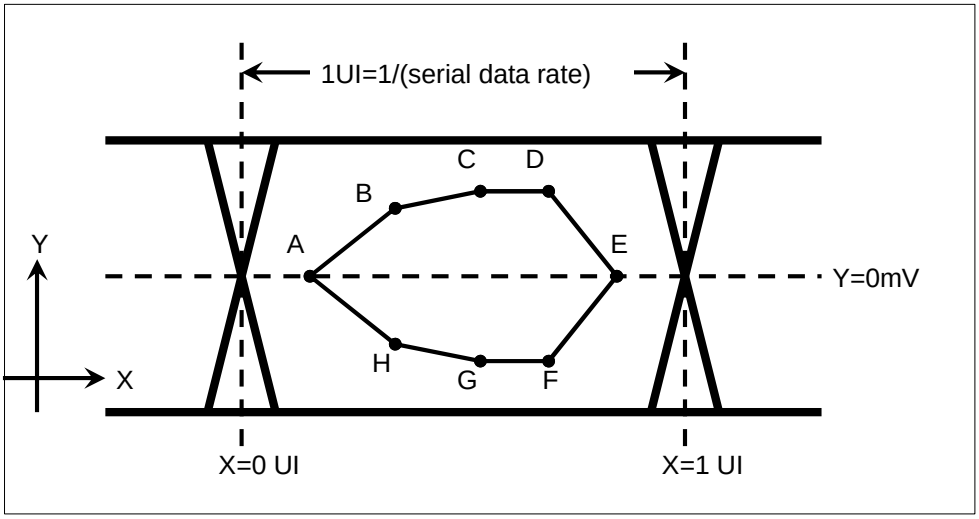


Figure 8 Standby mode timing diagram

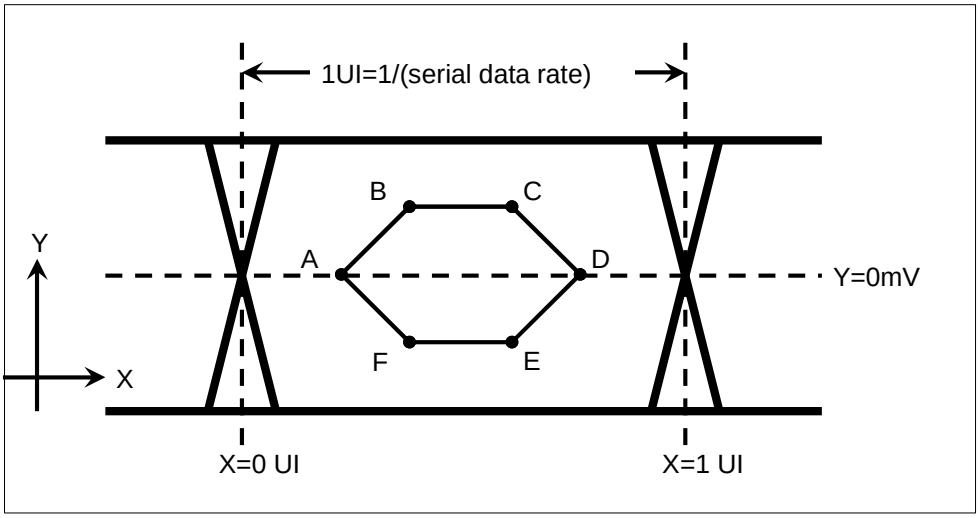
6. CML Line Eye diagrams

6.1. CML output Eye diagrams



	X[UI]	Y[mV]
A	0.15	0
B	0.355	140
C	0.5	175
D	0.645	175
E	0.85	0
F	0.645	-175
G	0.5	-175
H	0.355	-140

6.2. CML input Eye diagrams



	X[UI]	Y[mV]
A	0.25	0
B	0.3	50
C	0.7	50
D	0.75	0
E	0.7	-50
F	0.3	-50

7. Function

7.1. Functional overview

With high speed CML Serializer and Deserializer integrated onto a single chip, THCS252 enables Aggregation/Deaggregation up to 20-bits parallel General-Purpose I/O (GPIO) signal through full-duplex communication by two pairs of differential signal with minimal external components. THCS252 supports up to 8-bits low speed GPIO signal in low power Standby mode. It does not require any external clock generators e.g. a crystal oscillator. A pair of THCS252 enables to monitor and control peripheral devices via GPIOs. In case communication errors occur, they keep the GPIO signals and report by an interrupt signal.

7.2. Power supply

7.2.1. Internal regulator output/input function (CAPOUT, CAPINA, CAPINP)

An internal regulator produces 1.2V (CAPOUT) only for internal use. It shall not be used for any other external loads. Bypass CAPOUT to GND with 10uF as a power supply pin. Bypass AVDD to GND with >10uF.

CAPINP and CAPINA supply reference voltage for internal analog circuits. Bypass CAPINP/CAPINA to GND with 0.1uF as power supply pins to reduce high frequency noise. CAPOUT, CAPINA and CAPINP must be tied together as Figure 9.

It is recommended to place ferrite bead for AVDD pins to reduce noise as Figure 9.

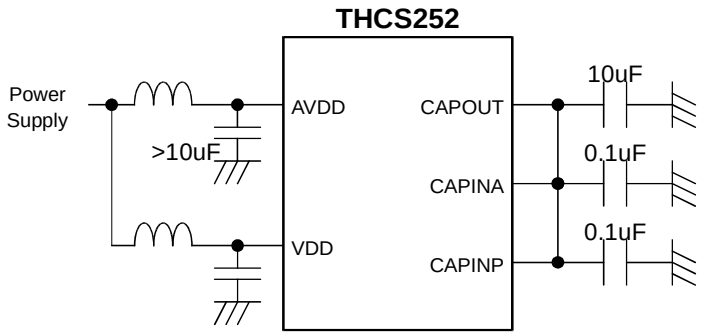


Figure 9 Connection of CAPOUT, CAPINA, CAPINP and decoupling capacitor

7.3. Operating mode

Table 1 shows operating mode setting.

Table 1 Operating mode setting

Operating mode	Setting		description
	RESETN	STANDBY	
Reset	0	-	Chip reset All outputs are Hi-Z
Normal	1	0	Normal operating mode
Standby	1	1	Low power and low frequency sampling rate transmission through up to 8-bits GPIO.

7.4. Transmission mode

THCS252 has a Bi-directional transmission mode with full-duplex communication and a Unidirectional communication mode.

7.4.1. Full duplex Bi-directional transmission mode

THCS252 can be used a pair of Master mode and Slave mode. Master mode samples data by external reference clock or internal oscillator clock. Slave mode samples data by CDR (Clock Data Recovery) clock generated by Rx. Same configuration of MSSEL between Master mode and Slave mode is prohibited. See Figure 10.

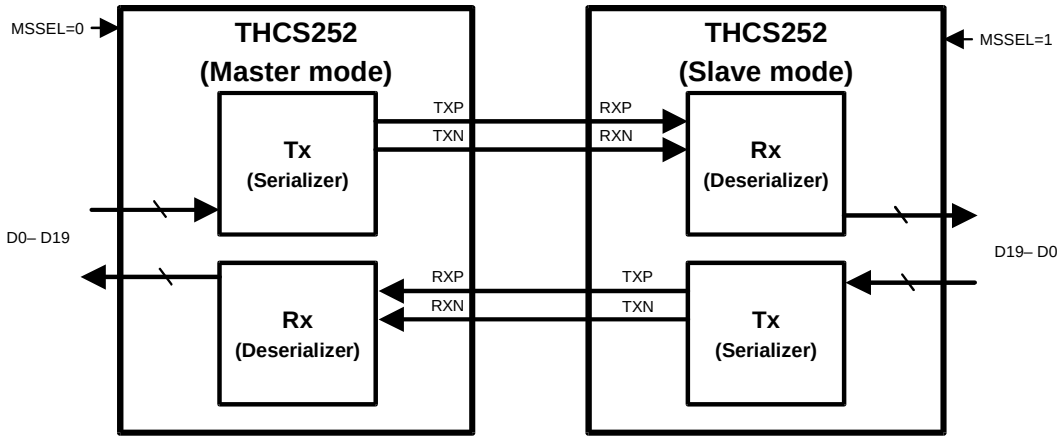


Figure 10 Setting for Bi-directional transmission mode

Table 2 Common setting of Master/Slave mode for Full duplex mode

Use case		A-1	A-2	A-3		
Setting	DIRSEL1, DIRSEL0	00	01	10		
Mode	Downstream bit count	10	14	18		
	Upstream bit count	10	6	2		
	CML line data rate	External reference clock mode: 1/tTCIP x 30 Internal oscillator clock mode: 1/tOSC x 30				
Data pin for Master mode	D0/D19	=>	=>	=>	D19/D0	Data pin for Slave mode
	D1/D18	=>	=>	=>	D18/D1	
	D2/D17	=>	=>	=>	D17/D2	
	D3/D16	=>	=>	=>	D16/D3	
	D4/D15	=>	=>	=>	D15/D4	
	D5/D14	=>	=>	=>	D14/D5	
	D6/D13	=>	=>	=>	D13/D6	
	D7/D12	=>	=>	=>	D12/D7	
	D8/D11	=>	=>	=>	D11/D8	
	D9/D10	=>	=>	=>	D10/D9	
	D10/D9	<=	=>	=>	D9/D10	
	D11/D8	<=	=>	=>	D8/D11	
	D12/D7	<=	=>	=>	D7/D12	
	D13/D6	<=	=>	=>	D6/D13	
	D14/D5	<=	<=	=>	D5/D14	
	D15/D4	<=	<=	=>	D4/D15	
	D16/D3	<=	<=	=>	D3/D16	
	D17/D2	<=	<=	=>	D2/D17	
	D18/D1	<=	<=	<=	D1/D18	
	D19/D0	<=	<=	<=	D0/D19	

"=>" means Downstream (GPIO input in Master mode and GPIO output in Slave mode).

"<=" means Upstream (GPIO input in Slave mode and GPIO output in Master mode).

Start communication after setting each "Use case" in both Master/Slave.

7.4.2. Unidirectional transmission mode

THCS252 operates in Unidirectional transmission mode by setting DIRSEL1=1 and DIRSEL0=1. A pair of differential signal from Slave mode to Master mode shall not be connected. LOCKN connection from Slave mode to Master mode is required.

Table 3 INT/LOCKN function in Unidirectional transmission mode

Setting			LOCKN	Description
DIRSEL1	DIRSEL0	MSSEL		
1	1	0	LOCKN Input	Master mode
		1	LOCKN Output (open-drain)	Slave mode

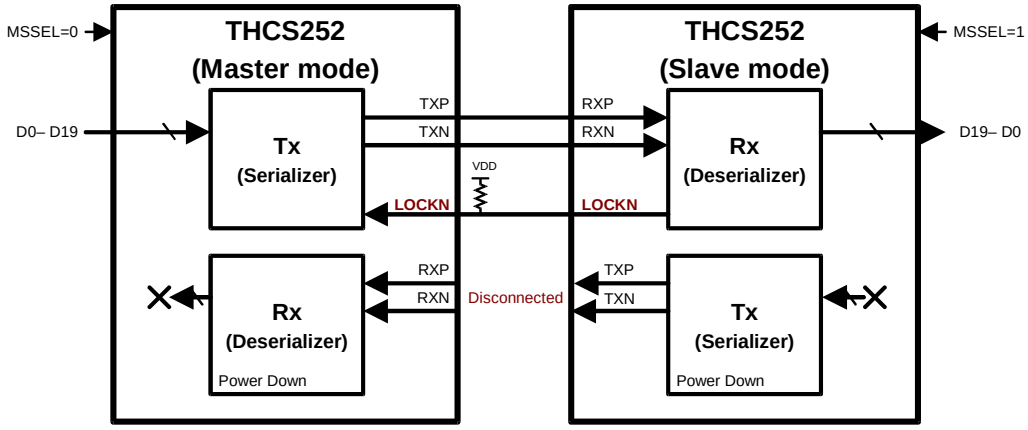


Figure 11 Setting for Unidirectional transmission mode

Table 4 Common setting of Master/Slave mode for Unidirectional transmission mode

Use case		U-1		
Mode	Downstream bit count	20		
	Upstream bit count	0		
	CML line data rate	External reference clock mode: 1/tTCIP x 30 Internal oscillator clock mode: 1/tOSC x 30		
Data pin for Master mode	D0/D19 - D19/D0	=>	D19/D0 - D0/D19	Data pin for Slave mode

"=>" means Downstream (GPIO input in Master mode and GPIO output in Slave mode).

Start communication after setting each "Use case" in both Master/Slave.

7.5. IO configuration

7.5.1. Input and Output digital noise filter

THCS252 has digital noise filters for GPIO input (for CMOS input noise immunity) and output (for CML Line noise immunity) which are configured by setting FILTSEL1 and FILTSEL0 shown in Table 5 and Table 6. The data width less than (tap_num - 1) tFLTCK is filtered. tap_num is shown in Table 5, Table 6.

Table 5 Input digital noise filter setting

FILTSEL1	FILTSEL0	Function	Filter number of taps (tap_num)
0	0	All digital noise filter setting	Disable
	1		4
1	0		8
	1		16

Table 6 Output digital noise filter setting

FILTSEL1	FILTSEL0	Function	Filter number of taps (tap_num)
0	0	All digital noise filter setting	Disable
	1		4
1	0		8
	1		16

7.5.2. LVCMOS output buffer type configuration

GPIO output buffer types are selectable from open-drain or push-pull by setting OBUF.

Table 7 Output buffer type configuration

Setting OBUF	Function
0	All GPIO outputs buffer type are selected to open-drain.
1	All GPIO outputs buffer type are selected to push-pull.

7.5.3. 5V tolerant I/O

Figure 12 shows the 5V tolerant I/O. Master and Slave has eight 5V tolerant I/O each.

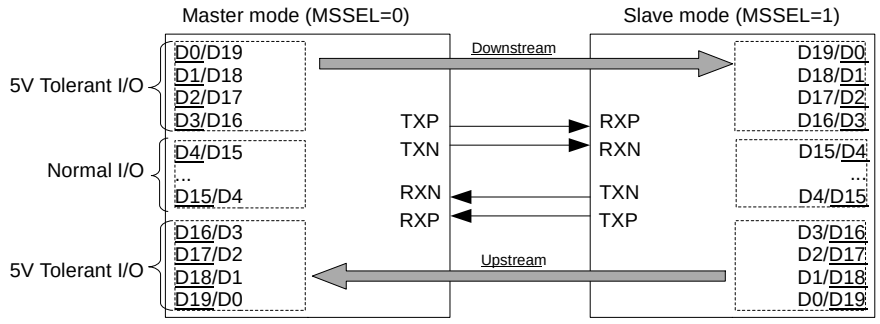


Figure 12 5V tolerant I/O

7.6. Sampling clock configuration

7.6.1. Sampling clock selection

GPIO sampling clock is always supplied from the Master mode and Master mode is selectable from internal oscillator clock or external reference clock input as shown in Figure 13 and Table 8. Internal oscillator frequency is selectable from 20MHz, 40MHz or 80MHz. Table 9 shows internal oscillator frequency and CML Line data rate. REFEN of Master mode and Slave mode shall be the same setting. GPIO data sampling clock of Slave mode is CDR clock from Rx.

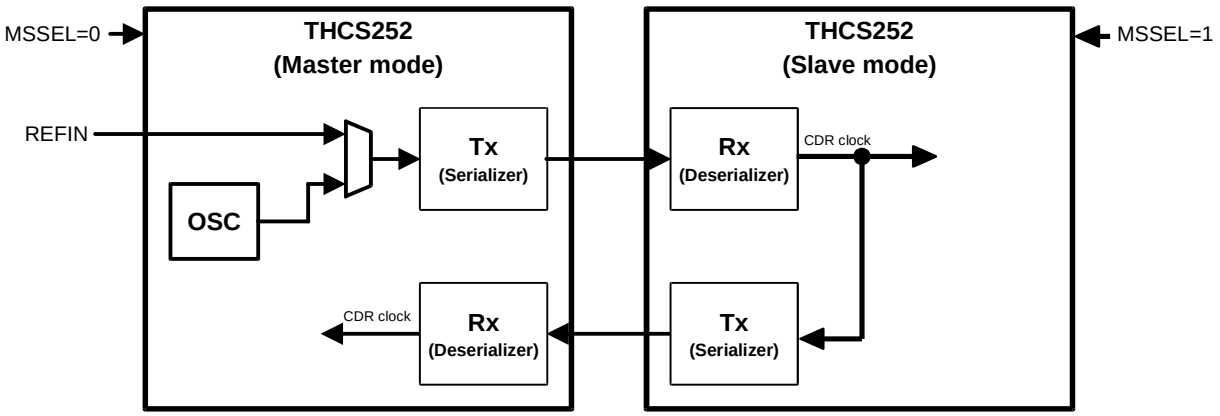


Figure 13 GPIO sampling clock source

Table 8 Sampling clock and REFIN/REFOUT/OSCSEL1 and RF/OSCSEL0 function

Setting		Sampling clock	REFIN/REFOUT/ OSCSEL1	RF/ OSCSEL0	Description
REFEN	MSSEL				
0	0 (Master mode)	Internal oscillator clock	Internal oscillator clock setting OSCSEL1, OSCSEL0		GPIO inputs are sampled by internal oscillator clock. Internal oscillator clock frequency is selected by setting of OSCSEL1 and OSCSEL0 (See Table 9)
	1 (Slave mode)	CDR clock	Hi-Z	- (Set to Low)	-
1	0 (Master mode)	External reference clock	External reference clock input REFIN	Sampling clock edge selection RF	GPIO inputs are sampled by external reference clock
	1 (Slave mode)	CDR clock	CDR clock output REFOUT	GPIO output clock edge selection RF	CDR clock output

Table 9 Oscillator Clock Frequency and CML Line data rate

Setting				Sampling frequency [*1]	CML Line data rate[*1]	Description
REFEN	MSSEL	OSCSEL1	OSCSEL0			
0	0 (Master mode)	0	0	20MHz	600Mbps	-
		0	1	-	-	Prohibition
		1	0	40MHz	1.2Gbps	-
		1	1	80MHz	2.4Gbps	-

*1 Typical value, Spec is typical±20%

When REFEN=1, RF selects REFIN sampling clock edge of Master mode and REFOUT output clock edge of Slave mode.

Table 10 RF Function

Setting	Description	
RF	REFIN sampling edge	REFOUT output edge
0	Fall edge	Fall edge
1	Rise edge	Rise edge

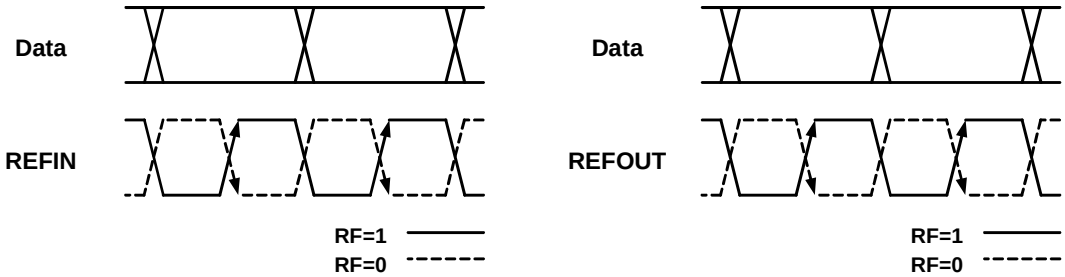


Figure 14 Input / Output clock edge

7.6.2. Spread Spectrum Clock Generator (SSCG) and REFIN frequency

THCS252 CML serial data output, GPIO data output and clock output are modulated by integrated programmable SSCG. Only Master mode operates SSCG function. The SSCG is enabled by setting SSEN. Modulation rate and frequency variation of output spread are controlled by setting the SSCG control registers shown in Table 11. Modulation rate is ±0.5% and Modulation frequency is up to 30kHz.

Table 11 SSCG setting registers

Setting SSEN	Description
0	SSCG is off.
1	SSCG is on and fixed setting. Modulation rate is ±0.5%. Modulation frequency is 12kHz when $f_{CLKSSCG}$ = FREF = 20MHz. (20MHz / 1664) = 12kHz)

Table 12 $f_{CLKSSSG}$

Setting			Sampling clock	Sampling clock frequency	$f_{CLKSSCG}$
REFEN	OSCSEL1	OSCSEL0			
0	0	0	Internal oscillator clock	Low	FREF[*1]
	0	1		-	-
	1	0		Low	FREF[*1]
	1	1		High	FREF[*1]/2
1	-		External reference clock input REFIN	15 – 57MHz	

*1 FREF : Sampling clock frequency

Table 13 External reference clock input frequency range and SSCG setting

Setting SSEN	External reference clock input frequency range [MHz]	CML Line multiply ratio	CML Line data rate [Gbps]	SSCG
0	15 - 100	x30	0.45- 3.0	Disable
1	15 - 57	x30	0.45 - 1.71	Enable

7.7. Error detection and indication

THCS252 has READY and INT for indicating Link status of CML Line communication.

READY indicates establishment of communication for GPIOs. INT indicates CML Link communication error.

Table 14 READY and INT

Status		Description
READY	INT [*1]	
0	1 (pull-up)	CML Link communication unlock state GPIO cannot transmit
1	0	CML Link communication lock state Bit level error occurred
	1 (pull-up)	CML Link communication lock state No error

*1 INT buffer type is open-drain. “1” output means pull-up.

7.8. Standby mode

THCS252 operates in Standby mode by setting STANDBY =1. The Standby mode is low power consumption and low frequency sampling rate transmission mode. In Standby mode, THCS252 can transmit up to 8-bits GPIO through handshake communication between Master mode and Slave mode. Polling period is 100ms.
READY is also enabled in Standby mode. When handshake communication is completed, READY goes from low to high.

GPIO transmitting pins show in Table 15 are configured to Downstream, Upstream or Static state. On the other hand D4/D15 – D15/D4 are fixed to Static state.

Table 15 Standby mode direction setting

Data Pin for Master mode			Data Pin for Slave mode
D0/D19	=>	D19/D0	
D1/D18	=>	D18/D1	
D2/D17	=>	D17/D2	
D3/D16	=>	D16/D3	
D4/D15 - D15/D4	Static	D15/D4 - D4/D15	
D16/D3	<=	D3/D16	
D17/D2	<=	D2/D17	
D18/D1	<=	D1/D18	
D19/D0	<=	D0/D19	

"=>" means Downstream (GPIO input in Master mode and GPIO output in Slave mode).
"<=" means Upstream (GPIO input in Slave mode and GPIO output in Master mode).
Static" means GPIO pins are Static state.

8. Package

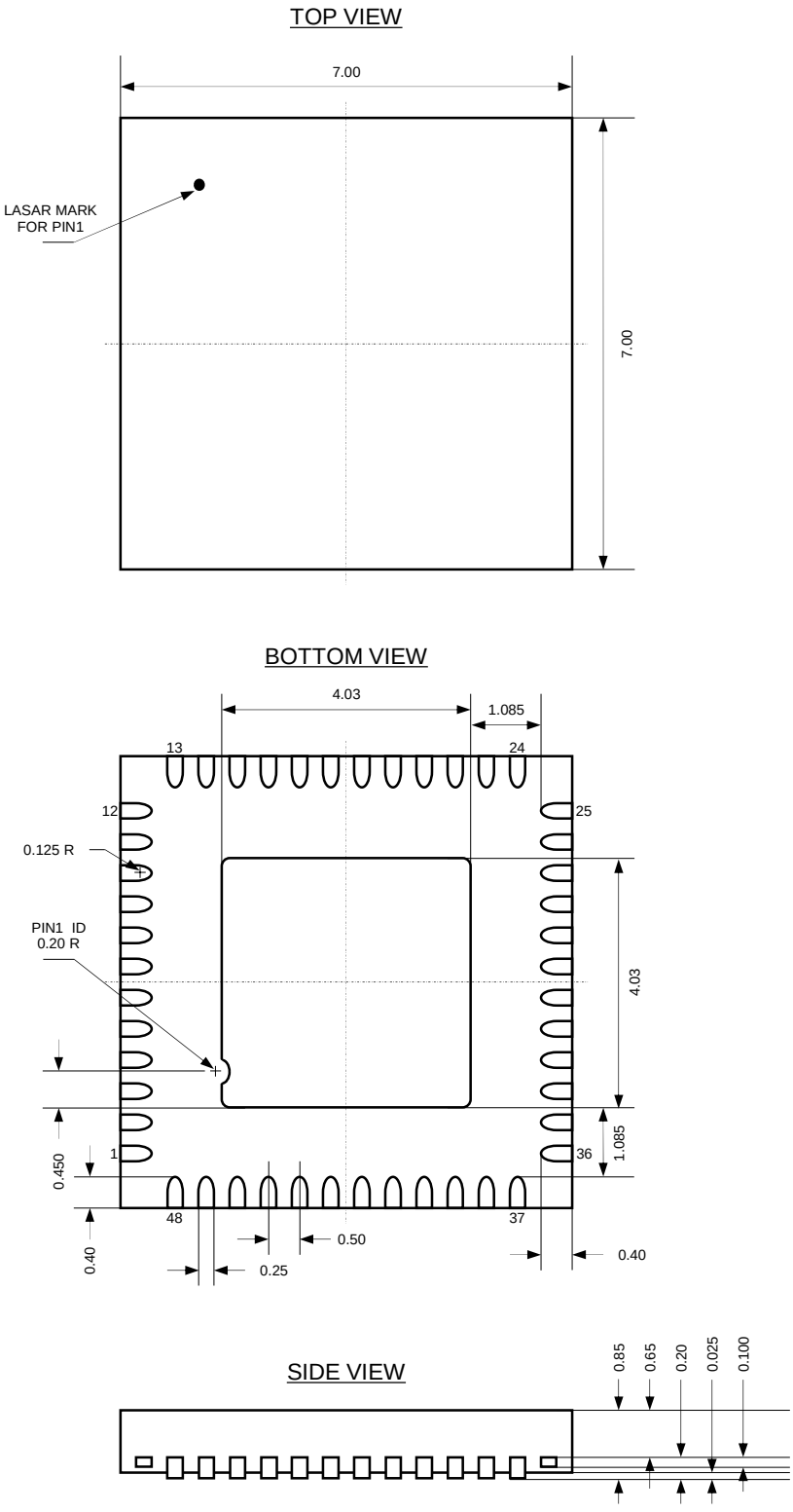


Figure 15 48-pin QFN package physical dimension

Unit : mm

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