THCS251

35bit GPIO High Speed Bus Signal Transceiver

System Design Guide

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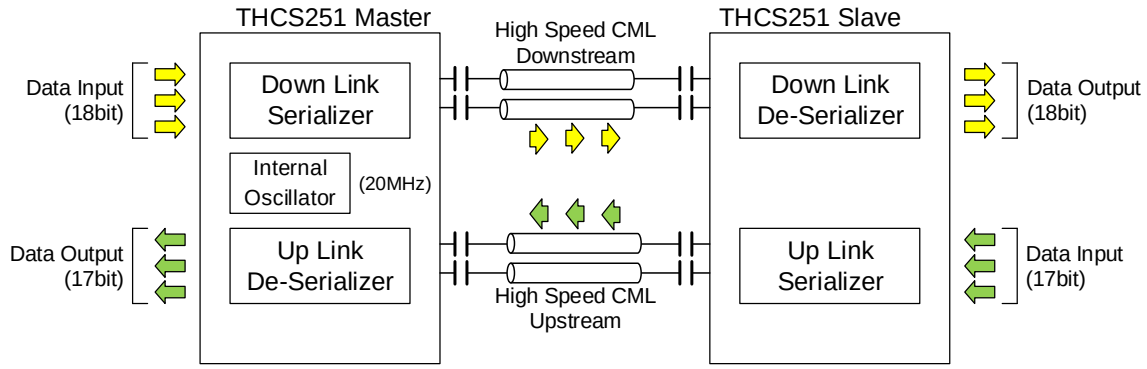
■Example1-1. Bi-directional transmit using internal oscillator. -1-

-Internal clock frequency: 20MHz
-Downstream: 18bit
-Upstream: 17bit
-Output: Push-Pull

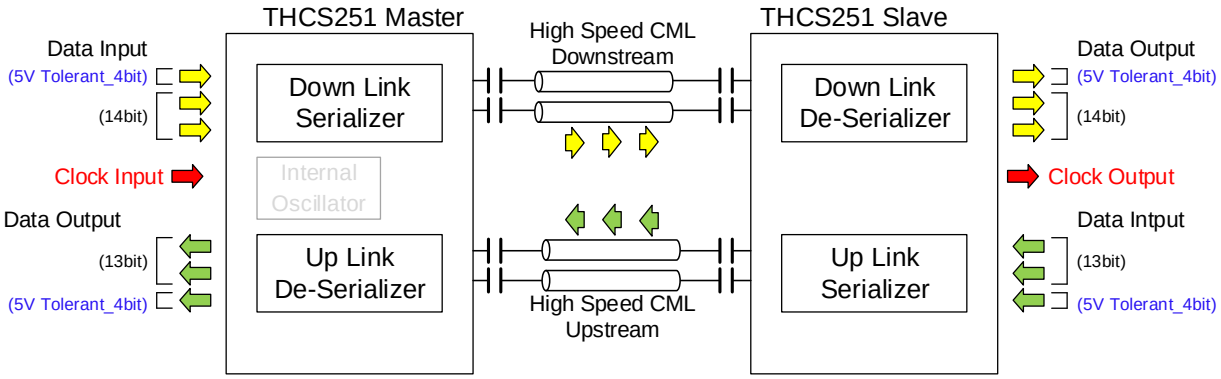
[Details: Page.5.]



■Example1-2. Bi-directional transmit using external reference clock. -2-

-Downstream: 18bit
-Upstream: 17bit
-Output: Open-Drain
*Some I/O Pins are 5V tolerant.

[Details: Page.6]

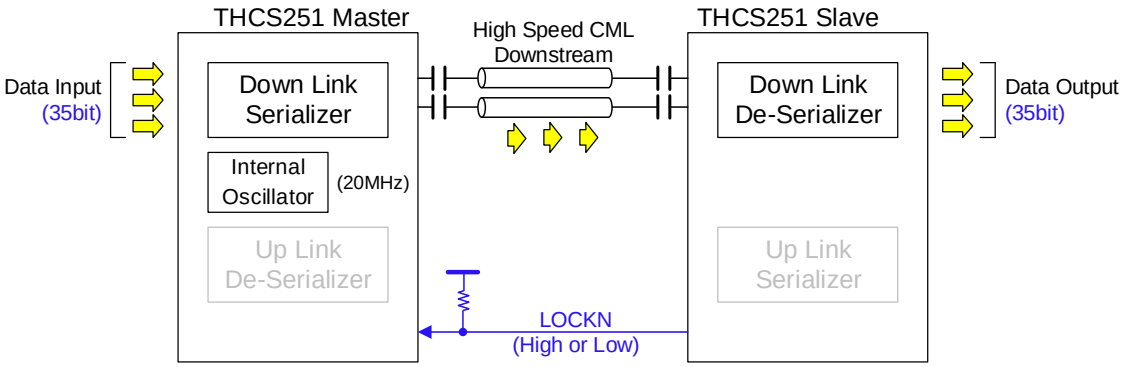


Connection Selection Guide: Standard Application 2

■Example2. Uni-directional transmit using internal oscillator

-Internal clock frequency: 20MHz
-Downstream: 35bit
-Upstream: -
-Output: Push-Pull

[Details: Page.7]



Example1-1. Bi-directional transmit using internal oscillator -1-

This case shows bi-directional transmit 18bit downstream and 17bit upstream using internal oscillator (20MHz). It can be reduced the external parts by using internal oscillator.

Pin settings are as follows.

[Chip-Master/Slave common settings]

*1. **RESERVED** (#63) is must be tied to Low.

*2. **DIRSEL0** (#46), **DIRSEL1** (#47) and **DATA_WIDTH** (#50) are set Low to support the 18bit downstream and 17bit upstream.

*3. **OBUF** (#49) is set High to select Push-Pull output type.

[Only Chip-Master settings]

*4. **MSSEL** (#1) is set Low to select Chip-Master.

*5. **REFEN** (#45) is set Low to use internal oscillator.

*6. **RF/OSCSEL0** (#2) and **REFIN/REFOUT/OSCSEL1** (#26) are set Low to select internal oscillator frequency as 20MHz.

*7. **SSEN** (#4) can be set Spread Spectrum. In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

*8. **MSSEL** (#1) is set High to select Chip-Slave.

*9. **REFEN** (#45) is set Low to disable the clock output from **REFIN/REFOUT/OSCSEL1** (#26).

*10. **RF/OSCSEL0** (#2) is disabled and should be connected to GND.

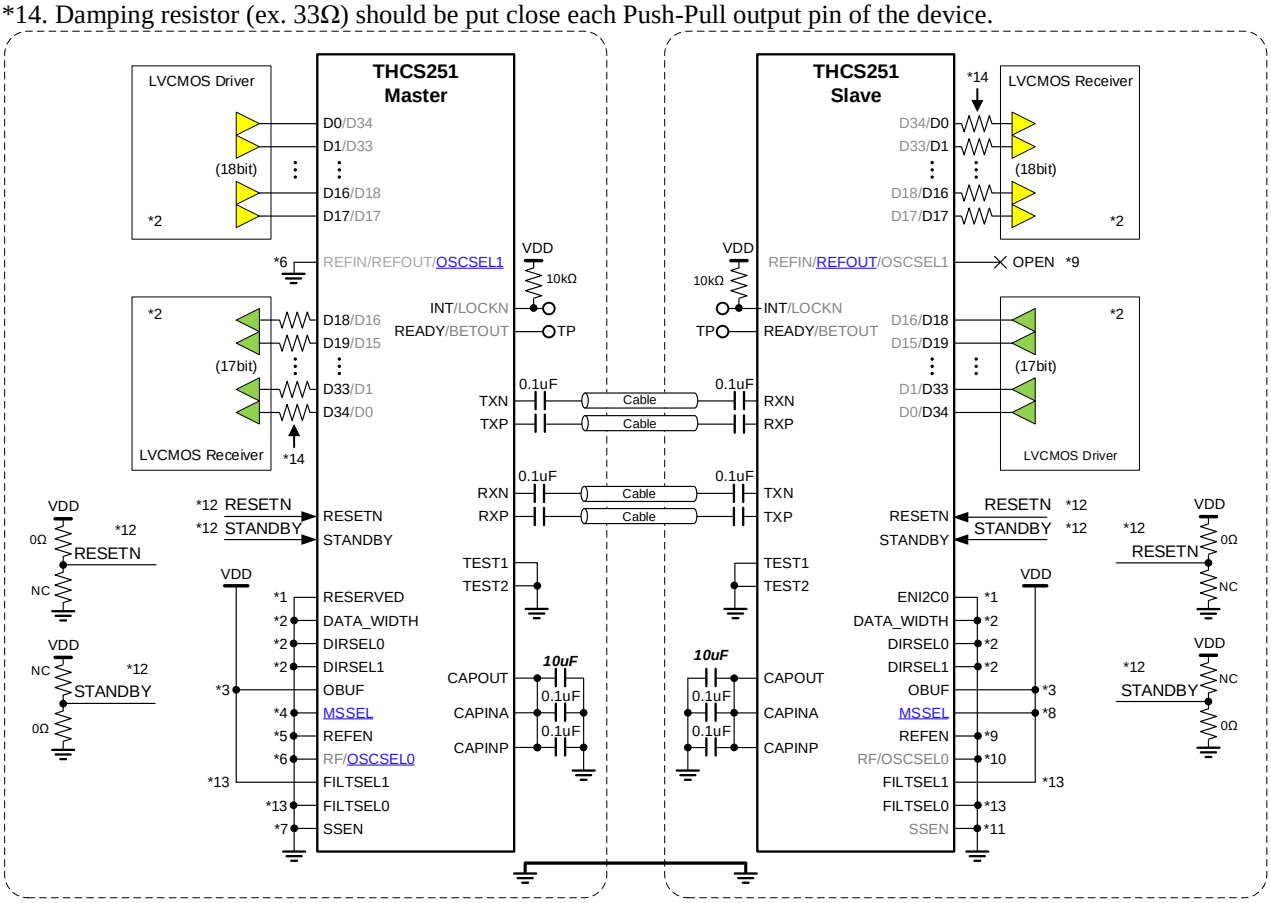
*11. **SSEN** (#4) is disabled and should be connected to GND.

[Other settings]

*12. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.

*13. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control digital filters.
In this case, the digital filter of 8 stages is selected.

*14. Damping resistor (ex. 33Ω) should be put close each Push-Pull output pin of the device.



Example1-2. Bi-directional transmit using external reference clock -2-

This case shows bi-directional transmit 18bit downstream and 17bit upstream using external reference clock.
Pin settings are as follows.

[Chip-Master/Slave common settings]

*1. **RESERVED** (#63) is must be tied to Low.
*2. **DIRSEL0** (#46), **DIRSEL1** (#47) and **DATA_WIDTH** (#50) are set Low to support the 18bit downstream and 17bit upstream.
*3. **OBUF** (#49) is set Low to select Open-Drain output type.

[Only Chip-Master settings]

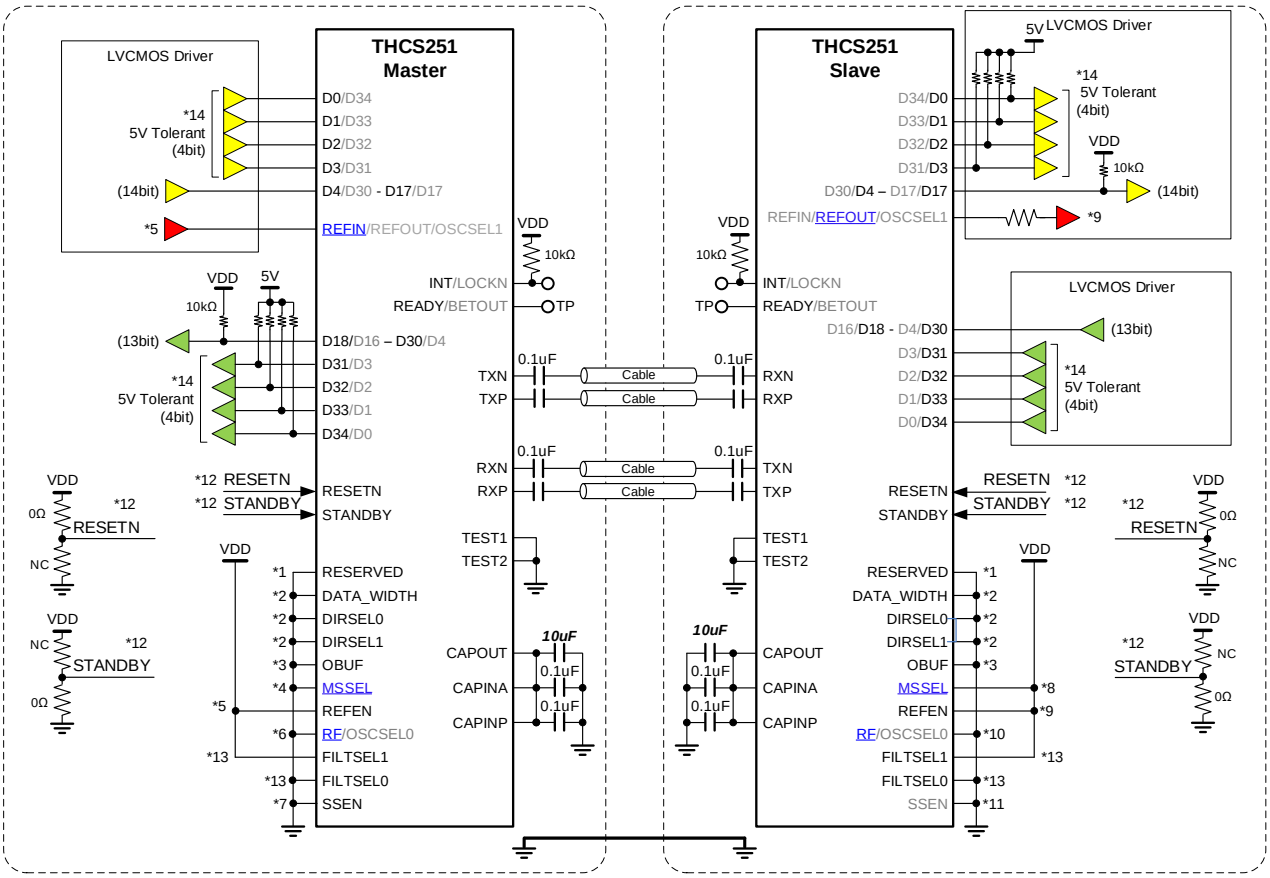
*4. **MSSEL** (#1) is set Low to select Chip-Master.
*5. **REFEN** (#45) is set High to use external clock that is input to **REFIN**/REFOUT/**OSCSEL1** (#26).
*6. **RF**/OSCSEL0 (#2) is enabled and it is adjusted to external clock edge.
*7. **SSEN** (#4) can be set Spread Spectrum. In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

*8. **MSSEL** (#1) is set High to select Chip-Slave.
*9. **REFEN** (#45) is set High to enable the clock output from REFIN/REFOUT/OSCSEL1 (#26).
*10. RF/OSCSEL0 (#2) is enabled and adjusted to clock edge of the later device.
In this case, RF is Low and it is set as Fall Edge.
*11. SSEN (#4) is disabled and should be connected to GND.

[Other settings]

*12. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.
*13. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control digital filters.
In this case, the digital filter of 8 stages is selected.
*14. Some I/O Pins are 5V tolerant.



Example2. Uni-directional transmit using internal oscillator

This case shows uni-directional transmit 35bit downstream using the internal oscillator (20MHz).
It can be reduced the external parts by using internal oscillator. The High Speed Signal line is only 1 Pair.
Pin settings are as follows.

[Chip-Master/Slave common settings]

*1. **RESERVED** (#63) is must to be tied to Low.
*2. **DIRSEL0** (#46) and **DIRSEL1** (#47) are set High and **DATA_WIDTH** (#50) is set High to support the connection of the 35bit downstream.

[Only Chip-Master settings]

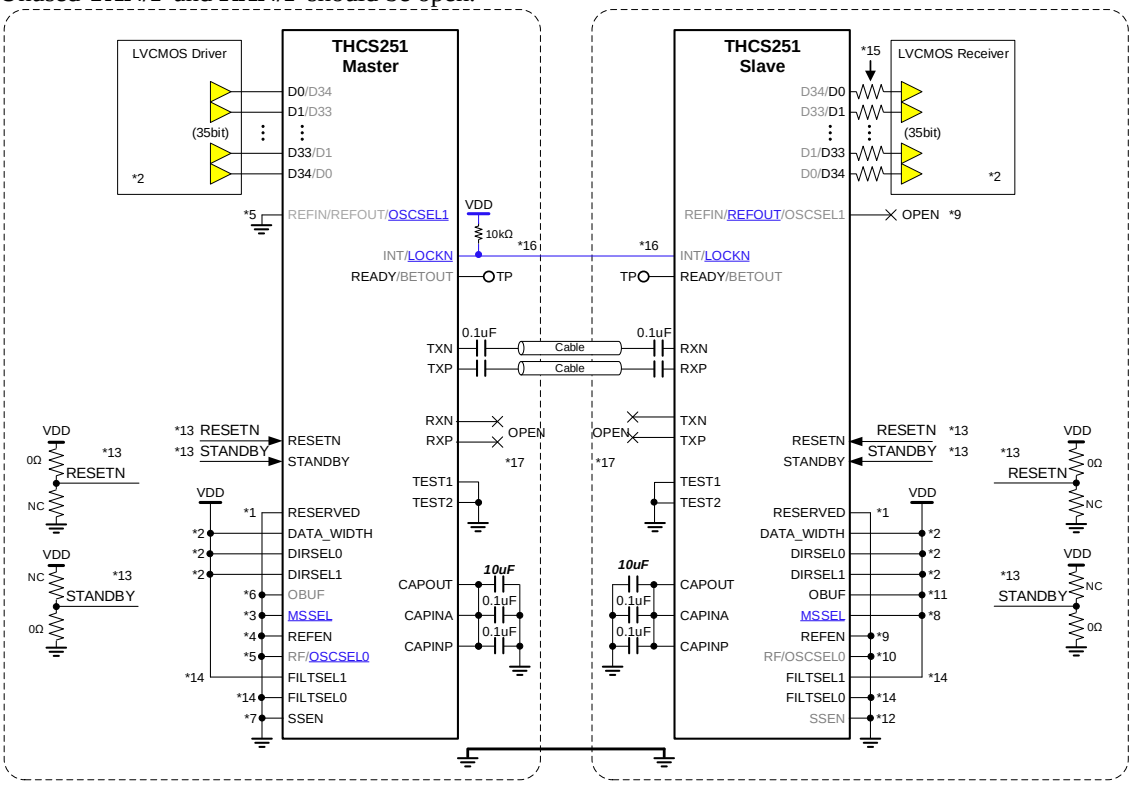
*3. **MSSEL** (#1) is set Low to select Chip-Master.
*4. **REFEN** (#45) is set Low to use internal oscillator.
*5. **RF/OSCSEL0** (#2) and **REFIN/REFOUT/OSCSEL1** (#26) are set Low to select internal oscillator frequency as 20MHz.
*6. **OBUF** (#49) is disabled and should be connected to GND.
*7. **SSEN** (#4) can be set the Spread Spectrum.
In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

*8. **MSSEL** (#1) is set High to select Chip-Slave.
*9. **REFEN** (#45) is set Low to disable the clock output from REFIN/REFOUT/OSCSEL1 (#26).
*10. **RF/OSCSEL0** (#2) is disabled and should be connected to GND.
*11. **OBUF** (#49) is set High to select Push-Pull output type.
*12. **SSEN** (#4) is disabled and should be connected to GND.

[Other settings]

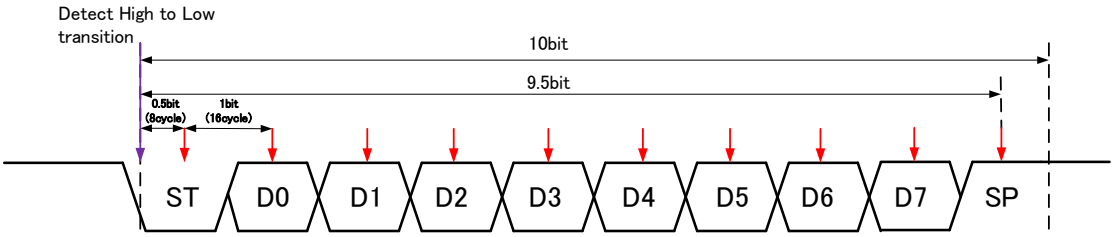
*13. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.
*14. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control the digital filters.
In this case, the digital filter of 8 stages is selected.
*15. Damping resistor (ex. 33Ω) should be put close each Push-Pull output pin of the device.
*16. **INT/LOCKN** (#60) is connected to Pull Up at the Chip-Master side.
*17. Unused **TXN/P** and **RXN/P** should be open.



Baud rate calculation method for UART communication

When propagating UART signals, sampling errors on the GPI pin that inputs the UART signals limit the baud rate of the UART device and the clock accuracy of the baud rate generator compared to when THCS251 is not used.

The following is an example of a UART communication method with 1-bit start bit, 8-bit data without parity, 1-bit stop bit, and 16 times baud rate oversampling for the receiving device.



The receiving device considers the sampling data 0.5 bits (8 sampling cycles) after detecting Low to be the start bit if it is Low, and then captures 8 bits of data and 1 bit of stop bit every 1 bit (16 sampling cycles) for a total of 9 times. In this case, if each bit is ideally sampled in the center, there is a margin of ±0.5 bits relative to the sampling point. However, it is necessary to take into account the sampling error in detecting the first low at the receiving side (one sampling period at the receiving side), the input setting time, the THCS251 sampling error, and the baud rate error between transmission and reception, which requires attention in asynchronous communications. Since the baud rate is generated by dividing the clock source of the UART transmitter/receiver device, an error in the clock source can be considered a baud rate error as it is. It should also be noted that baud rate error is different in nature from sampling error and is an accumulated error. In other words, in order to accurately sample the stop bit 9.5 bits after the first low is detected, there must remain a margin of at least the input setup and hold time required for the receiving device after 9.5 bits. Therefore, the allowable baud rate error per bit is the remaining time after subtracting each sampling error and setup time from the 0.5-bit margin, divided by 9.5 bits. This results in the following equation for the baud rate tolerance between UART transmitting and receiving devices.

$$\left\{\left(\frac{1}{2\times BAUD}-\frac{1}{16\times BAUD}-\frac{1}{REFCK}-tSH\right)\div 9.5\right\}\div\frac{1}{BAUD}\times 100 > Baud\ \ rate\ \ tolerance(\%)$$

BAUD : Baud rate (Hz)
REFCK : THCS251 operation frequency (Hz)
tSH : UART device input setup/hold time, whichever is greater (sec)

Note that the baud rate error is the relative difference in baud rates generated at each of the transmitter and receiver. For example, if your device has a tolerance of ±2% on the transmit side and ±1% on the receive side for the clock source, the relative maximum error is 3%.

With a UART device input setup and hold time of 10ns and a THCS251 internal oscillator set to 80MHz (*tOSC = max.15.7ns), the acceptable baud rate error for UART communication at a baud rate of 1Mbps is approximately 4.3% according to the above formula. The baud rate error is about 4.3%.If the maximum baud rate error of the UART device used is 4%, it means that communication is possible at a maximum baud rate of 2.56 Mbps. However, since there may be factors other than the above formulas such as transition time depending on the environment, the above calculations should be considered only as a guide and should be used with a sufficient margin.

SCLK frequency calculation method for SPI communication

Write operation

It is calculated by the following formula, which takes into account the sampling error at the GPI pin input and the setup/hold time of the SPI Target device input.

$$\frac{1}{2 \times fSCLK} > \left(\frac{1}{REFCK}\right) + tSUP/tHLD$$

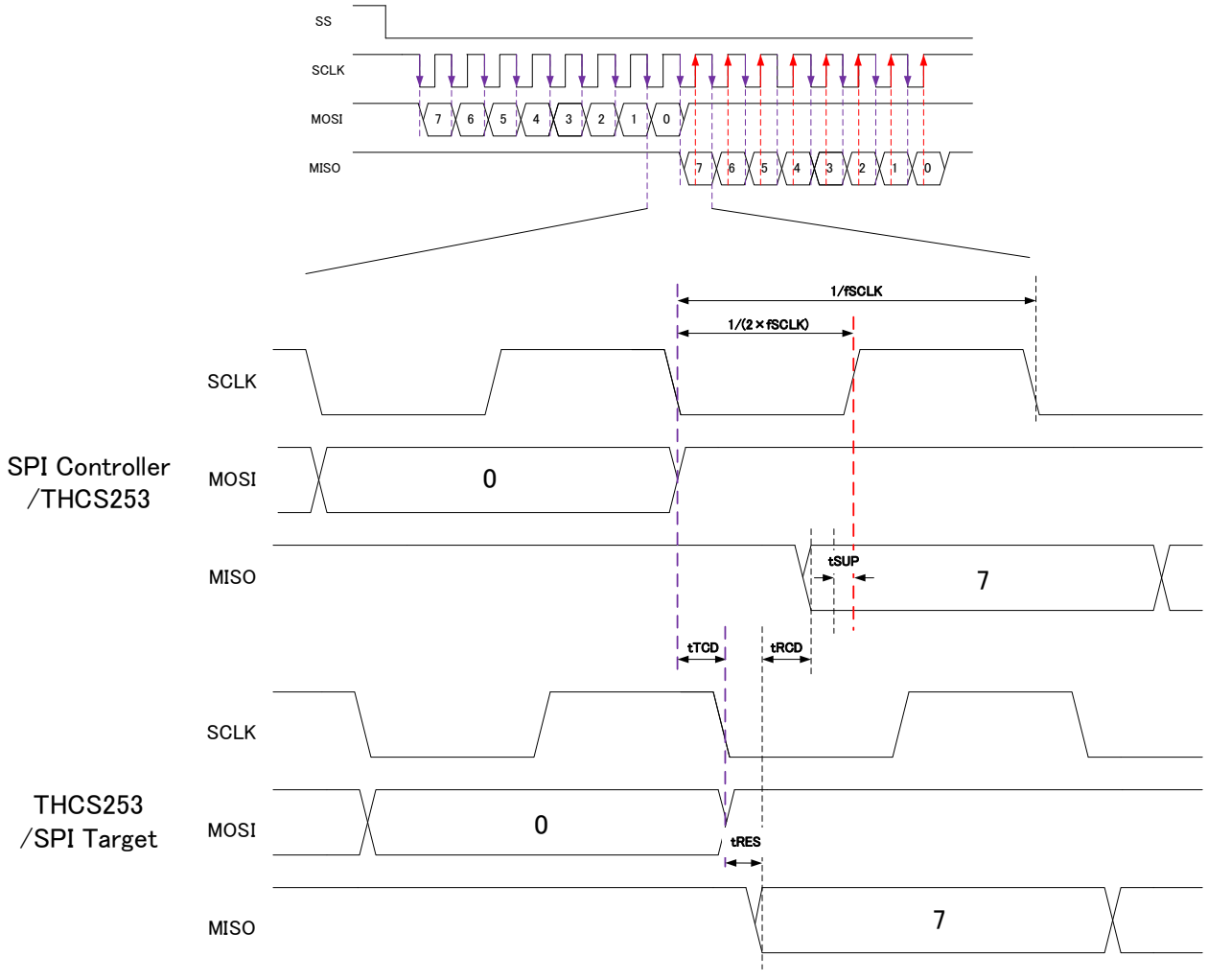
fSCLK	:	SCLK frequency (Hz)
REFCK	:	THCS251 operation frequency (Hz)
tSUP/tHLD	:	SPI Controller device input setup/hold time (sec)

If the tSUP/tHLD time is 10ns and REFCK is 80MHz, the maximum SCLK is 22MHz from the above formula.

Read operation

Read speed is limited by the delay (tTCD, tRCD) between Primary/Secondary of THCS251 and sampling error (equivalent to REFCK) at GPI pin input.

The timing chart for SPI read is shown below.



For the SPI Controller device to sample Read data correctly, the total delay shown in the timing chart above must be less than SCLK period x 1/2. Since the above timing chart does not show the sampling error due to asynchronous sampling of THCS251, the following equation is obtained by adding the sampling error (1/REFCK) to tTCD and tRCD.

$$\frac{1}{2 \times fSCLK} > \left(tTCD + \frac{1}{REFCK}\right) + tRES + \left(tRCD + \frac{1}{REFCK}\right) + tSUP$$

fSCLK	:	SCLK frequency (Hz)
REFCK	:	THCS251 operation frequency (Hz)
tTCD	:	THCS251 Primary to Secondary delay time (sec)
tRCD	:	THCS251 Secondary to Primary delay time (sec)
tRES	:	SPI Target device response time (sec)
tSUP	:	SPI Controller device input setup time (sec)

Assuming that the response time of the SPI target device and the input setup time of the SPI controller device are 10ns each, the calculation results are as follows.

$$fSCLK < 600KHz$$

REFCK	:	64MHz * Minimum frequency when the built-in OSC is set to 80 MHz.
tTCD	:	12.5ns(64MHz)×25=390.6ns *digital noise filter disable
tRCD	:	12.5ns(64MHz)×25=390.6ns *digital noise filter disable
tRES	:	10ns
tSUP	:	10ns

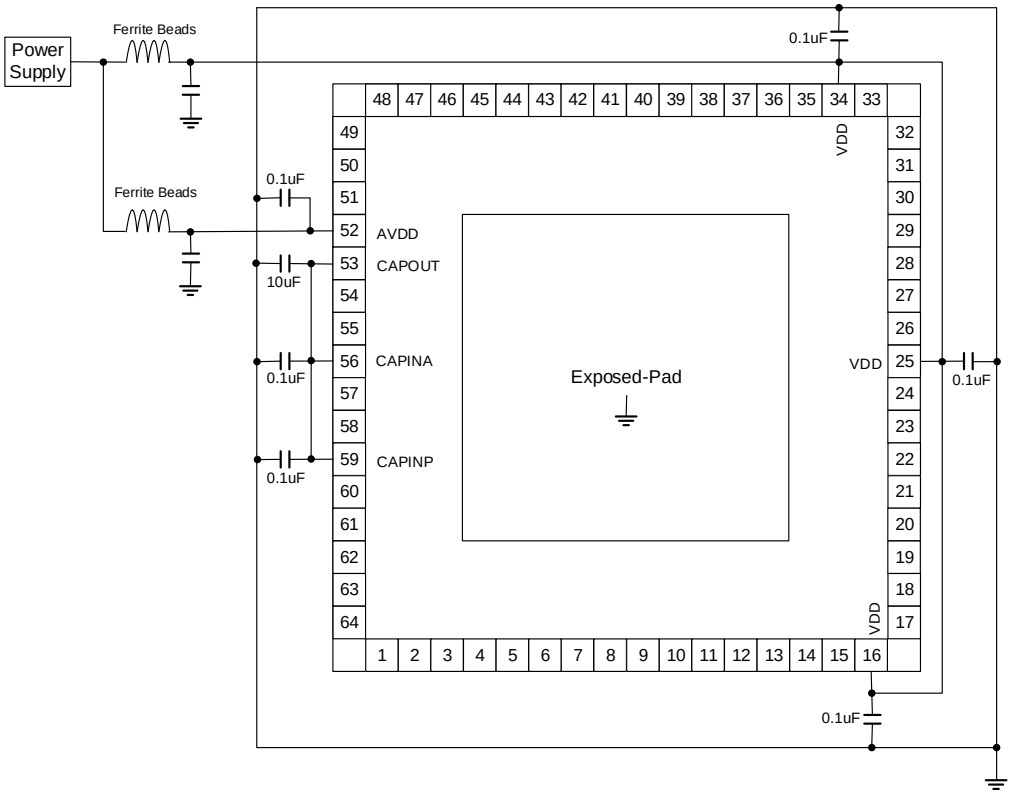
The above calculation example shows the maximum SCLK frequency when the built-in OSC is used, but a faster SCLK frequency can be supported by using the REFCK input pin to input a high-speed clock. When a 133 MHz clock signal is input to the REFCK input pin, the maximum SCLK frequency is 1.2 MHz.

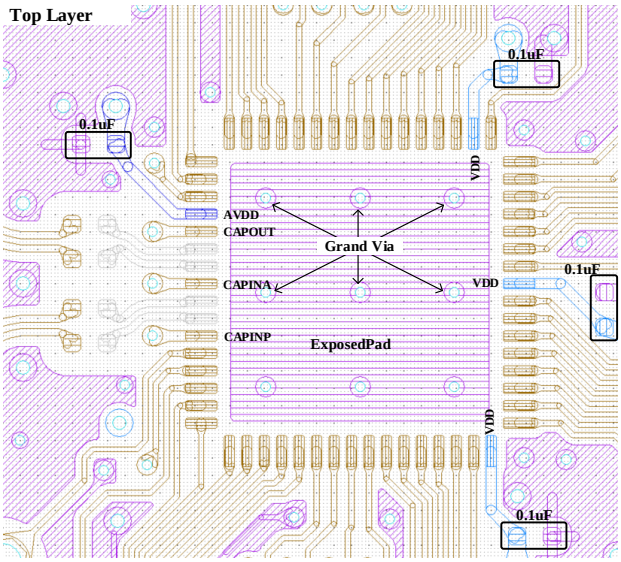
In the actual environment, multiple target devices are connected on the SPI bus, which deteriorates the transition time. The delay caused by this transition time deterioration cannot be ignored. In this case, the amount of delay due to transition time must be added to the right side of the above equation.

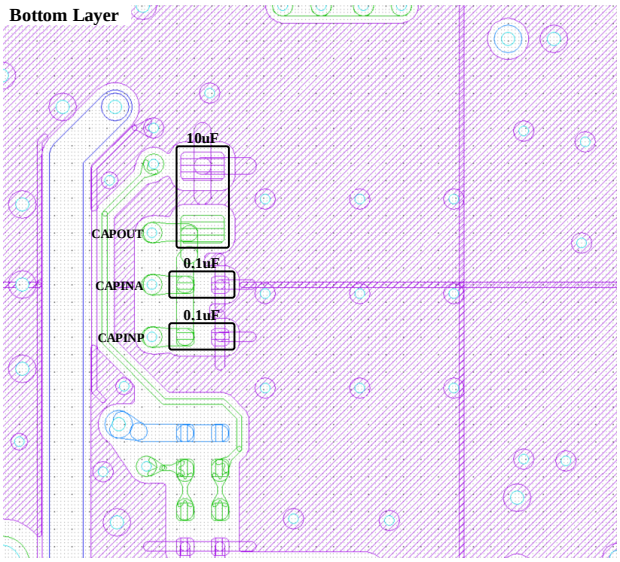
In the THCS series, either an external REFIN input or an internal oscillator can be selected as the REFCK, but it should be noted that the internal oscillator has a large frequency error. When using the THCS series product built-in oscillator, calculate using the maximum value of tOSC specified in the datasheet.

Design Guideline for Power Supply

Insert filters (Ferrite Beads and Capacitors) in the Power Supply (**VDD** and **AVDD**).
And insert Bypass Capacitor (0.1uF) in the Power Supply pins.
This device is equipped with a 1.2V built-in regulator
Insert Bypass Capacitors (**CAPOUT**: 10uF and **CAPINA/CAPINP**: 0.1uF) also for this regulator.
Bypass Capacitors should be attached just near the device.
Insert the GND-Via to the Exposed-Pad to strengthen.

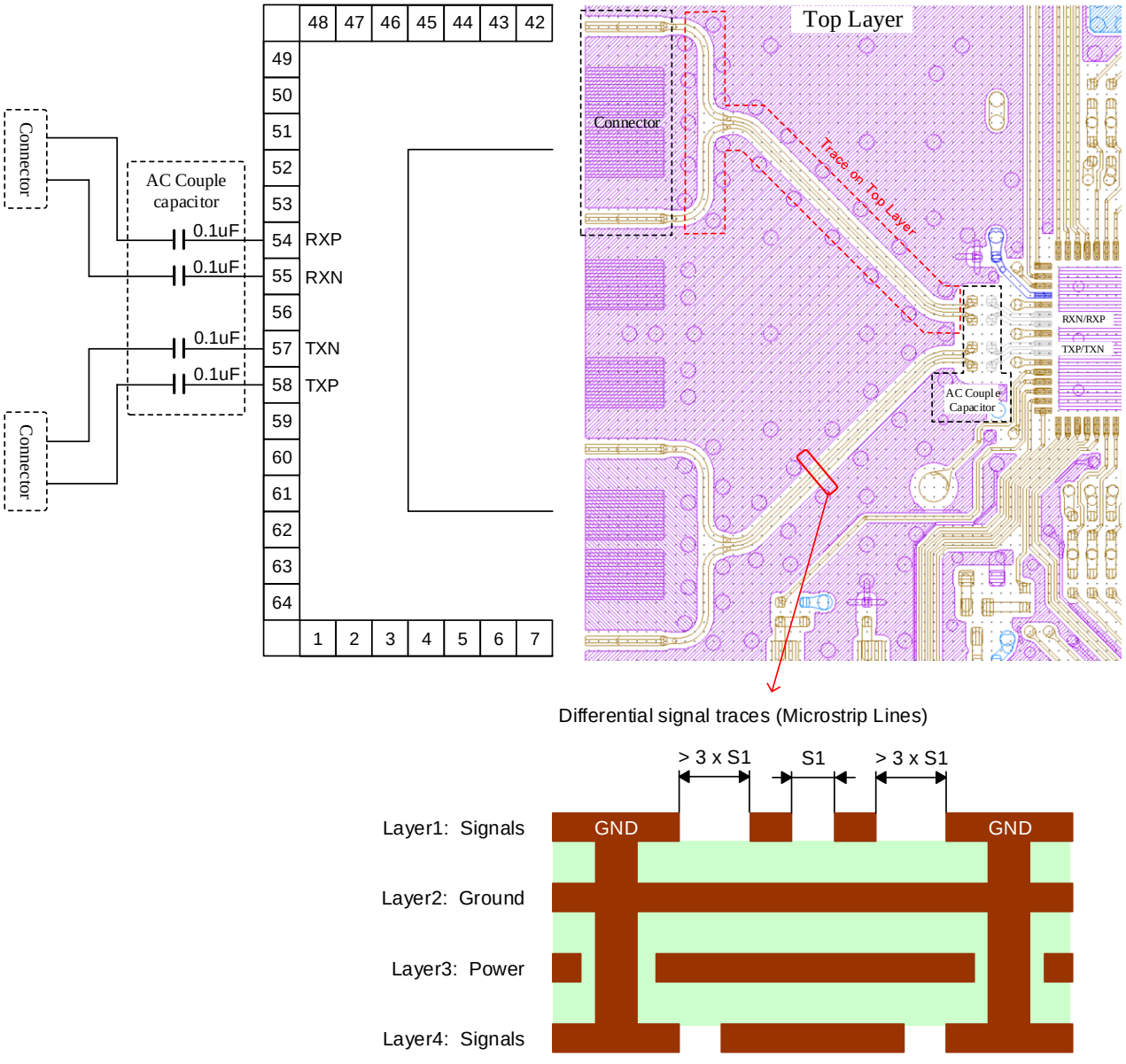






Design Guideline for High-Speed Signal

TXP/TXN and **RXP/RXN** are differential pairs of high-speed serial signals.
Differential pairs should be closely spaced and coupled to eliminate common mode noise.
Also, differential should be designed as 100Ω differential characteristic impedance (Zdiff).
The following is an example of microstrip line design.
The high-speed signal lines trace in only single layer.
The AC coupled capacitors should be attached just near the device.



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