THCX422R10 Design Guide

System Diagram and PCB Design Guideline

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Application information

The THCX422R10 is high performance bi-directional active re-driver for serial links with data rates up to 10Gbps.

The THCX422R10 feature a continuous time linear equalizer (CTLE) to provide a boost of up to +15.6dB at 5 GHz and open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums.

Design reference example

Reference equalization setting on the USB3.1 Gen2 Downstream Facing Port (DFP)

USB3.1 Gen2 TX Compliance Test lane

EQDCn *1	EQACnU *1	EQACnL *1	Host to THCX422R10 insertion loss [dB] at 5GHz	Host to THCX422R10 trace length [cm]
F	L	L	6.6	17.8
F	R	L	10.9	29.4

USB3.1 Gen2 RX Compliance Test lane

EQDCn *1	EQACnU *1	EQACnL *1	Host to THCX422R10 insertion loss [dB] at 5GHz	Host to THCX422R10 trace length [cm]
H	L	L	6.6	17.8
F	L	L	10.9	29.4

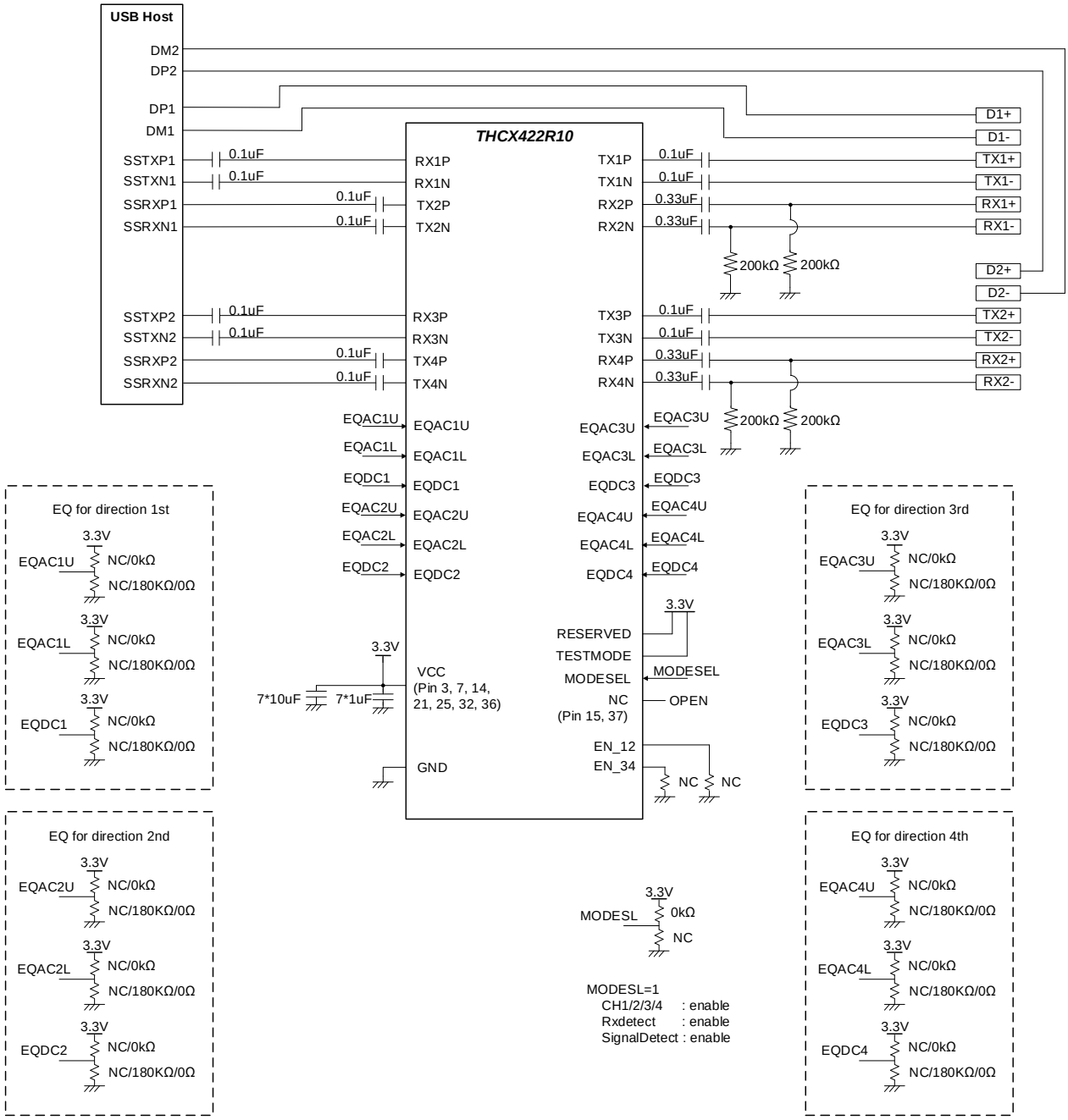
*1n=1, 2, 3, 4
*2This result is a calculated result when FR4 insertion loss = 0.37dB/cm
*3Assuming the insertion loss from THCX422R10 to connector side is 1.1dB at 5GHz
*4L: Tie 0Ω to GND
R: Tie 180kΩ to GND
F: Leave Open
H: Tie 0Ω to VCC

Reference condition

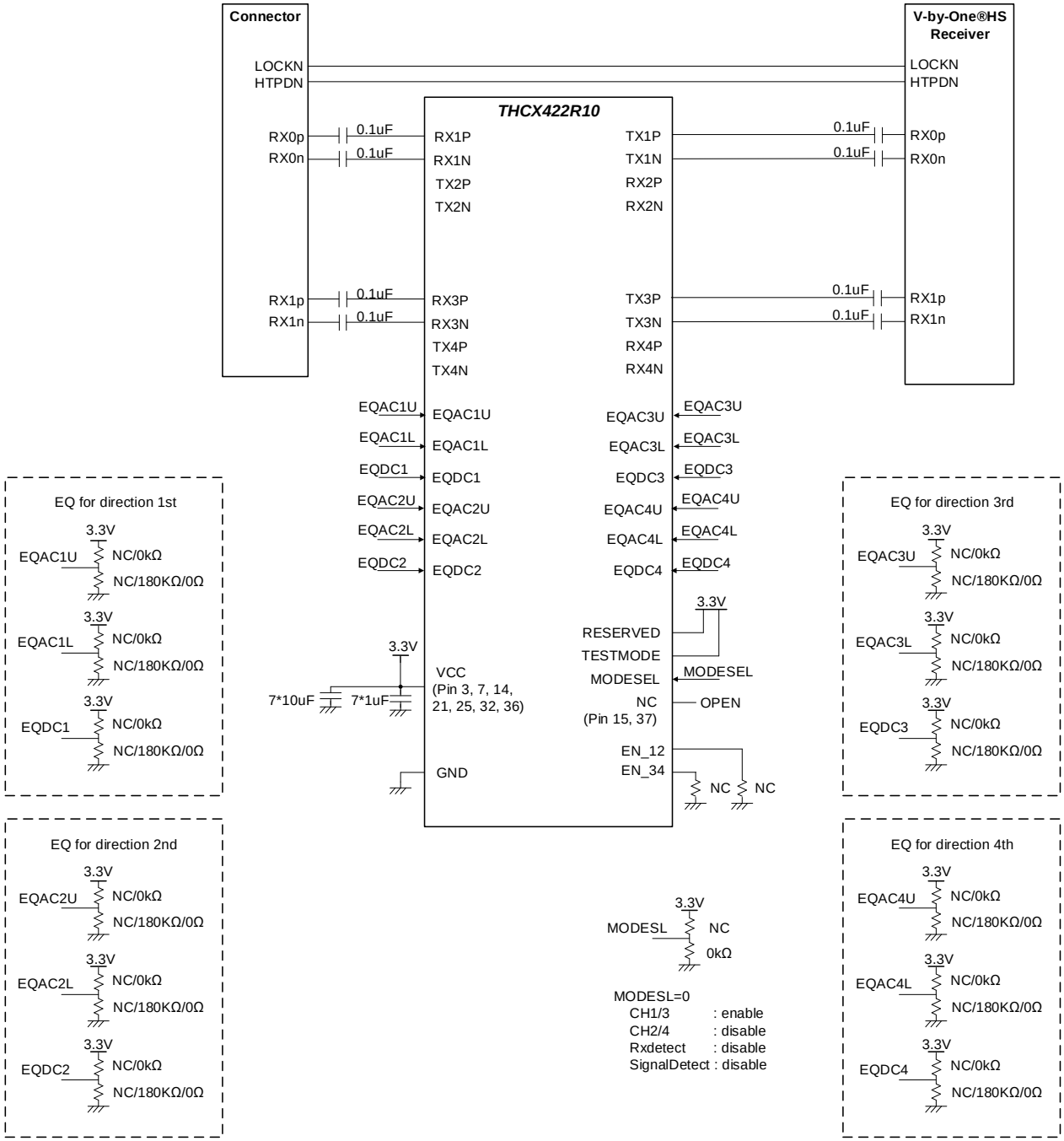
Parameter	**Value**
PCB trace width	0.17mm
VCC supply (3.0V – 3.6V)	3.3V
PCB material	FR4

Application diagram

Example of use in USB3.x Downstream Facing Port (DFP)



Example of use as an equalizer in V-by-One®HS receiver



Layout guide

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer.
- PCB traces for high-speed differential signals must be coupled microstrip lines whose differential characteristic impedance is 90Ω (USB) / 100Ω (V-by-One®HS) ±10%.
- Keep differential traces on the layer next to the ground plane, refer to Figure 1.
- Avoid right-angle turns (Figure 2) and minimize the number of vias within 2 or less on the high-speed traces to prevent impedance discontinuity and degrade the signal integrity.

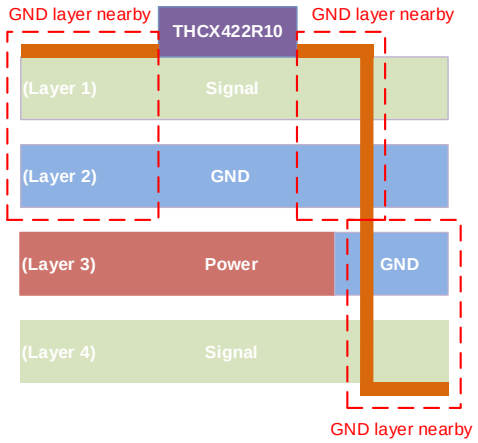


Figure 1. Keep High-speed line next to GND layer

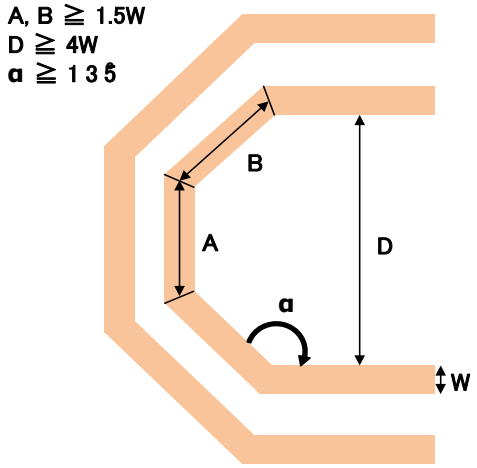
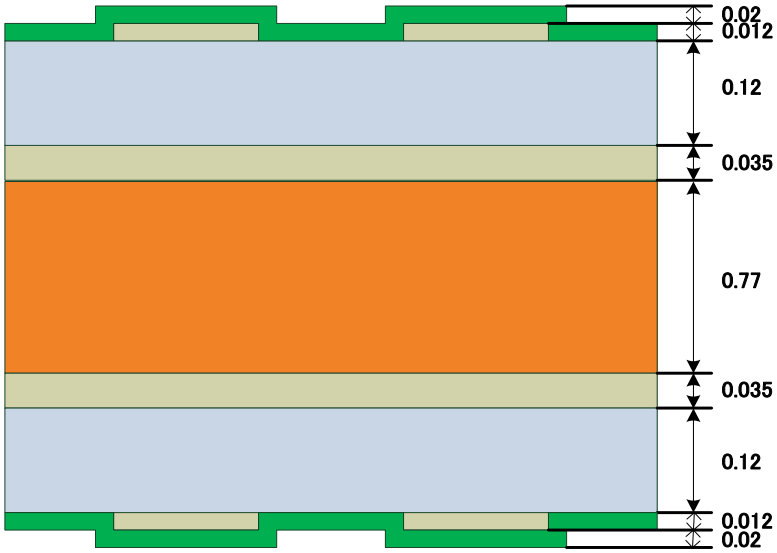


Figure 2. Avoid right angle turn

- Minimize the distance within 5mils between traces of a differential pair to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Distance between pair should be at least 4 times of the signal trace width.
- Keep away from other high-speed signals.
- Put adjacent GND plane and via between each differential pair for avoiding cross talk.
- Route differential signal traces symmetrically.
- Test points affect the signal integrity. If must place test points, they should be placed in series and symmetrically.
- Match the length of differential line at the mismatch location

PCB Stack up example (FR4)



Trace width:	0.17mm
Trace space:	0.13mm
Through hole's diameter:	0.201mm
Through hole's amount:	2

Figure 3. 4 layer PCB stack up example

Notices and Requests

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2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.

5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.

5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.
sales@thine.co.jp
https://www.thine.co.jp