

# **THCV2911A/B Design Guide**

## **System Diagram and PCB Design Guideline**

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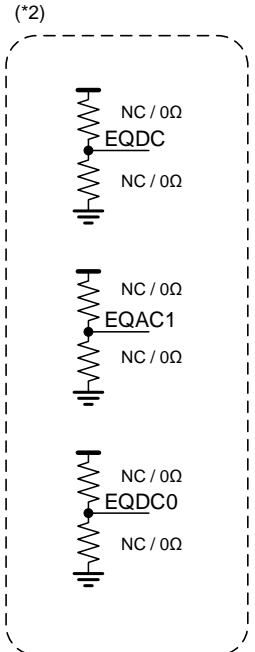
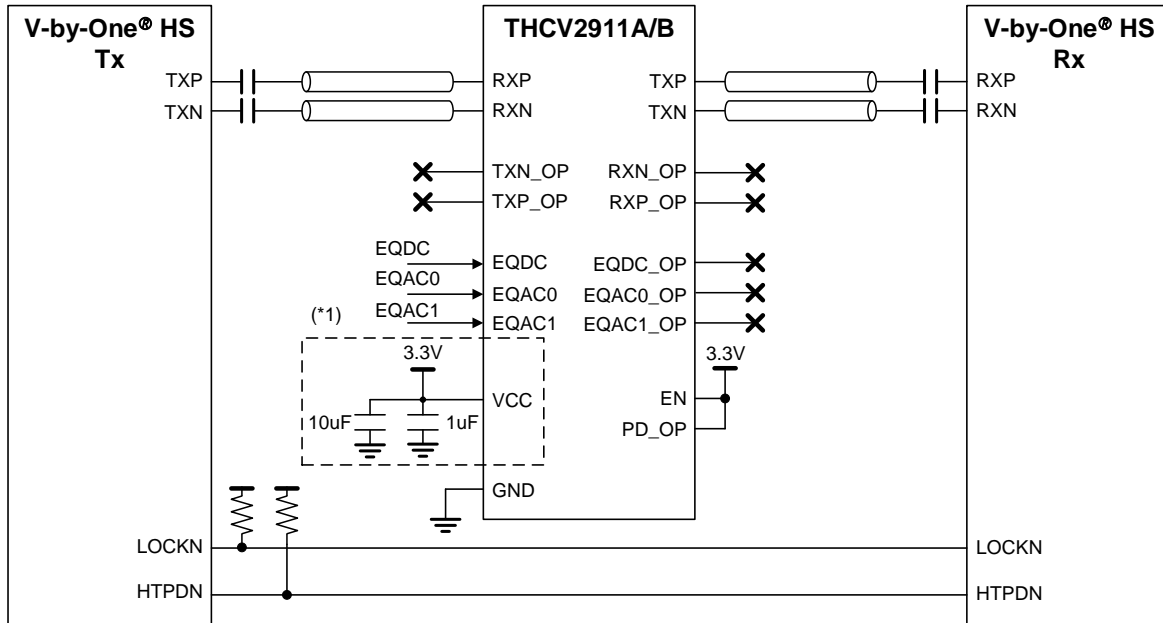
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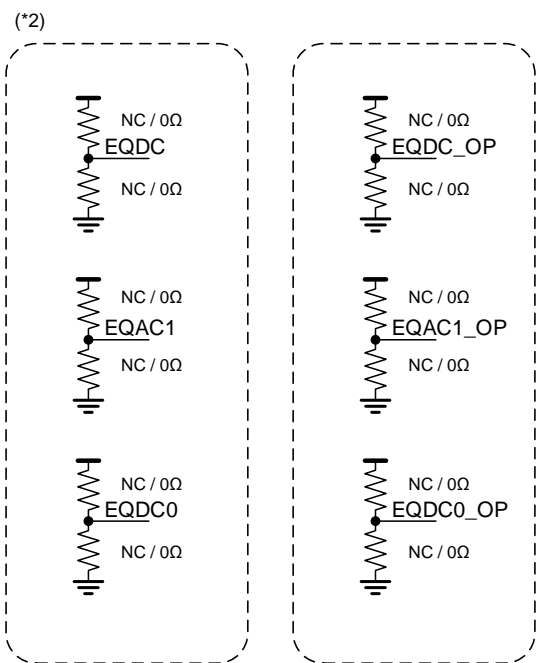
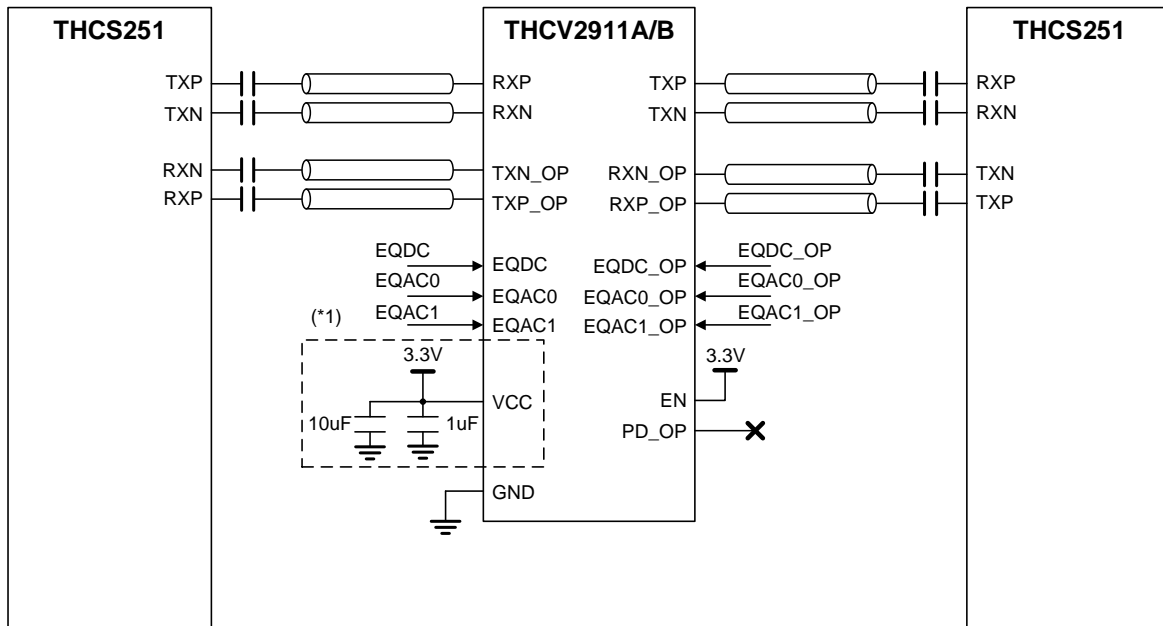
**Application diagram**

Example: Redriver for V-by-One® HS



(\*1) Place bypass capacitors on each VCC pin.  
 (\*2) Refer to a datasheet for Equalizer settings.

Example: Redriver for THCS251

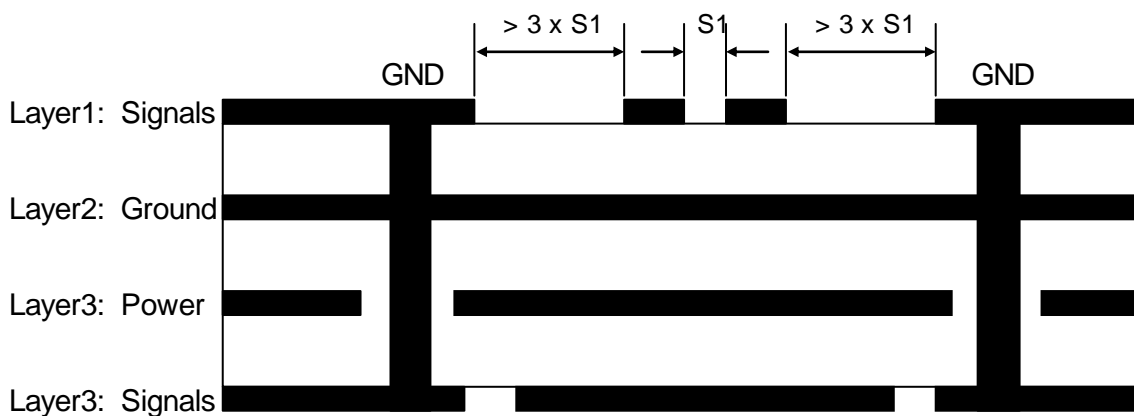


(\*1) Place bypass capacitors on each VCC pin.  
 (\*2) Refer to a datasheet for Equalizer settings.

**PCB Layout Considerations**

- Use at least four-layer PCB with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended microstrip lines or coupled microstrip lines for 100Ω differential characteristic impedance.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- For high speed signals, avoid right-angle bends in a trace. Route them at least with two 45° corners or round bend. Also avoid transmission line with vias in signal routings for signal integrity. If it is impossible, trace the differential line vias with symmetrically during and manage via impedance for required characteristic impedance.
- Mismatch among impedances of PCB traces, connectors and cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode choke filter on differential traces would reduce system EMI. Pay attention on parasitic capacitance for the component and differential mode attenuation for high speed signal. For example, in case of 3Gbps data-rate, low impedance of common mode at 1.5GHz would reduce the EMI, however low impedance of differential mode at 1.5GHz would make signal integrity worse.

**PCB Cross-sectional View  
for Microstrip Lines**



**Figure 1 PCB cross-sectional view**

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[sales@thine.co.jp](mailto:sales@thine.co.jp)

<https://www.thine.co.jp>