Application Note	*THCV242_DesignGuide_Rev.3.30_E*

THCV242 Application Note

Design Guideline

Contents

Design Flow

Design Flow Chart

THCV24x system typical design flow is shown below.

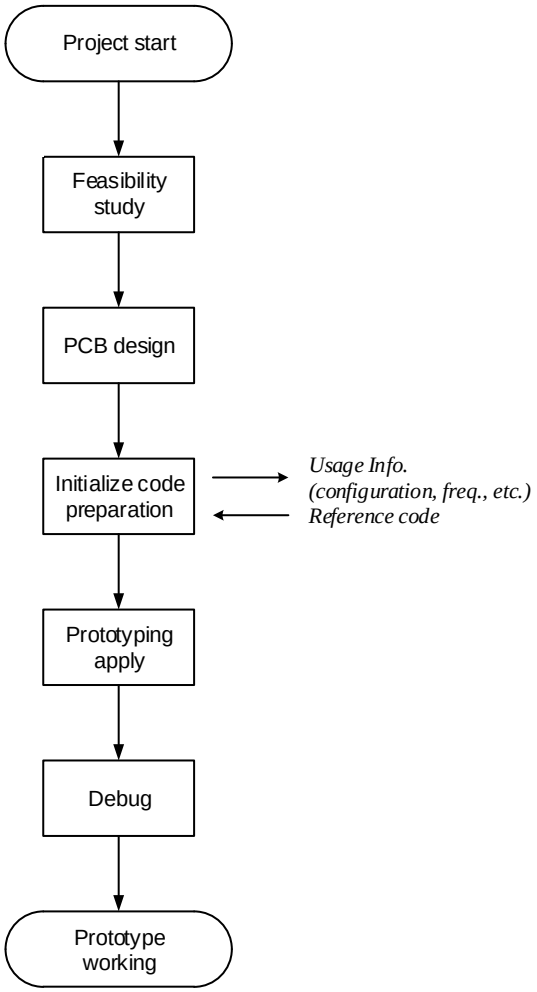


Figure 1 THCV24x typical design flow

This Design Guide provides reference information of hardware, code and other important information.

Reference code for each usage Initialization can be support option as a meaningful start point of coding.

Initialization coding consideration materials example

Initialization code requires understanding of application system. Below is an example of consideration.

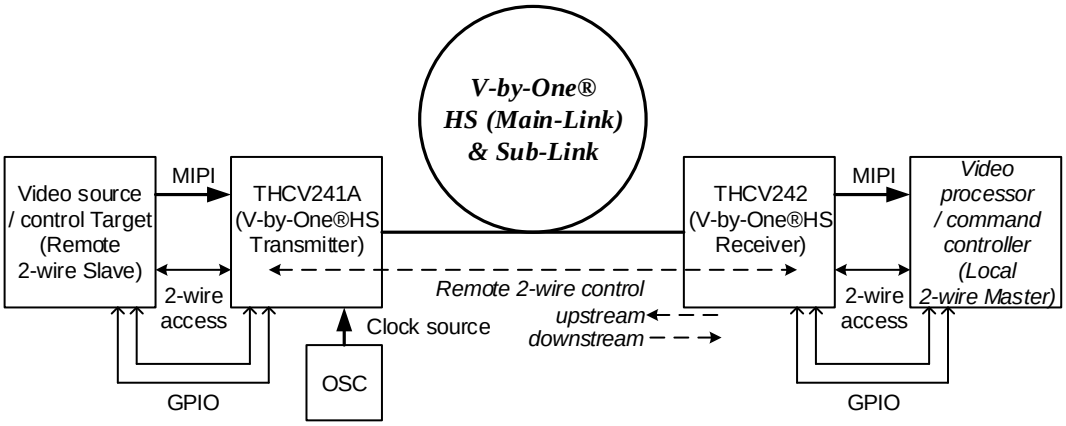


Figure 2 Example schematic diagram of Application system with regard to consider initialization code

Table 1 Initialization code reference materials example

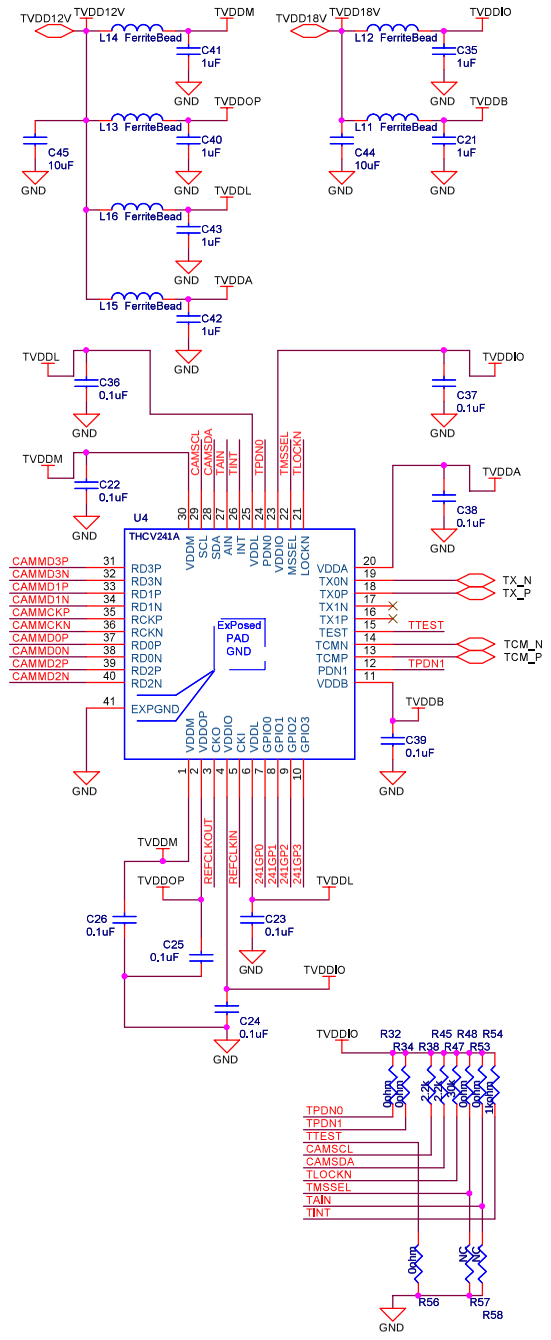
Category	Required items	example
Configuration	Tx IC name	THCV241A
Configuration	Tx IC number	1
Configuration	Rx IC name	THCV242
Configuration	Rx IC number	1
Configuration	2-wire control source (2-wire Master) location	THCV242 side only. (Leading controller is only one located at THCV242 side)
Configuration	2-wire control target device addr.	THCV242(Sub-Link Master) 7'h0B
Configuration	Sub-Link use or not	Yes (use Sub-Link)
Configuration	Vx1HS Tx CKI frequency	24MHz
Configuration	Vx1HS Tx CKO use or not	No (no use of CKO, which is recommended)
Local 2-wire Master Info.	2-wire slave clock-stretching allowed or not	Allowed (Sub-Link Pass-Through mode is recommended)
Remote 2-wire Slave Info.	Remote 2-wire Slave SCL communication Speed	100kbps
Remote 2-wire Slave Info.	Remote 2-wire Slave Device Address	7'h7A
Remote 2-wire Slave Info.	Remote 2-wire Slave Sub-Address Byte number	2Byte
MIPI (Tx side) Info.	MIPI input data-rate to Vx1HS Tx	891Mbps
MIPI (Tx side) Info.	MIPI input Lane number to Vx1HS Tx	2Lane
MIPI (Rx side) Info.	MIPI output data-rate from Vx1HS Rx	891Mbps
MIPI (Rx side) Info.	MIPI output Lane number from Vx1HS Rx	2Lane
MIPI (Rx side) Info.	MIPI output continuous clock from Vx1HS Rx	Yes (MIPI clk keep High Speed continuous output, which video processor needs)
GPIO Info.	GPIO purpose	Sensor reset
GPIO Info.	GPIO usage number	1
GPIO Info.	GPIO upstream number	1 (GPIO0 as Open-drain Register GPIO for slow reset control)
GPIO Info.	GPIO downstream number	0
GPIO Info.	GPIO time sensitive upstream number	0
GPIO Info.	GPIO time sensitive downstream number	0

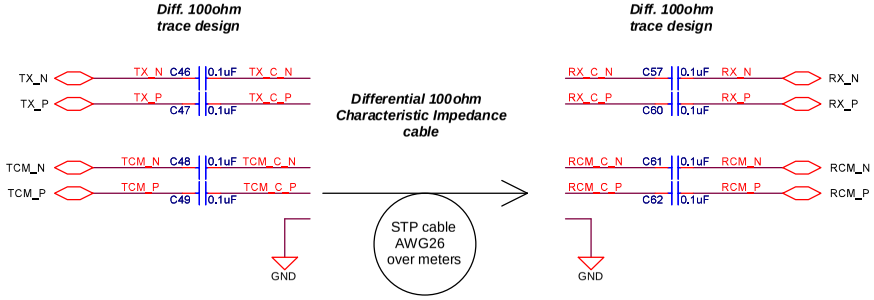
Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input
optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

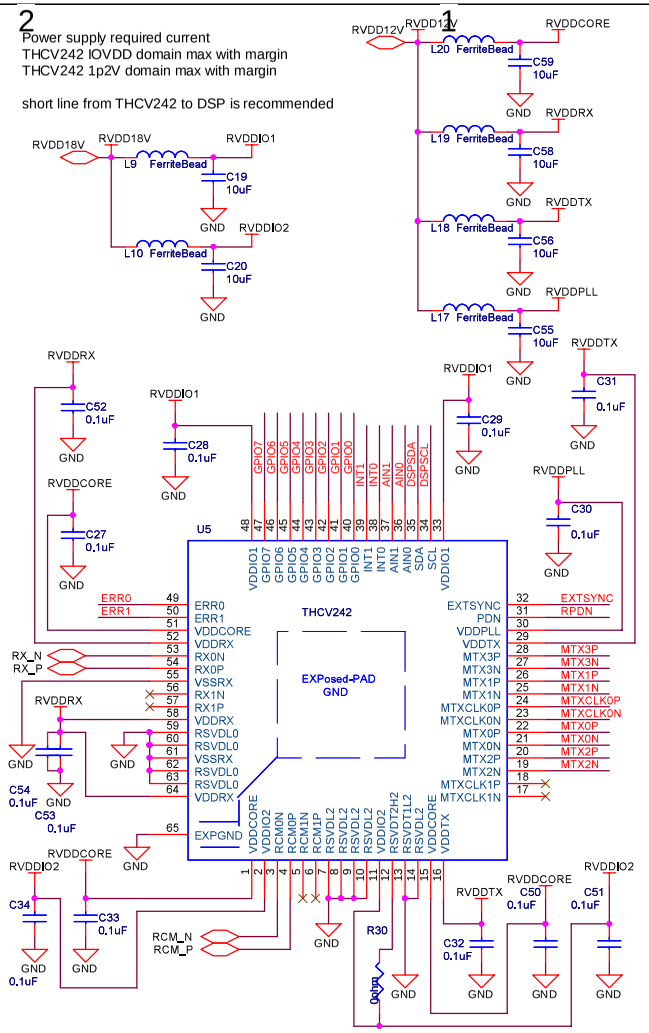
Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

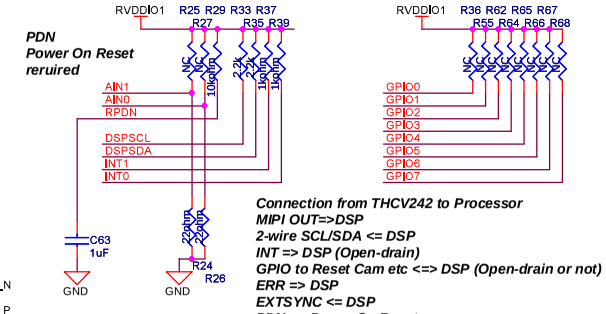
Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended









Connection from THCV242 to Processor
MIPI OUT=>DSP
2-wire SCL/SDA <= DSP
INT => DSP (Open-drain)
GPIO to Reset Cam etc <==> DSP (Open-drain or not)
ERR => DSP
EXTSYNC <= DSP
PDN <= Power On Reset

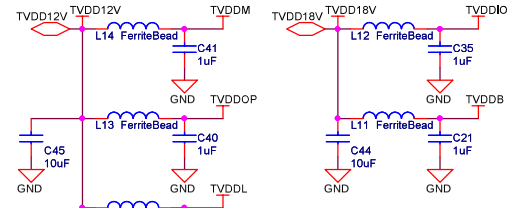
Title	THCV241A-242 Example1	
Size A3	Document Number CV241A-242_E1	Rev 1201
Date: Friday, December 11, 2020	Sheet 1 of 1	

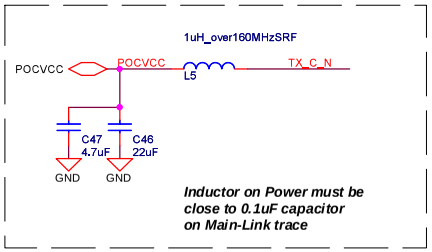
Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

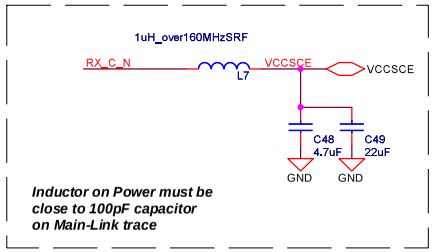
Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

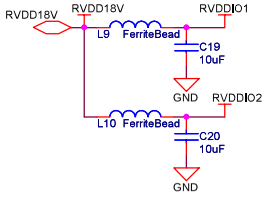
Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

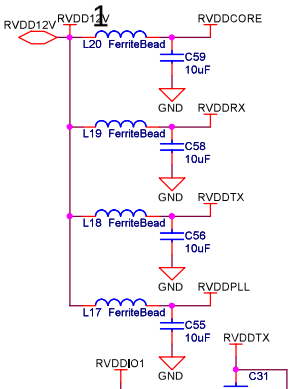
short line from THCV242 to DSP is recommended

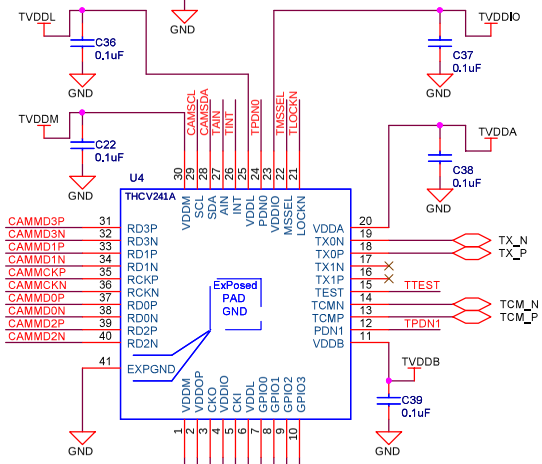


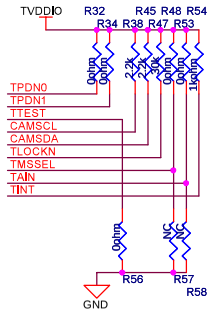


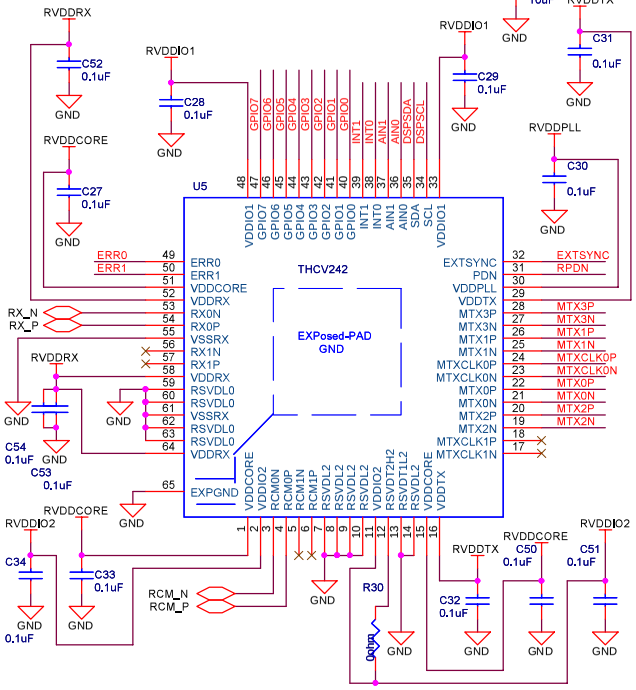




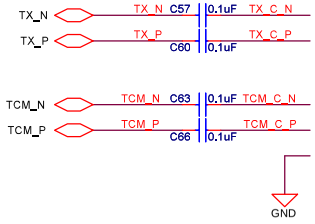








Diff. 100ohm trace design

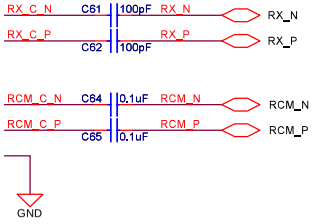


Differential 100ohm Characteristic Impedance cable

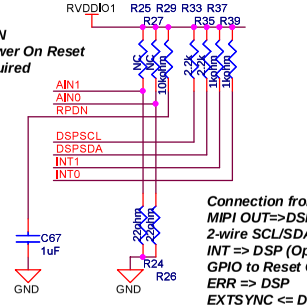
STP cable AWG26 over meters

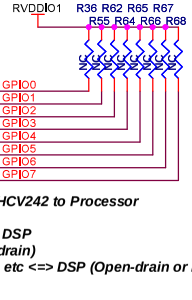
AC coupling capacitors on Main-Link trace are supposed to be changed depending on Data-rate

Diff. 100ohm trace design



PDN Power On Reset reruired





Connection from THCV242 to Processor
MIPI OUT=>DSP
2-wire SCL/SDA <= DSP
INT => DSP (Open-drain)
GPIO to Reset Cam etc <==> DSP (Open-drain or not)
ERR => DSP
EXTSYNC <= DSP
PDN <= Power On Reset

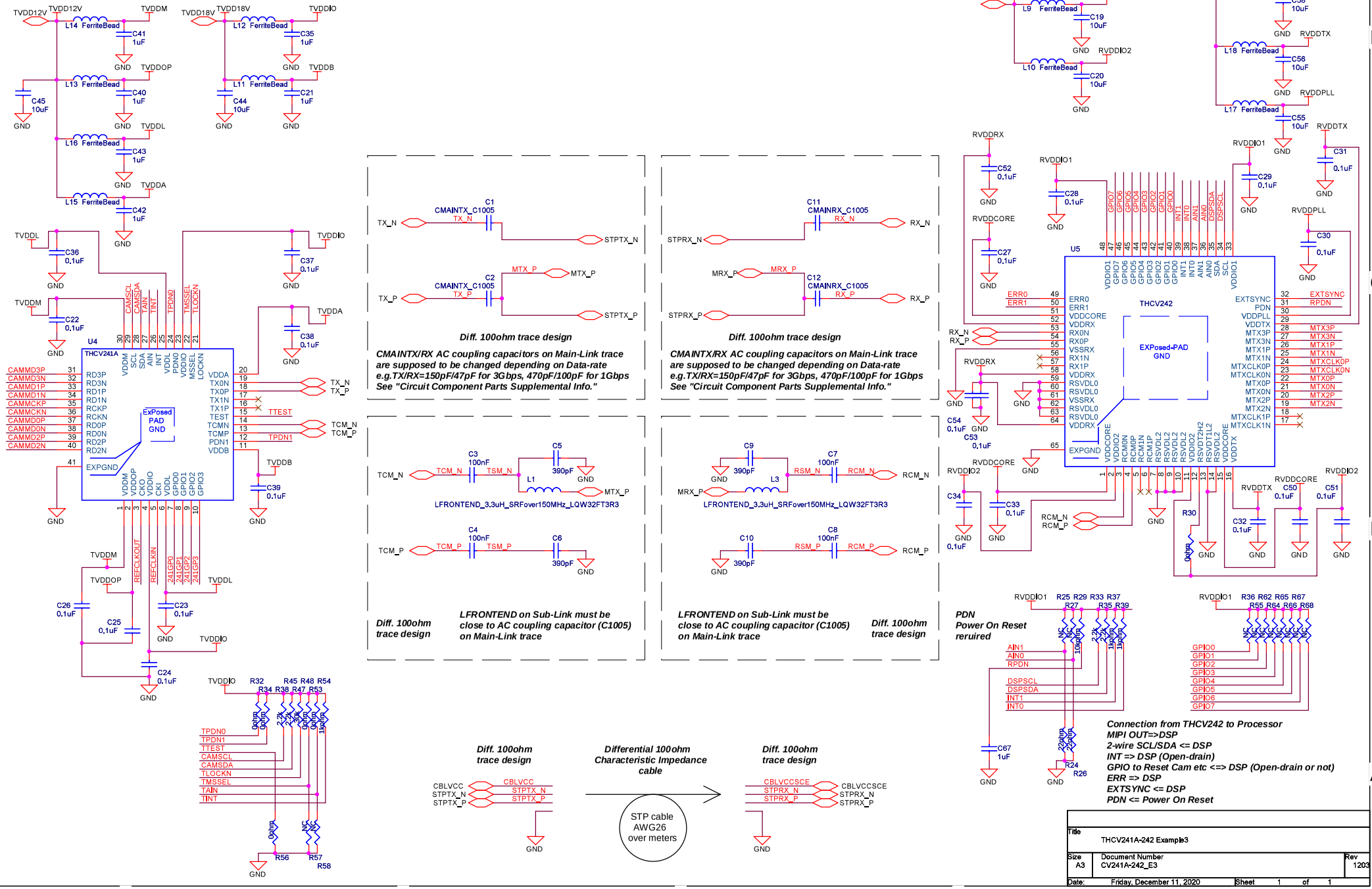
Title	THCV241A-242 Example2	
Size A3	Document Number CV241A-242_E2	Rev 1202
Date: Friday, December 11, 2020	Sheet 1 of 1	

Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <=> 2-wire SCL/SDA
Sensor/ISP <=> GPIO to Reset etc
Oscillator => CKI reference clock input
optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended



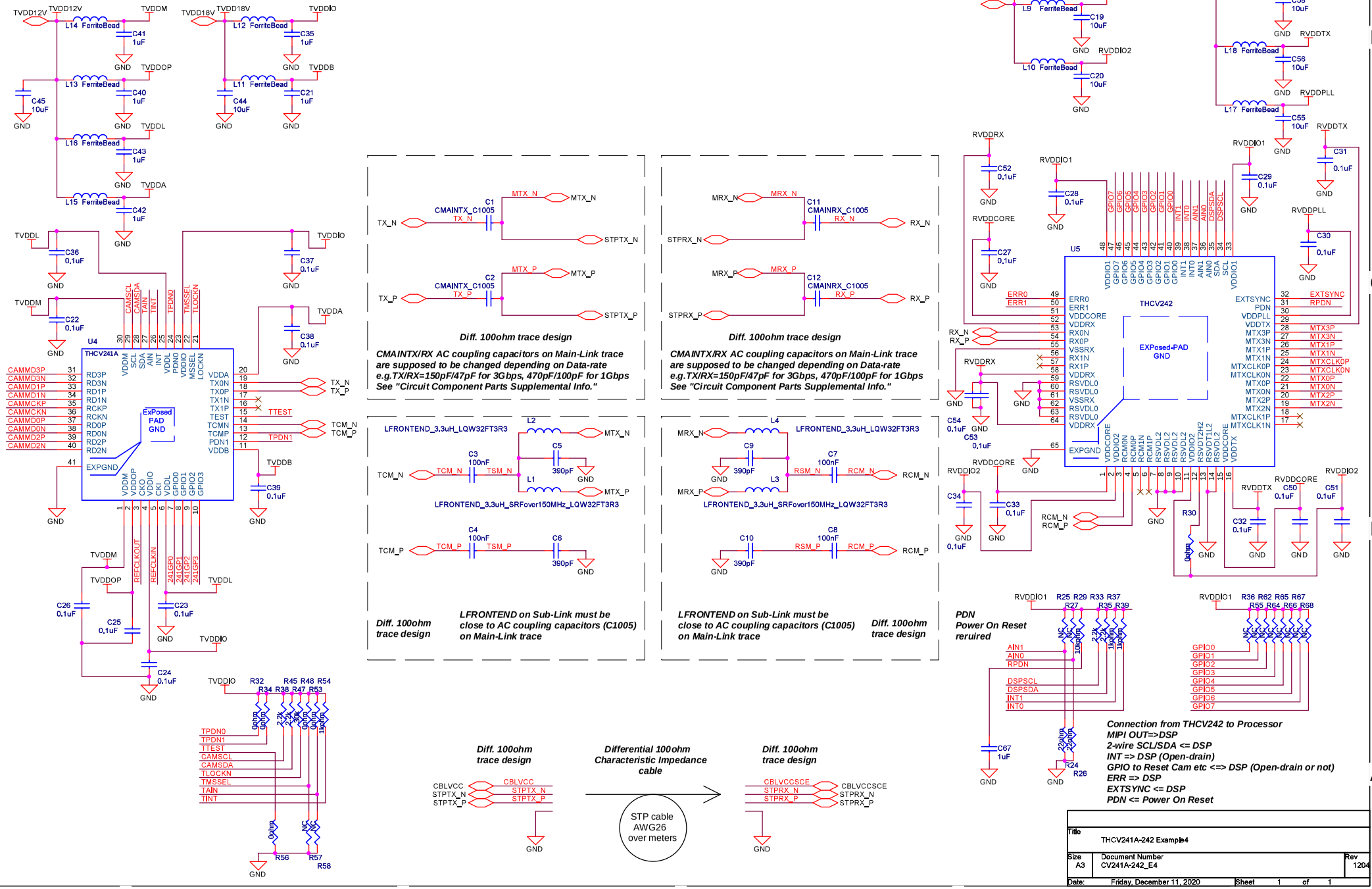
Title	THCV241A-242 Example3
Size	A3
Document Number	CV241A-242_E3
Rev	1203
Date:	Friday, December 11, 2020
Sheet	1 of 1

Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input
optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended



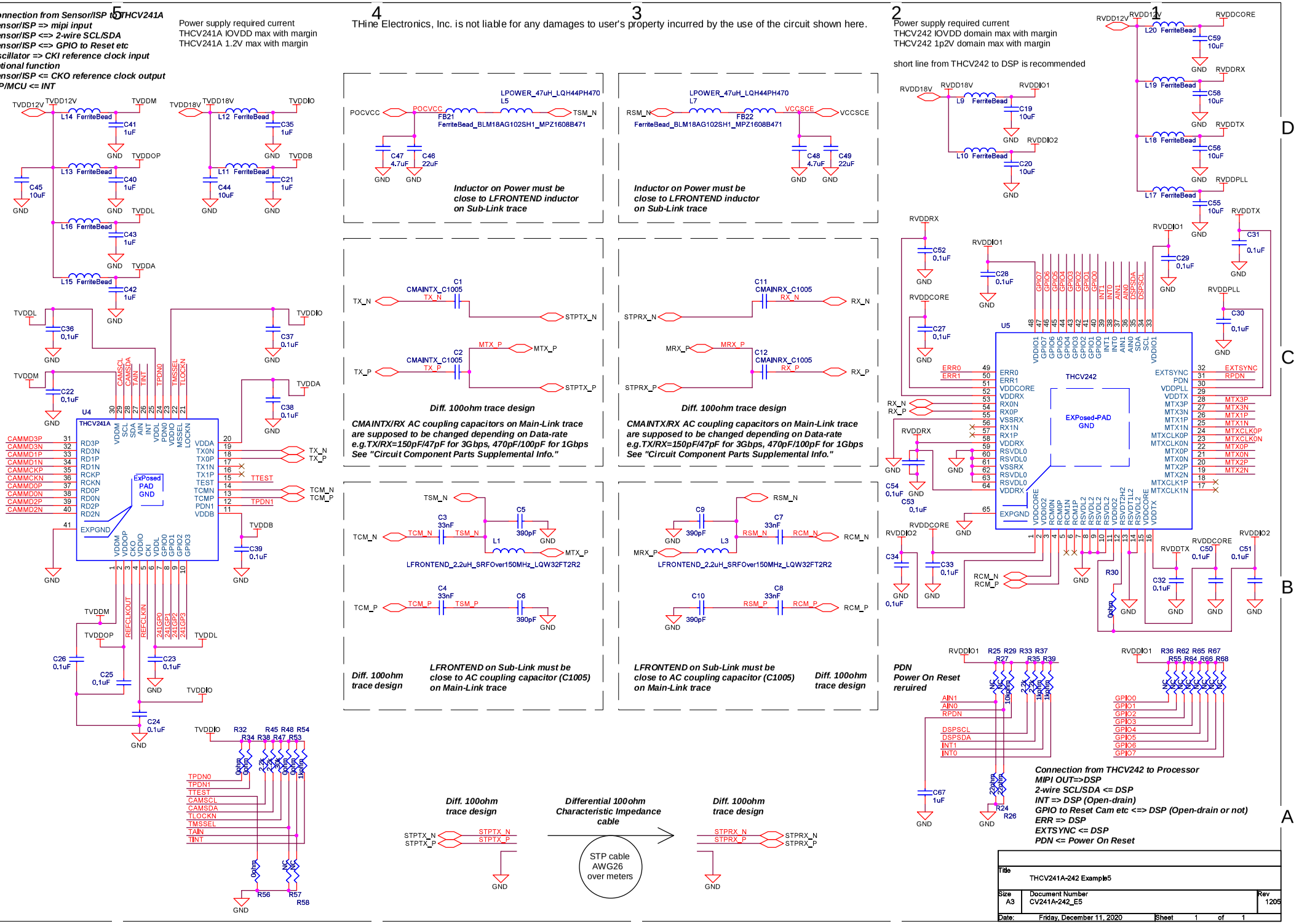
Title	THCV241A-242 Example4
Size	A3
Document Number	CV241A-242_E4
Rev	1204
Date:	Friday, December 11, 2020
Sheet	1 of 1

Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended



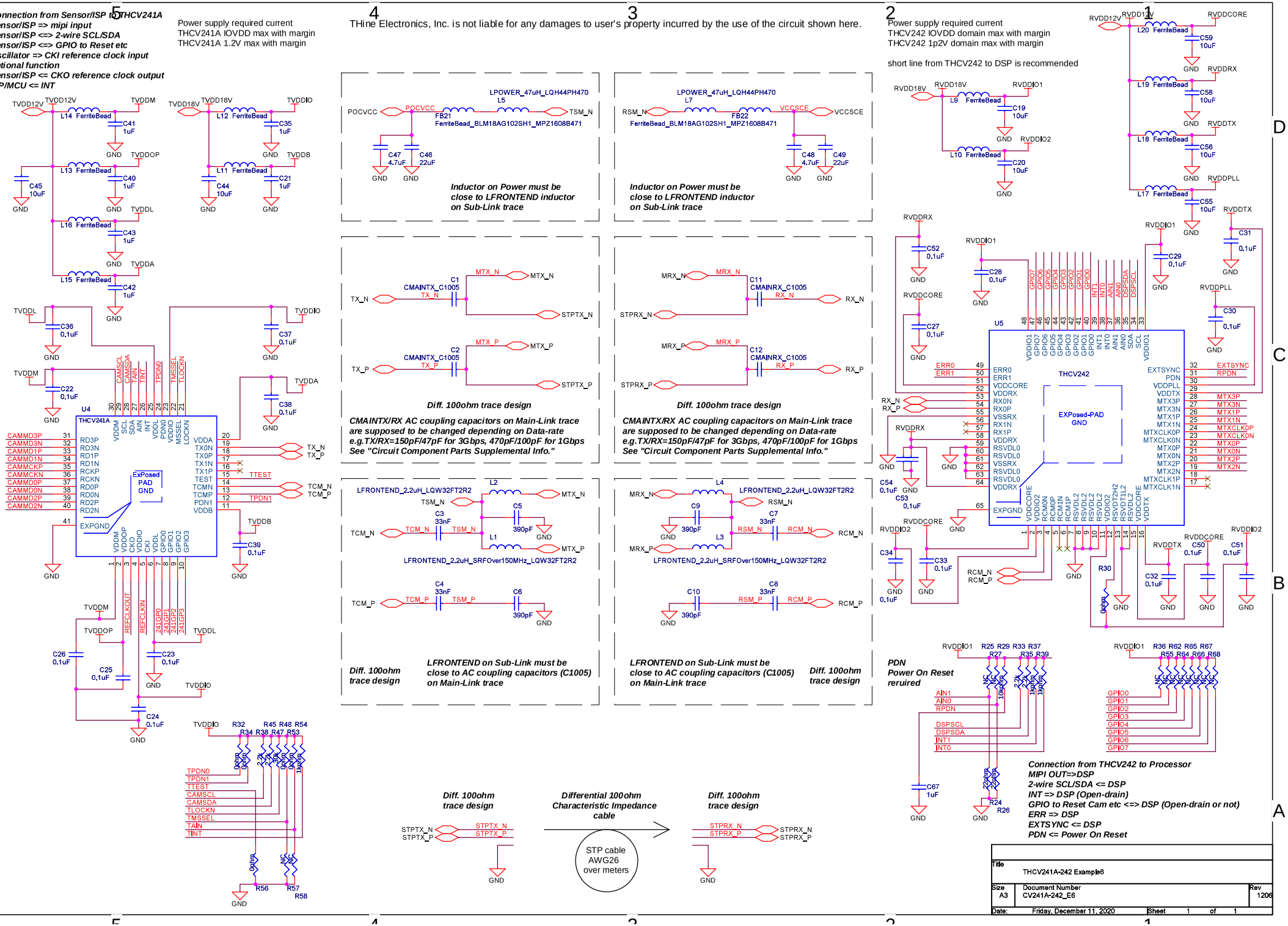
Title	THCV241A-242 Example5
Size	A3
Document Number	CV241A-242_E5
Rev	1205
Date:	Friday, December 11, 2020
Sheet	1 of 1

Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <=> 2-wire SCL/SDA
Sensor/ISP <=> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended



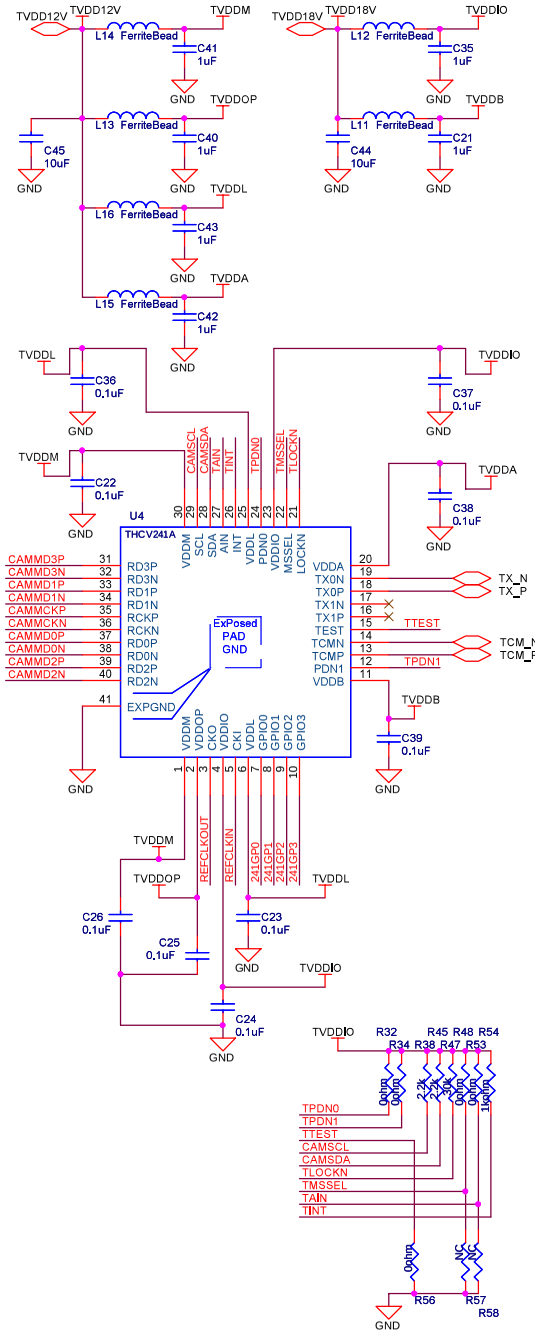
Title	THCV241A-242 Example
Size	A3
Document Number	CV241A-242_E6
Rev	1206
Date:	Friday, December 11, 2020
Sheet	1 of 1

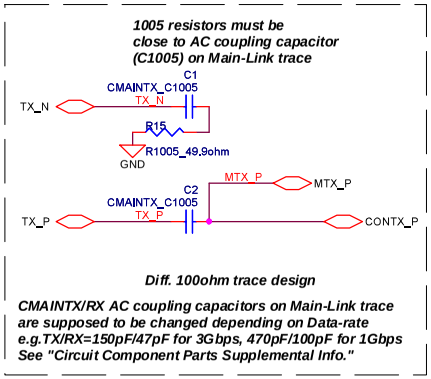
Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <=> 2-wire SCL/SDA
Sensor/ISP <=> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

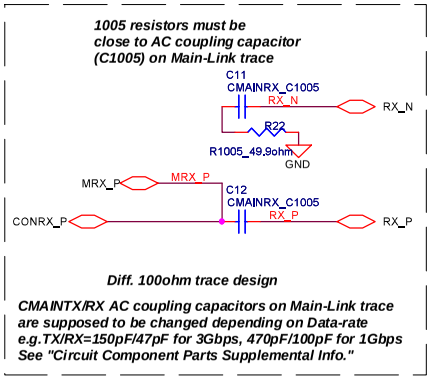
Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

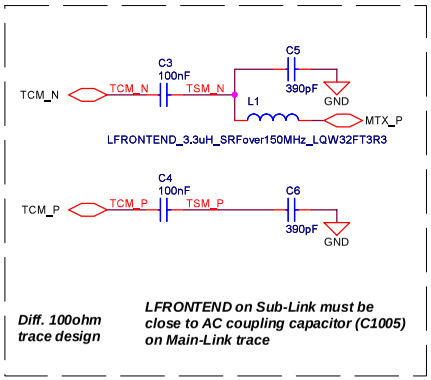
Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

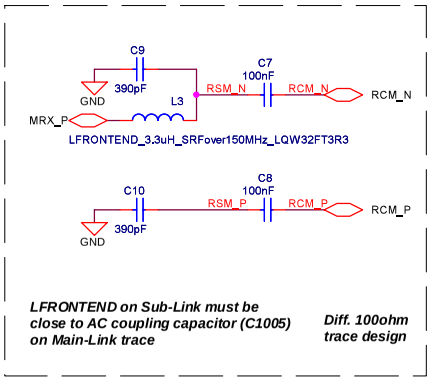
short line from THCV242 to DSP is recommended

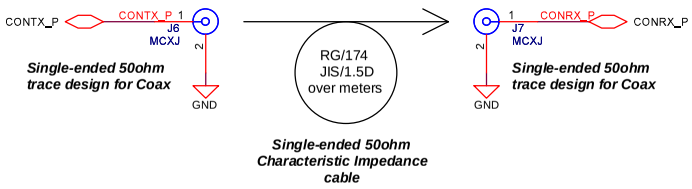


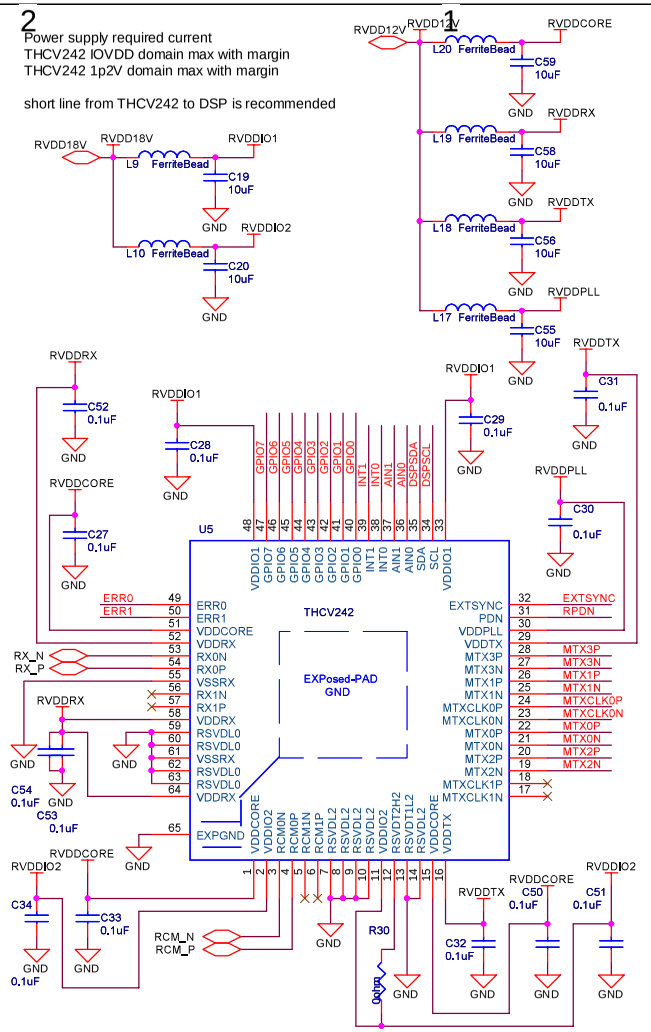


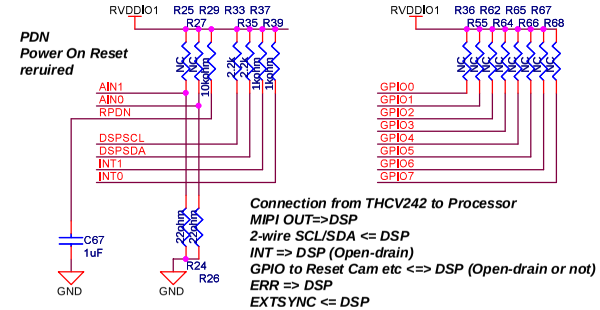












Connection from THCV242 to Processor
MIPI OUT=>DSP
2-wire SCL/SDA <= DSP
INT => DSP (Open-drain)
GPIO to Reset Cam etc <=> DSP (Open-drain or not)
ERR => DSP
EXTSYNC <= DSP
PDN <= Power On Reset

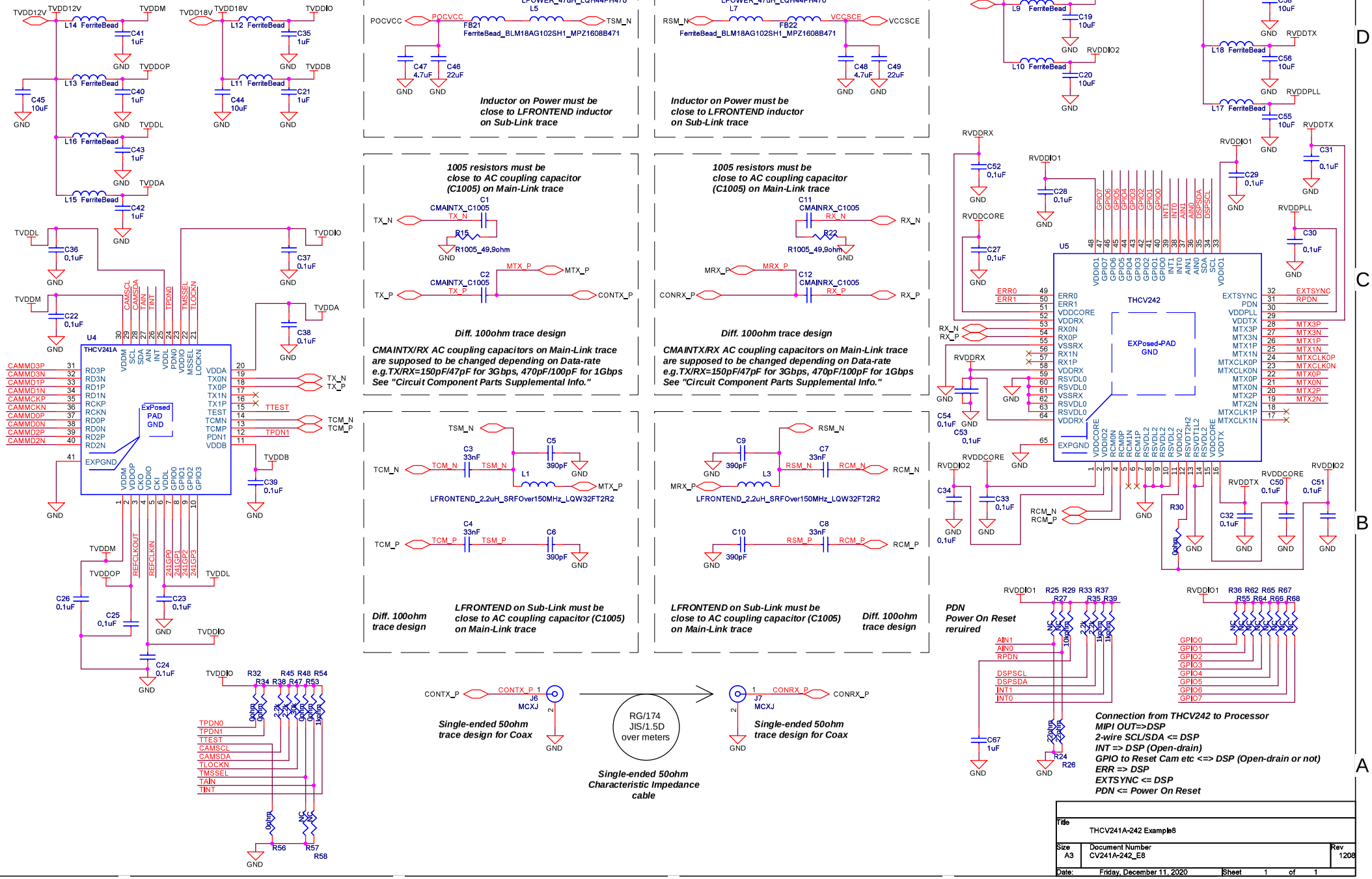
Title	THCV241A-242 Example7	
Size A3	Document Number CV241A-242_E7	Rev 1207
Date: Friday, December 11, 2020	Sheet 1 of 1	

Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended



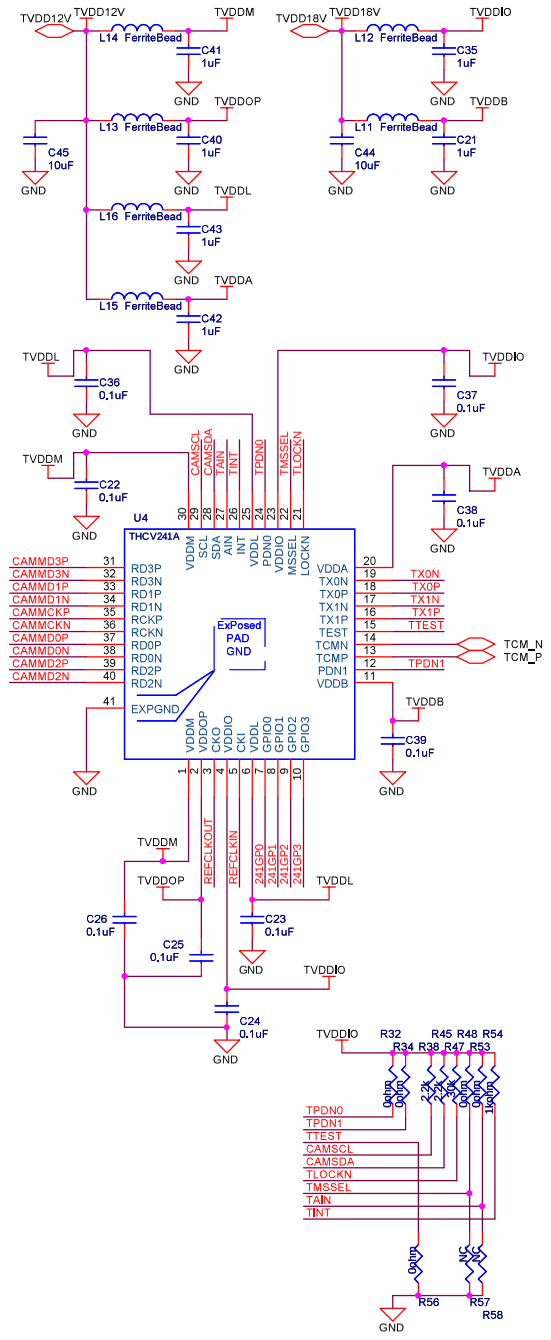
Title	THCV241A-242 Example	
Size A3	Document Number CV241A-242_E8	Rev 1208
Date: Friday, December 11, 2020	Sheet 1 of 1	

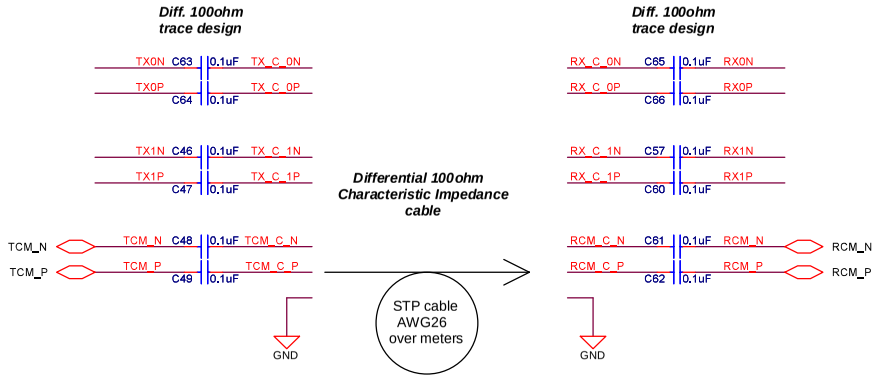
Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <==> 2-wire SCL/SDA
Sensor/ISP <==> GPIO to Reset etc
Oscillator => CKI reference clock input
optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

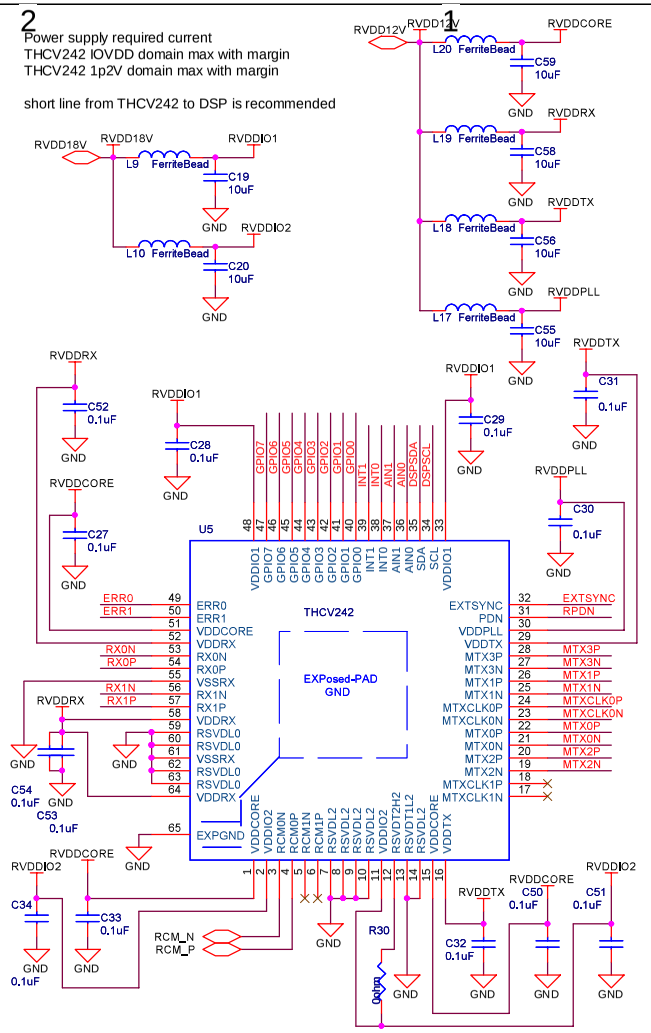
Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

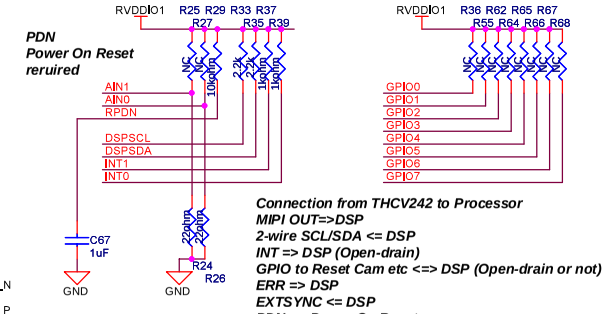
Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

short line from THCV242 to DSP is recommended









Connection from THCV242 to Processor
MIPI OUT=>DSP
2-wire SCL/SDA <= DSP
INT => DSP (Open-drain)
GPIO to Reset Cam etc <==> DSP (Open-drain or not)
ERR => DSP
EXTSYNC <= DSP
PDN <= Power On Reset

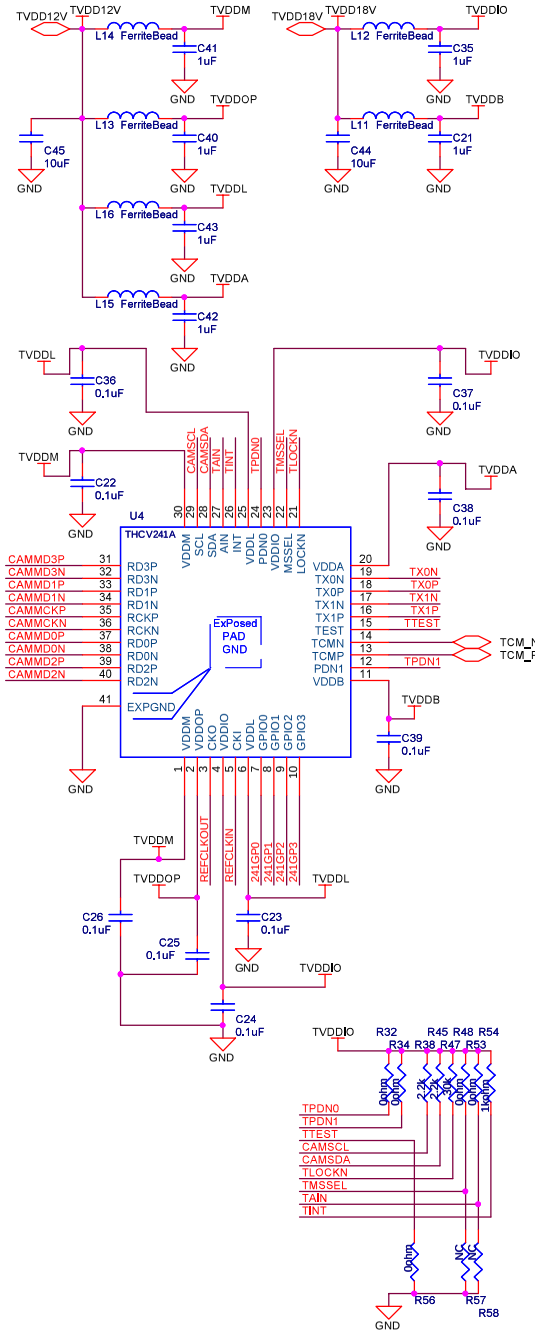
Title	THCV241A-242 Example9	
Size A3	Document Number CV241A-242_E9	Rev 1209
Date: Friday, December 11, 2020	Sheet 1 of 1	

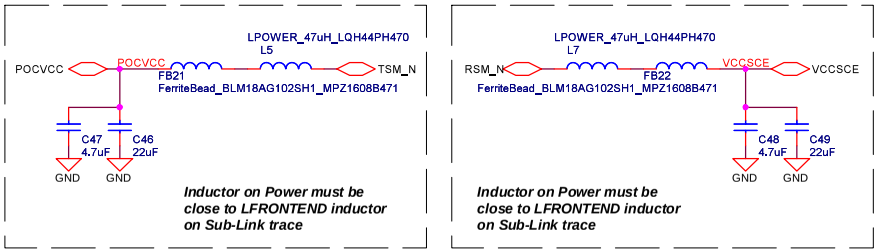
Connection from Sensor/ISP to THCV241A
Sensor/ISP => mipi input
Sensor/ISP <=> 2-wire SCL/SDA
Sensor/ISP <=> GPIO to Reset etc
Oscillator => CKI reference clock input optional function
Sensor/ISP <= CKO reference clock output
ISP/MCU <= INT

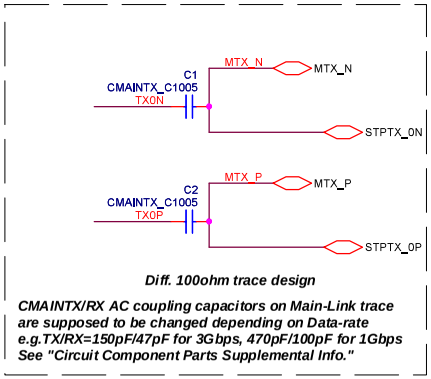
Power supply required current
THCV241A IOVDD max with margin
THCV241A 1.2V max with margin

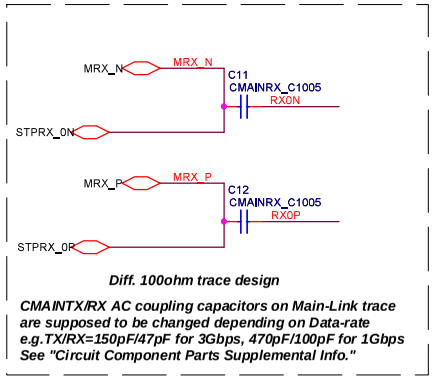
Power supply required current
THCV242 IOVDD domain max with margin
THCV242 1p2V domain max with margin

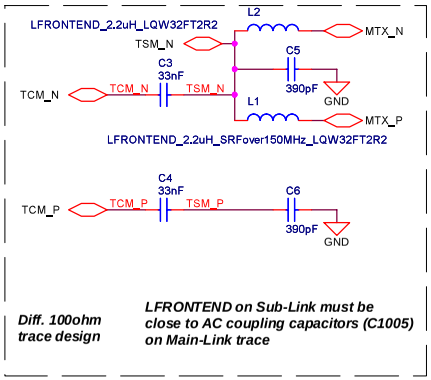
short line from THCV242 to DSP is recommended

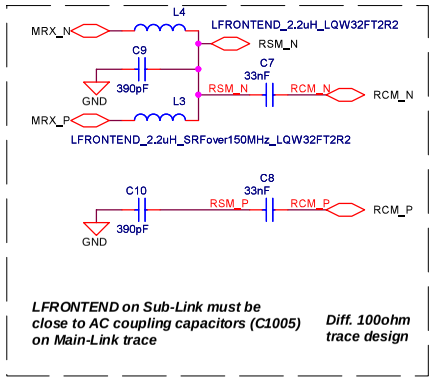


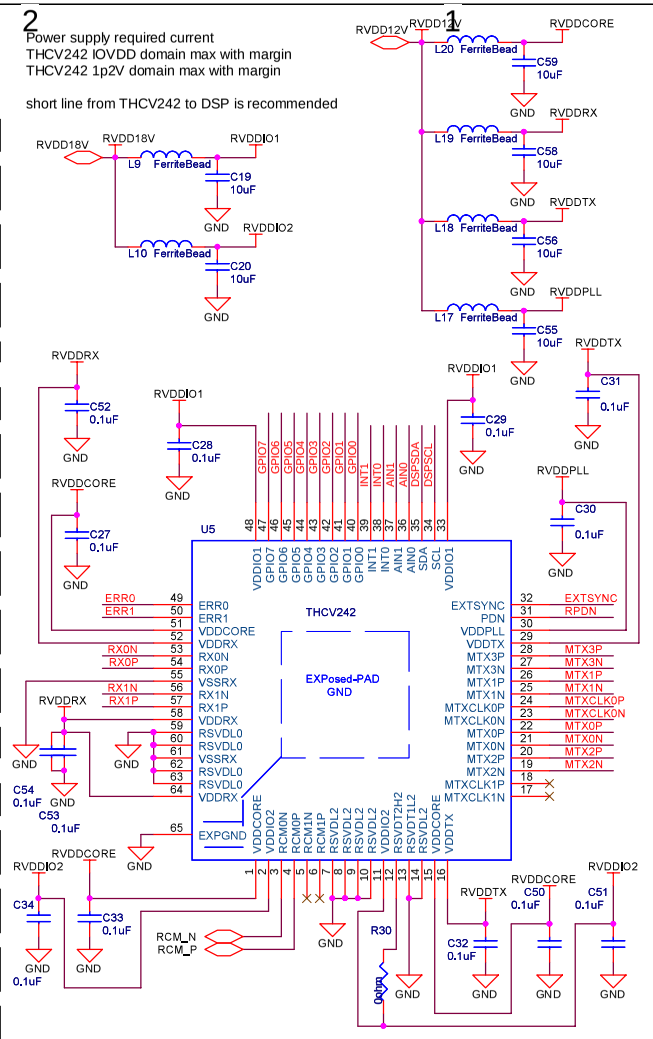


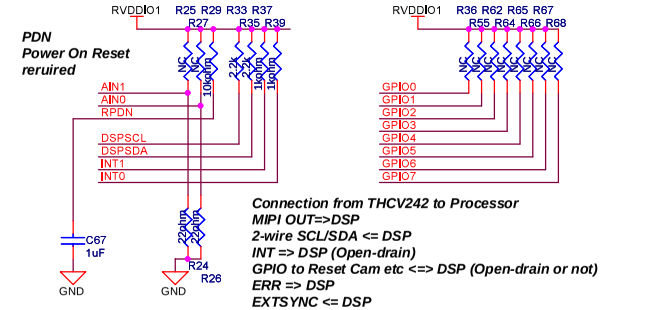


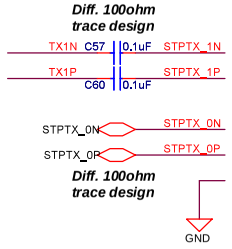






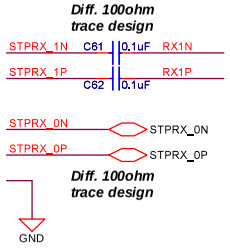






Differential 100ohm Characteristic Impedance cable
GND can be shell of connector

QTP cable AWG26 over meters



Title	THCV241A-242 Example10	
Size A3	Document Number CV241A-242_E10	Rev 1210
Date: Friday, December 11, 2020	Sheet 1 of 1	

Example Circuit Component Parts Supplemental Information

Additional informative information about example circuit is shown here.

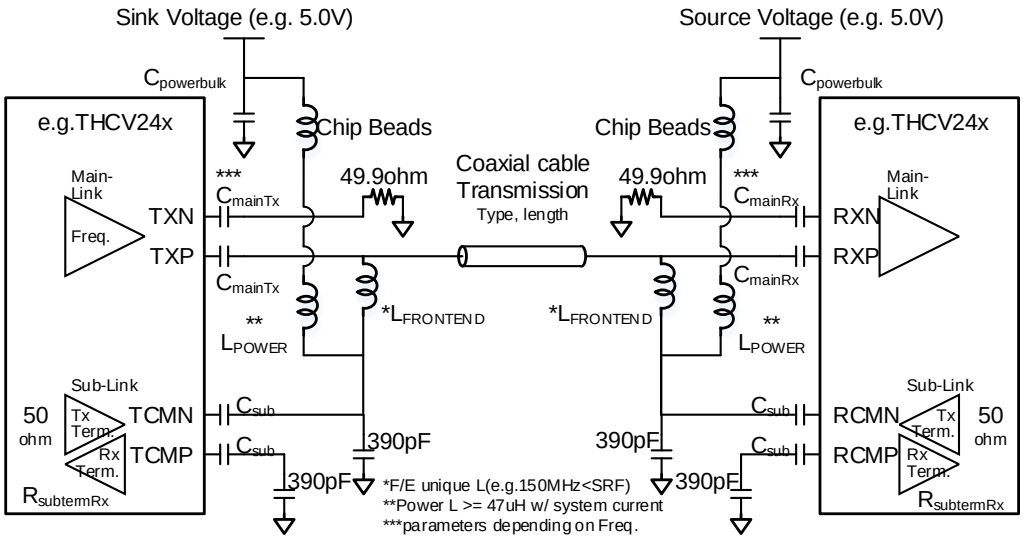


Figure 3 Example Schematic Diagram of Single-Line Configuration

$L_{FRONTEND}$ and L_{POWER} are key component for single line configuration. Some examples are introduced here.
$L_{FRONTEND}$ default guideline is 2.2uH in terms of robustness against whole system noise including power effect.
LFRONTEND is supposed to be equal or less than 3.3uH. Too small $L_{FRONTEND}$ is also unavailable.
L_{POWER} is supposed to be equal or more than 47uH.

Table 2 Example Inductor components

Symbol	Value	Maker	Part Number	Note
$L_{FRONTEND}$	2.2uH	Murata	LQW32FT2R2	AEC-Q200
	2.0uH	Murata	LQW21FT2R0	AEC-Q200
	3.3uH	Murata	LQW32FT3R3	AEC-Q200
	2.2uH	TDK	ADL2012-2R2M	AEC-Q200
	2.2uH	Taiyo Yuden	BRC2012T2R2MD	
	3.3uH	Taiyo Yuden	BRC2012T3R3MDV	Automotive
L_{POWER}	47uH	Murata	LQH44PH470MPR	AEC-Q200
	47uH	Murata	LQW32FT470	AEC-Q200
	47uH	TDK	VLS3015CX-470M-H	AEC-Q200
	47uH	Taiyo Yuden	BRL3225T470KV	Automotive

C_{mainTx} and C_{mainRx} are supposed to be properly selected depending on Main-Link Data-rate for single line configuration from 600Mbps to 4Gbps.

Table 3 Example Main-Link AC-coupling Capacitor components

	(pF)	(pF)	(pF)
(Mbps)	C_{mainTx}	C_{mainRx}	
Data-rate	available value	available value	available range
4000	150	47	47
3000	150	47	47
2250	150	47	47
1500	270	68	68-82
1250	470	82	68-100
1000	470	100	82-150
800	560	100	100-150
600	560	150	100-150

C_{sub} default guideline is 33nF in terms of robustness against whole system noise including power effect.
C_{sub} 100nF, which is easier to get in market, could be available.

$R_{subtermRx}$, Sub-Link PHY Rx PHY termination are controllable in THCV series register set.
$R_{subtermRx}$ default guideline is 200ohm(, where companion Sub-Link Rx PHY drive current is 3mA,) in terms of robustness against whole system noise including power effect.
$R_{subtermRx}$ 50ohm(, where companion Sub-Link Rx PHY drive current is 12mA,), which could affect termination condition aimed for EMC compatibility, could be available.

Main-Link data mapping reference (Parallel CMOS to V-by-One® HS Compatibility)

THCV231(-Q) (HFSEL=0) or THCV235(-Q) (HFSEL=0) to THCV242 pin assignment example

THCV242 V-by-One® HS standard format is used. THCV231/5(-Q) V-by-One® HS Mode is used. THCV231/5(-Q) COL1=0 and LFSEL=0 are also required.

THCV231/235 Pins	Format Name	RGB888	YUV422				
HFSEL=0	Vx1HS std. Packer Packet ref.		Normal Mode1	Normal Mode2	Normal Mode3	Demux Mode1	Demux Mode2
D[31]	V-by-One®HS_D[31]	0	0	0	0	Y[7](1st pixel)	Cb[7]
D[30]	V-by-One®HS_D[30]	0	0	0	0	Y[6](1st pixel)	Cb[6]
D[29]	V-by-One®HS_D[29]	0	0	0	0	Y[5](1st pixel)	Cb[5]
D[28]	V-by-One®HS_D[28]	0	0	0	0	Y[4](1st pixel)	Cb[4]
D[27]	V-by-One®HS_D[27]	0	0	0	0	Y[3](1st pixel)	Cb[3]
D[26]	V-by-One®HS_D[26]	0	0	0	0	Y[2](1st pixel)	Cb[2]
D[25]	V-by-One®HS_D[25]	0	0	0	0	Y[1](1st pixel)	Cb[1]
D[24]	V-by-One®HS_D[24]	0	0	0	0	Y[0](1st pixel)	Cb[0]
D[23]	V-by-One®HS_D[23]	B[7]	0	Cb[7]/Cr[7]	Y[7]	Cb[7]	Y[7](1st pixel)
D[22]	V-by-One®HS_D[22]	B[6]	0	Cb[6]/Cr[6]	Y[6]	Cb[6]	Y[6](1st pixel)
D[21]	V-by-One®HS_D[21]	B[5]	0	Cb[5]/Cr[5]	Y[5]	Cb[5]	Y[5](1st pixel)
D[20]	V-by-One®HS_D[20]	B[4]	0	Cb[4]/Cr[4]	Y[4]	Cb[4]	Y[4](1st pixel)
D[19]	V-by-One®HS_D[19]	B[3]	0	Cb[3]/Cr[3]	Y[3]	Cb[3]	Y[3](1st pixel)
D[18]	V-by-One®HS_D[18]	B[2]	0	Cb[2]/Cr[2]	Y[2]	Cb[2]	Y[2](1st pixel)
D[17]	V-by-One®HS_D[17]	B[1]	0	Cb[1]/Cr[1]	Y[1]	Cb[1]	Y[1](1st pixel)
D[16]	V-by-One®HS_D[16]	B[0]	0	Cb[0]/Cr[0]	Y[0]	Cb[0]	Y[0](1st pixel)
D[15]	V-by-One®HS_D[15]	G[7]	Y[7]	0	0	Y[7](2nd pixel)	Cr[7]
D[14]	V-by-One®HS_D[14]	G[6]	Y[6]	0	0	Y[6](2nd pixel)	Cr[6]
D[13]	V-by-One®HS_D[13]	G[5]	Y[5]	0	0	Y[5](2nd pixel)	Cr[5]
D[12]	V-by-One®HS_D[12]	G[4]	Y[4]	0	0	Y[4](2nd pixel)	Cr[4]
D[11]	V-by-One®HS_D[11]	G[3]	Y[3]	0	0	Y[3](2nd pixel)	Cr[3]
D[10]	V-by-One®HS_D[10]	G[2]	Y[2]	0	0	Y[2](2nd pixel)	Cr[2]
D[9]	V-by-One®HS_D[9]	G[1]	Y[1]	0	0	Y[1](2nd pixel)	Cr[1]
D[8]	V-by-One®HS_D[8]	G[0]	Y[0]	0	0	Y[0](2nd pixel)	Cr[0]
D[7]	V-by-One®HS_D[7]	R[7]	Cb[7]/Cr[7]	Y[7]	Cb[7]/Cr[7]	Cr[7]	Y[7](2nd pixel)
D[6]	V-by-One®HS_D[6]	R[6]	Cb[6]/Cr[6]	Y[6]	Cb[6]/Cr[6]	Cr[6]	Y[6](2nd pixel)
D[5]	V-by-One®HS_D[5]	R[5]	Cb[5]/Cr[5]	Y[5]	Cb[5]/Cr[5]	Cr[5]	Y[5](2nd pixel)
D[4]	V-by-One®HS_D[4]	R[4]	Cb[4]/Cr[4]	Y[4]	Cb[4]/Cr[4]	Cr[4]	Y[4](2nd pixel)
D[3]	V-by-One®HS_D[3]	R[3]	Cb[3]/Cr[3]	Y[3]	Cb[3]/Cr[3]	Cr[3]	Y[3](2nd pixel)
D[2]	V-by-One®HS_D[2]	R[2]	Cb[2]/Cr[2]	Y[2]	Cb[2]/Cr[2]	Cr[2]	Y[2](2nd pixel)
D[1]	V-by-One®HS_D[1]	R[1]	Cb[1]/Cr[1]	Y[1]	Cb[1]/Cr[1]	Cr[1]	Y[1](2nd pixel)
D[0]	V-by-One®HS_D[0]	R[0]	Cb[0]/Cr[0]	Y[0]	Cb[0]/Cr[0]	Cr[0]	Y[0](2nd pixel)

THCV231/235 Pins	Format Name	RAW8		
HFSEL=0	Vx1HS std. Packer Packet ref.	Normal Mode1	Normal Mode2	Demux Mode1
D[31]	V-by-One®HS_D[31]	0	0	RAW[7] (2nd pixel)
D[30]	V-by-One®HS_D[30]	0	0	RAW[6] (2nd pixel)
D[29]	V-by-One®HS_D[29]	0	0	RAW[5] (2nd pixel)
D[28]	V-by-One®HS_D[28]	0	0	RAW[4] (2nd pixel)
D[27]	V-by-One®HS_D[27]	0	0	RAW[3] (2nd pixel)
D[26]	V-by-One®HS_D[26]	0	0	RAW[2] (2nd pixel)
D[25]	V-by-One®HS_D[25]	0	0	RAW[1] (2nd pixel)
D[24]	V-by-One®HS_D[24]	0	0	RAW[0] (2nd pixel)
D[23]	V-by-One®HS_D[23]	0	RAW[7] (1st pixel)	RAW[7] (1st pixel)
D[22]	V-by-One®HS_D[22]	0	RAW[6] (1st pixel)	RAW[6] (1st pixel)
D[21]	V-by-One®HS_D[21]	0	RAW[5] (1st pixel)	RAW[5] (1st pixel)
D[20]	V-by-One®HS_D[20]	0	RAW[4] (1st pixel)	RAW[4] (1st pixel)
D[19]	V-by-One®HS_D[19]	0	RAW[3] (1st pixel)	RAW[3] (1st pixel)
D[18]	V-by-One®HS_D[18]	0	RAW[2] (1st pixel)	RAW[2] (1st pixel)
D[17]	V-by-One®HS_D[17]	0	RAW[1] (1st pixel)	RAW[1] (1st pixel)
D[16]	V-by-One®HS_D[16]	0	RAW[0] (1st pixel)	RAW[0] (1st pixel)
D[15]	V-by-One®HS_D[15]	RAW[7] (2nd pixel)	0	RAW[7] (4th pixel)
D[14]	V-by-One®HS_D[14]	RAW[6] (2nd pixel)	0	RAW[6] (4th pixel)
D[13]	V-by-One®HS_D[13]	RAW[5] (2nd pixel)	0	RAW[5] (4th pixel)
D[12]	V-by-One®HS_D[12]	RAW[4] (2nd pixel)	0	RAW[4] (4th pixel)
D[11]	V-by-One®HS_D[11]	RAW[3] (2nd pixel)	0	RAW[3] (4th pixel)
D[10]	V-by-One®HS_D[10]	RAW[2] (2nd pixel)	0	RAW[2] (4th pixel)
D[9]	V-by-One®HS_D[9]	RAW[1] (2nd pixel)	0	RAW[1] (4th pixel)
D[8]	V-by-One®HS_D[8]	RAW[0] (2nd pixel)	0	RAW[0] (4th pixel)
D[7]	V-by-One®HS_D[7]	RAW[7] (1st pixel)	RAW[7] (2nd pixel)	RAW[7] (3rd pixel)
D[6]	V-by-One®HS_D[6]	RAW[6] (1st pixel)	RAW[6] (2nd pixel)	RAW[6] (3rd pixel)
D[5]	V-by-One®HS_D[5]	RAW[5] (1st pixel)	RAW[5] (2nd pixel)	RAW[5] (3rd pixel)
D[4]	V-by-One®HS_D[4]	RAW[4] (1st pixel)	RAW[4] (2nd pixel)	RAW[4] (3rd pixel)
D[3]	V-by-One®HS_D[3]	RAW[3] (1st pixel)	RAW[3] (2nd pixel)	RAW[3] (3rd pixel)
D[2]	V-by-One®HS_D[2]	RAW[2] (1st pixel)	RAW[2] (2nd pixel)	RAW[2] (3rd pixel)
D[1]	V-by-One®HS_D[1]	RAW[1] (1st pixel)	RAW[1] (2nd pixel)	RAW[1] (3rd pixel)
D[0]	V-by-One®HS_D[0]	RAW[0] (1st pixel)	RAW[0] (2nd pixel)	RAW[0] (3rd pixel)

THCV231/235 Pins	Format Name	RAW10		
HFSEL=0	Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
D[31]	V-by-One®HS_D[31]	0	0	0
D[30]	V-by-One®HS_D[30]	0	0	0
D[29]	V-by-One®HS_D[29]	0	0	0
D[28]	V-by-One®HS_D[28]	0	0	0
D[27]	V-by-One®HS_D[27]	0	0	0
D[26]	V-by-One®HS_D[26]	0	0	0
D[25]	V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
D[24]	V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
D[23]	V-by-One®HS_D[23]	0	RAW[9](1st pixel)	0
D[22]	V-by-One®HS_D[22]	0	RAW[8](1st pixel)	0
D[21]	V-by-One®HS_D[21]	0	RAW[7](1st pixel)	RAW[1](1st pixel)
D[20]	V-by-One®HS_D[20]	0	RAW[6](1st pixel)	RAW[0](1st pixel)
D[19]	V-by-One®HS_D[19]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
D[18]	V-by-One®HS_D[18]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
D[17]	V-by-One®HS_D[17]	0	RAW[3](1st pixel)	RAW[7](1st pixel)
D[16]	V-by-One®HS_D[16]	0	RAW[2](1st pixel)	RAW[6](1st pixel)
D[15]	V-by-One®HS_D[15]	0	0	RAW[5](1st pixel)
D[14]	V-by-One®HS_D[14]	0	0	RAW[4](1st pixel)
D[13]	V-by-One®HS_D[13]	0	0	RAW[3](1st pixel)
D[12]	V-by-One®HS_D[12]	0	0	RAW[2](1st pixel)
D[11]	V-by-One®HS_D[11]	0	0	0
D[10]	V-by-One®HS_D[10]	0	0	0
D[9]	V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
D[8]	V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
D[7]	V-by-One®HS_D[7]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
D[6]	V-by-One®HS_D[6]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
D[5]	V-by-One®HS_D[5]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
D[4]	V-by-One®HS_D[4]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
D[3]	V-by-One®HS_D[3]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
D[2]	V-by-One®HS_D[2]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)
D[1]	V-by-One®HS_D[1]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
D[0]	V-by-One®HS_D[0]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)

THCV231/235 Pins	Format Name	RAW12		
HFSEL=0	Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
D[31]	V-by-One®HS_D[31]	0	0	0
D[30]	V-by-One®HS_D[30]	0	0	0
D[29]	V-by-One®HS_D[29]	0	0	0
D[28]	V-by-One®HS_D[28]	0	0	0
D[27]	V-by-One®HS_D[27]	0	RAW[3](1st pixel)	0
D[26]	V-by-One®HS_D[26]	0	RAW[2](1st pixel)	0
D[25]	V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
D[24]	V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
D[23]	V-by-One®HS_D[23]	0	RAW[11](1st pixel)	RAW[3](1st pixel)
D[22]	V-by-One®HS_D[22]	0	RAW[10](1st pixel)	RAW[2](1st pixel)
D[21]	V-by-One®HS_D[21]	0	RAW[9](1st pixel)	RAW[1](1st pixel)
D[20]	V-by-One®HS_D[20]	0	RAW[8](1st pixel)	RAW[0](1st pixel)
D[19]	V-by-One®HS_D[19]	0	RAW[7](1st pixel)	RAW[11](1st pixel)
D[18]	V-by-One®HS_D[18]	0	RAW[6](1st pixel)	RAW[10](1st pixel)
D[17]	V-by-One®HS_D[17]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
D[16]	V-by-One®HS_D[16]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
D[15]	V-by-One®HS_D[15]	0	0	RAW[7](1st pixel)
D[14]	V-by-One®HS_D[14]	0	0	RAW[6](1st pixel)
D[13]	V-by-One®HS_D[13]	0	0	RAW[5](1st pixel)
D[12]	V-by-One®HS_D[12]	0	0	RAW[4](1st pixel)
D[11]	V-by-One®HS_D[11]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
D[10]	V-by-One®HS_D[10]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)
D[9]	V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
D[8]	V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
D[7]	V-by-One®HS_D[7]	RAW[11]	RAW[11](2nd pixel)	RAW[11](2nd pixel)
D[6]	V-by-One®HS_D[6]	RAW[10]	RAW[10](2nd pixel)	RAW[10](2nd pixel)
D[5]	V-by-One®HS_D[5]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
D[4]	V-by-One®HS_D[4]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
D[3]	V-by-One®HS_D[3]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
D[2]	V-by-One®HS_D[2]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
D[1]	V-by-One®HS_D[1]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
D[0]	V-by-One®HS_D[0]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)

THCV231 (HFSEL=1) or THCV235 (HFSEL=1) to THCV242 pin assignment example

THCV242 V-by-One® HS standard format is used. Formats with dark cell in below table cannot be used. Basically 4Byte Mode is required. Particular mode of THCV231-Q allows 3Byte Mode.
THCV231/5(-Q) V-by-One® HS Mode is used. THCV231/5(-Q) COL1=0 and LFSEL=0 are also required.

THCV231/235 Pins	Format Name	RGB888	YUV422				
HFSEL=1	Vx1HS std. Packer Packet ref.		Normal Mode1	Normal Mode2	Normal Mode3	Demux Mode1	Demux Mode2
D[15](1st)	V-by-One®HS_D[31]	0	0	0	0	Y[7](1st pixel)	Cb[7]
D[14](1st)	V-by-One®HS_D[30]	0	0	0	0	Y[6](1st pixel)	Cb[6]
D[13](1st)	V-by-One®HS_D[29]	0	0	0	0	Y[5](1st pixel)	Cb[5]
D[12](1st)	V-by-One®HS_D[28]	0	0	0	0	Y[4](1st pixel)	Cb[4]
D[11](1st)	V-by-One®HS_D[27]	0	0	0	0	Y[3](1st pixel)	Cb[3]
D[10](1st)	V-by-One®HS_D[26]	0	0	0	0	Y[2](1st pixel)	Cb[2]
D[9](1st)	V-by-One®HS_D[25]	0	0	0	0	Y[1](1st pixel)	Cb[1]
D[8](1st)	V-by-One®HS_D[24]	0	0	0	0	Y[0](1st pixel)	Cb[0]
D[7](1st)	V-by-One®HS_D[23]	B[7]	0	Cb[7]/Cr[7]	Y[7]	Cb[7]	Y[7](1st pixel)
D[6](1st)	V-by-One®HS_D[22]	B[6]	0	Cb[6]/Cr[6]	Y[6]	Cb[6]	Y[6](1st pixel)
D[5](1st)	V-by-One®HS_D[21]	B[5]	0	Cb[5]/Cr[5]	Y[5]	Cb[5]	Y[5](1st pixel)
D[4](1st)	V-by-One®HS_D[20]	B[4]	0	Cb[4]/Cr[4]	Y[4]	Cb[4]	Y[4](1st pixel)
D[3](1st)	V-by-One®HS_D[19]	B[3]	0	Cb[3]/Cr[3]	Y[3]	Cb[3]	Y[3](1st pixel)
D[2](1st)	V-by-One®HS_D[18]	B[2]	0	Cb[2]/Cr[2]	Y[2]	Cb[2]	Y[2](1st pixel)
D[1](1st)	V-by-One®HS_D[17]	B[1]	0	Cb[1]/Cr[1]	Y[1]	Cb[1]	Y[1](1st pixel)
D[0](1st)	V-by-One®HS_D[16]	B[0]	0	Cb[0]/Cr[0]	Y[0]	Cb[0]	Y[0](1st pixel)
D[15](2nd)	V-by-One®HS_D[15]	G[7]	Y[7]	0	0	Y[7](2nd pixel)	Cr[7]
D[14](2nd)	V-by-One®HS_D[14]	G[6]	Y[6]	0	0	Y[6](2nd pixel)	Cr[6]
D[13](2nd)	V-by-One®HS_D[13]	G[5]	Y[5]	0	0	Y[5](2nd pixel)	Cr[5]
D[12](2nd)	V-by-One®HS_D[12]	G[4]	Y[4]	0	0	Y[4](2nd pixel)	Cr[4]
D[11](2nd)	V-by-One®HS_D[11]	G[3]	Y[3]	0	0	Y[3](2nd pixel)	Cr[3]
D[10](2nd)	V-by-One®HS_D[10]	G[2]	Y[2]	0	0	Y[2](2nd pixel)	Cr[2]
D[9](2nd)	V-by-One®HS_D[9]	G[1]	Y[1]	0	0	Y[1](2nd pixel)	Cr[1]
D[8](2nd)	V-by-One®HS_D[8]	G[0]	Y[0]	0	0	Y[0](2nd pixel)	Cr[0]
D[7](2nd)	V-by-One®HS_D[7]	R[7]	Cb[7]/Cr[7]	Y[7]	Cb[7]/Cr[7]	Cr[7]	Y[7](2nd pixel)
D[6](2nd)	V-by-One®HS_D[6]	R[6]	Cb[6]/Cr[6]	Y[6]	Cb[6]/Cr[6]	Cr[6]	Y[6](2nd pixel)
D[5](2nd)	V-by-One®HS_D[5]	R[5]	Cb[5]/Cr[5]	Y[5]	Cb[5]/Cr[5]	Cr[5]	Y[5](2nd pixel)
D[4](2nd)	V-by-One®HS_D[4]	R[4]	Cb[4]/Cr[4]	Y[4]	Cb[4]/Cr[4]	Cr[4]	Y[4](2nd pixel)
D[3](2nd)	V-by-One®HS_D[3]	R[3]	Cb[3]/Cr[3]	Y[3]	Cb[3]/Cr[3]	Cr[3]	Y[3](2nd pixel)
D[2](2nd)	V-by-One®HS_D[2]	R[2]	Cb[2]/Cr[2]	Y[2]	Cb[2]/Cr[2]	Cr[2]	Y[2](2nd pixel)
D[1](2nd)	V-by-One®HS_D[1]	R[1]	Cb[1]/Cr[1]	Y[1]	Cb[1]/Cr[1]	Cr[1]	Y[1](2nd pixel)
D[0](2nd)	V-by-One®HS_D[0]	R[0]	Cb[0]/Cr[0]	Y[0]	Cb[0]/Cr[0]	Cr[0]	Y[0](2nd pixel)

THCV231/235 Pins	Format Name	RAW8		
HFSEL=1	Vx1HS std. Packer Packet ref.	Normal Mode1	Normal Mode2	Demux Mode1
D[15](1st)	V-by-One®HS_D[31]	0	0	RAW[7] (2nd pixel)
D[14](1st)	V-by-One®HS_D[30]	0	0	RAW[6] (2nd pixel)
D[13](1st)	V-by-One®HS_D[29]	0	0	RAW[5] (2nd pixel)
D[12](1st)	V-by-One®HS_D[28]	0	0	RAW[4] (2nd pixel)
D[11](1st)	V-by-One®HS_D[27]	0	0	RAW[3] (2nd pixel)
D[10](1st)	V-by-One®HS_D[26]	0	0	RAW[2] (2nd pixel)
D[9](1st)	V-by-One®HS_D[25]	0	0	RAW[1] (2nd pixel)
D[8](1st)	V-by-One®HS_D[24]	0	0	RAW[0] (2nd pixel)
D[7](1st)	V-by-One®HS_D[23]	0	RAW[7] (1st pixel)	RAW[7] (1st pixel)
D[6](1st)	V-by-One®HS_D[22]	0	RAW[6] (1st pixel)	RAW[6] (1st pixel)
D[5](1st)	V-by-One®HS_D[21]	0	RAW[5] (1st pixel)	RAW[5] (1st pixel)
D[4](1st)	V-by-One®HS_D[20]	0	RAW[4] (1st pixel)	RAW[4] (1st pixel)
D[3](1st)	V-by-One®HS_D[19]	0	RAW[3] (1st pixel)	RAW[3] (1st pixel)
D[2](1st)	V-by-One®HS_D[18]	0	RAW[2] (1st pixel)	RAW[2] (1st pixel)
D[1](1st)	V-by-One®HS_D[17]	0	RAW[1] (1st pixel)	RAW[1] (1st pixel)
D[0](1st)	V-by-One®HS_D[16]	0	RAW[0] (1st pixel)	RAW[0] (1st pixel)
D[15](2nd)	V-by-One®HS_D[15]	RAW[7] (2nd pixel)	0	RAW[7] (4th pixel)
D[14](2nd)	V-by-One®HS_D[14]	RAW[6] (2nd pixel)	0	RAW[6] (4th pixel)
D[13](2nd)	V-by-One®HS_D[13]	RAW[5] (2nd pixel)	0	RAW[5] (4th pixel)
D[12](2nd)	V-by-One®HS_D[12]	RAW[4] (2nd pixel)	0	RAW[4] (4th pixel)
D[11](2nd)	V-by-One®HS_D[11]	RAW[3] (2nd pixel)	0	RAW[3] (4th pixel)
D[10](2nd)	V-by-One®HS_D[10]	RAW[2] (2nd pixel)	0	RAW[2] (4th pixel)
D[9](2nd)	V-by-One®HS_D[9]	RAW[1] (2nd pixel)	0	RAW[1] (4th pixel)
D[8](2nd)	V-by-One®HS_D[8]	RAW[0] (2nd pixel)	0	RAW[0] (4th pixel)
D[7](2nd)	V-by-One®HS_D[7]	RAW[7] (1st pixel)	RAW[7] (2nd pixel)	RAW[7] (3rd pixel)
D[6](2nd)	V-by-One®HS_D[6]	RAW[6] (1st pixel)	RAW[6] (2nd pixel)	RAW[6] (3rd pixel)
D[5](2nd)	V-by-One®HS_D[5]	RAW[5] (1st pixel)	RAW[5] (2nd pixel)	RAW[5] (3rd pixel)
D[4](2nd)	V-by-One®HS_D[4]	RAW[4] (1st pixel)	RAW[4] (2nd pixel)	RAW[4] (3rd pixel)
D[3](2nd)	V-by-One®HS_D[3]	RAW[3] (1st pixel)	RAW[3] (2nd pixel)	RAW[3] (3rd pixel)
D[2](2nd)	V-by-One®HS_D[2]	RAW[2] (1st pixel)	RAW[2] (2nd pixel)	RAW[2] (3rd pixel)
D[1](2nd)	V-by-One®HS_D[1]	RAW[1] (1st pixel)	RAW[1] (2nd pixel)	RAW[1] (3rd pixel)
D[0](2nd)	V-by-One®HS_D[0]	RAW[0] (1st pixel)	RAW[0] (2nd pixel)	RAW[0] (3rd pixel)

THCV231/235 Pins	Format Name	RAW10		
HFSEL=1	Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
D[15](1st)	V-by-One®HS_D[31]	0	0	0
D[14](1st)	V-by-One®HS_D[30]	0	0	0
D[13](1st)	V-by-One®HS_D[29]	0	0	0
D[12](1st)	V-by-One®HS_D[28]	0	0	0
D[11](1st)	V-by-One®HS_D[27]	0	0	0
D[10](1st)	V-by-One®HS_D[26]	0	0	0
D[9](1st)	V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
D[8](1st)	V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
D[7](1st)	V-by-One®HS_D[23]	0	RAW[9](1st pixel)	0
D[6](1st)	V-by-One®HS_D[22]	0	RAW[8](1st pixel)	0
D[5](1st)	V-by-One®HS_D[21]	0	RAW[7](1st pixel)	RAW[1](1st pixel)
D[4](1st)	V-by-One®HS_D[20]	0	RAW[6](1st pixel)	RAW[0](1st pixel)
D[3](1st)	V-by-One®HS_D[19]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
D[2](1st)	V-by-One®HS_D[18]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
D[1](1st)	V-by-One®HS_D[17]	0	RAW[3](1st pixel)	RAW[7](1st pixel)
D[0](1st)	V-by-One®HS_D[16]	0	RAW[2](1st pixel)	RAW[6](1st pixel)
D[15](2nd)	V-by-One®HS_D[15]	0	0	RAW[5](1st pixel)
D[14](2nd)	V-by-One®HS_D[14]	0	0	RAW[4](1st pixel)
D[13](2nd)	V-by-One®HS_D[13]	0	0	RAW[3](1st pixel)
D[12](2nd)	V-by-One®HS_D[12]	0	0	RAW[2](1st pixel)
D[11](2nd)	V-by-One®HS_D[11]	0	0	0
D[10](2nd)	V-by-One®HS_D[10]	0	0	0
D[9](2nd)	V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
D[8](2nd)	V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
D[7](2nd)	V-by-One®HS_D[7]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
D[6](2nd)	V-by-One®HS_D[6]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
D[5](2nd)	V-by-One®HS_D[5]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
D[4](2nd)	V-by-One®HS_D[4]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
D[3](2nd)	V-by-One®HS_D[3]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
D[2](2nd)	V-by-One®HS_D[2]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)
D[1](2nd)	V-by-One®HS_D[1]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
D[0](2nd)	V-by-One®HS_D[0]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)

THCV231/235 Pins	Format Name	RAW12		
HFSEL=1	Vx1HS std. Packer Packet ref.	Normal	Demux Mode1	Demux Mode2
D[15](1st)	V-by-One®HS_D[31]	0	0	0
D[14](1st)	V-by-One®HS_D[30]	0	0	0
D[13](1st)	V-by-One®HS_D[29]	0	0	0
D[12](1st)	V-by-One®HS_D[28]	0	0	0
D[11](1st)	V-by-One®HS_D[27]	0	RAW[3](1st pixel)	0
D[10](1st)	V-by-One®HS_D[26]	0	RAW[2](1st pixel)	0
D[9](1st)	V-by-One®HS_D[25]	0	RAW[1](1st pixel)	0
D[8](1st)	V-by-One®HS_D[24]	0	RAW[0](1st pixel)	0
D[7](1st)	V-by-One®HS_D[23]	0	RAW[11](1st pixel)	RAW[3](1st pixel)
D[6](1st)	V-by-One®HS_D[22]	0	RAW[10](1st pixel)	RAW[2](1st pixel)
D[5](1st)	V-by-One®HS_D[21]	0	RAW[9](1st pixel)	RAW[1](1st pixel)
D[4](1st)	V-by-One®HS_D[20]	0	RAW[8](1st pixel)	RAW[0](1st pixel)
D[3](1st)	V-by-One®HS_D[19]	0	RAW[7](1st pixel)	RAW[11](1st pixel)
D[2](1st)	V-by-One®HS_D[18]	0	RAW[6](1st pixel)	RAW[10](1st pixel)
D[1](1st)	V-by-One®HS_D[17]	0	RAW[5](1st pixel)	RAW[9](1st pixel)
D[0](1st)	V-by-One®HS_D[16]	0	RAW[4](1st pixel)	RAW[8](1st pixel)
D[15](2nd)	V-by-One®HS_D[15]	0	0	RAW[7](1st pixel)
D[14](2nd)	V-by-One®HS_D[14]	0	0	RAW[6](1st pixel)
D[13](2nd)	V-by-One®HS_D[13]	0	0	RAW[5](1st pixel)
D[12](2nd)	V-by-One®HS_D[12]	0	0	RAW[4](1st pixel)
D[11](2nd)	V-by-One®HS_D[11]	RAW[3]	RAW[3](2nd pixel)	RAW[3](2nd pixel)
D[10](2nd)	V-by-One®HS_D[10]	RAW[2]	RAW[2](2nd pixel)	RAW[2](2nd pixel)
D[9](2nd)	V-by-One®HS_D[9]	RAW[1]	RAW[1](2nd pixel)	RAW[1](2nd pixel)
D[8](2nd)	V-by-One®HS_D[8]	RAW[0]	RAW[0](2nd pixel)	RAW[0](2nd pixel)
D[7](2nd)	V-by-One®HS_D[7]	RAW[11]	RAW[11](2nd pixel)	RAW[11](2nd pixel)
D[6](2nd)	V-by-One®HS_D[6]	RAW[10]	RAW[10](2nd pixel)	RAW[10](2nd pixel)
D[5](2nd)	V-by-One®HS_D[5]	RAW[9]	RAW[9](2nd pixel)	RAW[9](2nd pixel)
D[4](2nd)	V-by-One®HS_D[4]	RAW[8]	RAW[8](2nd pixel)	RAW[8](2nd pixel)
D[3](2nd)	V-by-One®HS_D[3]	RAW[7]	RAW[7](2nd pixel)	RAW[7](2nd pixel)
D[2](2nd)	V-by-One®HS_D[2]	RAW[6]	RAW[6](2nd pixel)	RAW[6](2nd pixel)
D[1](2nd)	V-by-One®HS_D[1]	RAW[5]	RAW[5](2nd pixel)	RAW[5](2nd pixel)
D[0](2nd)	V-by-One®HS_D[0]	RAW[4]	RAW[4](2nd pixel)	RAW[4](2nd pixel)

Reference code

THCV241A remote initialization from THCV242 by Set&Trig. mode1 code sample1:594Mbps x4Lane

THCV242 2-wire slave 7bit address is 0b0001011 (0x0B) below, being with write command, 0x16 as 8bit.

THCV242 to THCV241A connection is assumed. 68, 00, FE are all hexadecimal value.

Main-Link input:2.97Gbps 1Lane, MIPI output 594Mbps 4Lane, 2Mpixel YUV422 data, MPRF format

Table 4 THCV241A-242 Initialization code sample1 with Set&Trig. mode1:594x4Lane

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	16	00	04	01	Stop	// Sub-Link Initialization
2	Start	16	00	10	10	Stop	// Sub-Link Initialization
3	Start	16	17	04	01	Stop	// Sub-Link Initialization
4	Start	16	01	02	02	Stop	// Sub-Link Initialization
5	Start	16	01	03	02	Stop	// Sub-Link Initialization
6	Start	16	01	04	00	Stop	// Sub-Link Initialization
7	Start	16	01	05	00	Stop	// Sub-Link Initialization
8	Start	16	01	00	03	Stop	// Sub-Link Initialization
9	Start	16	01	0F	25	Stop	// Sub-Link Initialization
10	Start	16	01	0A	15	Stop	// Sub-Link Initialization
11	Start	16	00	E4	01	Stop	// Sub-Link Initialization
12	Start	16	00	D0	00	Stop	// THCV241A Sub-Link Initialization
13	Start	16	00	D1	FE	Stop	// THCV241A bank setting
14	Start	16	00	D2	11	Stop	//
15	Start	16	00	E0	16	Stop	// Sub-Link access target
16	Start	16	00	E1	10	Stop	// Sub-Link 2Byte Addr. Access
17	Start	16	00	E5	01	Stop	//
18	Start	16	00	D0	F3	Stop	// THCV241A Sub-Link Initialization
19	Start	16	00	D1	00	Stop	//
20	Start	16	00	E1	00	Stop	// Sub-Link 1Byte Addr. Access
21	Start	16	00	E5	01	Stop	//
22	Start	16	00	D0	F2	Stop	// THCV241A Sub-Link Initialization
23	Start	16	00	D1	22	Stop	//
24	Start	16	00	E5	01	Stop	//
25	Start	16	00	D0	F0	Stop	// THCV241A Sub-Link Initialization
26	Start	16	00	D1	03	Stop	//
27	Start	16	00	E5	01	Stop	//
28	Start	16	00	D0	FF	Stop	// THCV241A Sub-Link Initialization
29	Start	16	00	D1	19	Stop	//
30	Start	16	00	E5	01	Stop	//
31	Start	16	00	D0	F6	Stop	// THCV241A Sub-Link Initialization
32	Start	16	00	D1	15	Stop	//
33	Start	16	00	E5	01	Stop	//
34	Start	16	00	D0	FE	Stop	// THCV241A bank setting
35	Start	16	00	D1	21	Stop	//
36	Start	16	00	E5	01	Stop	//
37	Start	16	00	D0	0F	Stop	// THCV241A PLL setting
38	Start	16	00	D1	01	Stop	//
39	Start	16	00	E5	01	Stop	//
40	Start	16	00	D0	11	Stop	// THCV241A PLL setting
41	Start	16	00	D1	31	Stop	//
42	Start	16	00	E5	01	Stop	//
43	Start	16	00	D0	12	Stop	// THCV241A PLL setting
44	Start	16	00	D1	80	Stop	//
45	Start	16	00	E5	01	Stop	//

Step		SlvAddr	SubAddr	SubAddr	Data		comment
46	Start	16	00	D0	13	Stop	// THCV241A PLL setting
47	Start	16	00	D1	00	Stop	//
48	Start	16	00	E5	01	Stop	//
49	Start	16	00	D0	14	Stop	// THCV241A PLL setting
50	Start	16	00	D1	00	Stop	//
51	Start	16	00	E5	01	Stop	//
52	Start	16	00	D0	15	Stop	// THCV241A PLL setting
53	Start	16	00	D1	44	Stop	//
54	Start	16	00	E5	01	Stop	//
55	Start	16	00	D0	16	Stop	// THCV241A PLL setting
56	Start	16	00	D1	01	Stop	//
57	Start	16	00	E5	01	Stop	//
58	Start	16	00	D0	00	Stop	// THCV241A Main-Link setting
59	Start	16	00	D1	00	Stop	//
60	Start	16	00	E5	01	Stop	//
61	Start	16	00	D0	01	Stop	// THCV241A Main-Link setting
62	Start	16	00	D1	00	Stop	//
63	Start	16	00	E5	01	Stop	//
64	Start	16	00	D0	02	Stop	// THCV241A Main-Link setting
65	Start	16	00	D1	00	Stop	//
66	Start	16	00	E5	01	Stop	//
67	Start	16	00	D0	55	Stop	// THCV241A Main-Link setting
68	Start	16	00	D1	00	Stop	//
69	Start	16	00	E5	01	Stop	//
70	Start	16	00	D0	04	Stop	// THCV241A SYNC setting
71	Start	16	00	D1	00	Stop	//
72	Start	16	00	E5	01	Stop	//
73	Start	16	00	D0	2B	Stop	// THCV241A MIPI setting
74	Start	16	00	D1	06	Stop	//
75	Start	16	00	E5	01	Stop	//
76	Start	16	00	D0	27	Stop	// THCV241A MIPI setting
77	Start	16	00	D1	00	Stop	//
78	Start	16	00	E5	01	Stop	//
79	Start	16	00	D0	07	Stop	// THCV241A SYNC setting
80	Start	16	00	D1	00	Stop	//
81	Start	16	00	E5	01	Stop	//
82	Start	16	00	D0	08	Stop	// THCV241A SYNC setting
83	Start	16	00	D1	00	Stop	//
84	Start	16	00	E5	01	Stop	//
85	Start	16	00	D0	09	Stop	// THCV241A SYNC setting
86	Start	16	00	D1	00	Stop	//
87	Start	16	00	E5	01	Stop	//
88	Start	16	00	D0	0C	Stop	// THCV241A SYNC setting
89	Start	16	00	D1	00	Stop	//
90	Start	16	00	E5	01	Stop	//
91	Start	16	00	D0	0D	Stop	// THCV241A SYNC setting
92	Start	16	00	D1	00	Stop	//
93	Start	16	00	E5	01	Stop	//
94	Start	16	00	D0	2D	Stop	// THCV241A MIPI setting
95	Start	16	00	D1	13	Stop	//
96	Start	16	00	E5	01	Stop	//
97	Start	16	00	D0	2C	Stop	// THCV241A MIPI setting
98	Start	16	00	D1	01	Stop	//
99	Start	16	00	E5	01	Stop	//

Step		SlvAddr	SubAddr	SubAddr	Data		comment
100	Start	16	00	D0	05	Stop	// THCV241A PLL reset
101	Start	16	00	D1	01	Stop	//
102	Start	16	00	E5	01	Stop	//
103	Start	16	00	D0	06	Stop	// THCV241A Main-Link reset
104	Start	16	00	D1	01	Stop	//
105	Start	16	00	E5	01	Stop	//
106	Start	16	00	10	11	Stop	// Sub-Link Initialization end
107	Start	16	10	10	A1	Stop	// Main-Link setting
108	Start	16	10	11	05	Stop	// Main-Link setting
109	Start	16	10	12	00	Stop	// Main-Link setting
110	Start	16	10	21	20	Stop	// PLL setting
111	Start	16	10	22	02	Stop	// PLL setting
112	Start	16	10	23	21	Stop	// PLL setting
113	Start	16	10	24	00	Stop	// PLL setting
114	Start	16	10	25	00	Stop	// PLL setting
115	Start	16	10	26	00	Stop	// PLL setting
116	Start	16	10	27	07	Stop	// Reserved procedure
117	Start	16	10	28	00	Stop	// MIPI setting
118	Start	16	11	00	01	Stop	// Main-Link / MIPI setting
119	Start	16	11	01	01	Stop	// Main-Link / MIPI setting
120	Start	16	11	02	01	Stop	// Main-Link / MIPI setting
121	Start	16	11	03	00	Stop	// Main-Link / MIPI setting
122	Start	16	11	04	00	Stop	// Main-Link / MIPI setting
123	Start	16	16	09	02	Stop	// MIPI setting
124	Start	16	16	0A	1D	Stop	// MIPI setting
125	Start	16	16	0B	07	Stop	// MIPI setting
126	Start	16	16	0C	02	Stop	// MIPI setting
127	Start	16	16	0D	0C	Stop	// MIPI setting
128	Start	16	16	0E	0B	Stop	// MIPI setting
129	Start	16	16	0F	05	Stop	// MIPI setting
130	Start	16	16	10	02	Stop	// MIPI setting
131	Start	16	16	11	10	Stop	// MIPI setting
132	Start	16	16	12	07	Stop	// MIPI setting
133	Start	16	16	13	40	Stop	// MIPI setting
134	Start	16	16	05	2B	Stop	// MIPI setting
135	Start	16	16	06	44	Stop	// MIPI setting
136	Start	16	16	00	1A	Stop	// MIPI reset
137	Start	16	17	03	01	Stop	// PLL reset
138	Start	16	17	04	11	Stop	// Main-Link reset

THCV241A remote initialization from THCV242 by Set&Trig. mode1 code sample2:891Mbps x2Lane

THCV242 2-wire slave 7bit address is 0b0001011 (0x0B) below, being with write command, 0x16 as 8bit.

THCV242 to THCV241A connection is assumed. 68, 00, FE are all hexadecimal value.

Main-Link input:2.2275Gbps 1Lane, MIPI output 891Mbps 2Lane, 2Mpixel RAW12 data, MPRF format

Table 5 THCV241A-242 Initialization code sample2 with Set&Trig. mode1:891x2Lane

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	16	00	04	01	Stop	// Sub-Link Initialization
2	Start	16	00	10	10	Stop	// Sub-Link Initialization
3	Start	16	17	04	01	Stop	// Sub-Link Initialization
4	Start	16	01	02	02	Stop	// Sub-Link Initialization
5	Start	16	01	03	02	Stop	// Sub-Link Initialization
6	Start	16	01	04	00	Stop	// Sub-Link Initialization
7	Start	16	01	05	00	Stop	// Sub-Link Initialization
8	Start	16	01	00	03	Stop	// Sub-Link Initialization
9	Start	16	01	0F	25	Stop	// Sub-Link Initialization
10	Start	16	01	0A	15	Stop	// Sub-Link Initialization
11	Start	16	00	E4	01	Stop	// Sub-Link Initialization
12	Start	16	00	D0	00	Stop	// THCV241A Sub-Link Initialization
13	Start	16	00	D1	FE	Stop	// THCV241A bank setting
14	Start	16	00	D2	11	Stop	//
15	Start	16	00	E0	16	Stop	// Sub-Link access target
16	Start	16	00	E1	10	Stop	// Sub-Link 2Byte Addr. Access
17	Start	16	00	E5	01	Stop	//
18	Start	16	00	D0	F3	Stop	// THCV241A Sub-Link Initialization
19	Start	16	00	D1	00	Stop	//
20	Start	16	00	E1	00	Stop	// Sub-Link 1Byte Addr. Access
21	Start	16	00	E5	01	Stop	//
22	Start	16	00	D0	F2	Stop	// THCV241A Sub-Link Initialization
23	Start	16	00	D1	22	Stop	//
24	Start	16	00	E5	01	Stop	//
25	Start	16	00	D0	F0	Stop	// THCV241A Sub-Link Initialization
26	Start	16	00	D1	03	Stop	//
27	Start	16	00	E5	01	Stop	//
28	Start	16	00	D0	FF	Stop	// THCV241A Sub-Link Initialization
29	Start	16	00	D1	19	Stop	//
30	Start	16	00	E5	01	Stop	//
31	Start	16	00	D0	F6	Stop	// THCV241A Sub-Link Initialization
32	Start	16	00	D1	15	Stop	//
33	Start	16	00	E5	01	Stop	//
34	Start	16	00	D0	FE	Stop	// THCV241A bank setting
35	Start	16	00	D1	21	Stop	//
36	Start	16	00	E5	01	Stop	//
37	Start	16	00	D0	0F	Stop	// THCV241A PLL setting
38	Start	16	00	D1	01	Stop	//
39	Start	16	00	E5	01	Stop	//
40	Start	16	00	D0	11	Stop	// THCV241A PLL setting
41	Start	16	00	D1	25	Stop	//
42	Start	16	00	E5	01	Stop	//
43	Start	16	00	D0	12	Stop	// THCV241A PLL setting
44	Start	16	00	D1	20	Stop	//
45	Start	16	00	E5	01	Stop	//

Step		SlvAddr	SubAddr	SubAddr	Data		comment
46	Start	16	00	D0	13	Stop	// THCV241A PLL setting
47	Start	16	00	D1	00	Stop	//
48	Start	16	00	E5	01	Stop	//
49	Start	16	00	D0	14	Stop	// THCV241A PLL setting
50	Start	16	00	D1	00	Stop	//
51	Start	16	00	E5	01	Stop	//
52	Start	16	00	D0	15	Stop	// THCV241A PLL setting
53	Start	16	00	D1	44	Stop	//
54	Start	16	00	E5	01	Stop	//
55	Start	16	00	D0	16	Stop	// THCV241A PLL setting
56	Start	16	00	D1	01	Stop	//
57	Start	16	00	E5	01	Stop	//
58	Start	16	00	D0	00	Stop	// THCV241A Main-Link setting
59	Start	16	00	D1	00	Stop	//
60	Start	16	00	E5	01	Stop	//
61	Start	16	00	D0	01	Stop	// THCV241A Main-Link setting
62	Start	16	00	D1	00	Stop	//
63	Start	16	00	E5	01	Stop	//
64	Start	16	00	D0	02	Stop	// THCV241A Main-Link setting
65	Start	16	00	D1	00	Stop	//
66	Start	16	00	E5	01	Stop	//
67	Start	16	00	D0	55	Stop	// THCV241A Main-Link setting
68	Start	16	00	D1	00	Stop	//
69	Start	16	00	E5	01	Stop	//
70	Start	16	00	D0	04	Stop	// THCV241A SYNC setting
71	Start	16	00	D1	00	Stop	//
72	Start	16	00	E5	01	Stop	//
73	Start	16	00	D0	2B	Stop	// THCV241A MIPI setting
74	Start	16	00	D1	05	Stop	//
75	Start	16	00	E5	01	Stop	//
76	Start	16	00	D0	27	Stop	// THCV241A MIPI setting
77	Start	16	00	D1	00	Stop	//
78	Start	16	00	E5	01	Stop	//
79	Start	16	00	D0	07	Stop	// THCV241A SYNC setting
80	Start	16	00	D1	00	Stop	//
81	Start	16	00	E5	01	Stop	//
82	Start	16	00	D0	08	Stop	// THCV241A SYNC setting
83	Start	16	00	D1	00	Stop	//
84	Start	16	00	E5	01	Stop	//
85	Start	16	00	D0	09	Stop	// THCV241A SYNC setting
86	Start	16	00	D1	00	Stop	//
87	Start	16	00	E5	01	Stop	//
88	Start	16	00	D0	0C	Stop	// THCV241A SYNC setting
89	Start	16	00	D1	00	Stop	//
90	Start	16	00	E5	01	Stop	//
91	Start	16	00	D0	0D	Stop	// THCV241A SYNC setting
92	Start	16	00	D1	00	Stop	//
93	Start	16	00	E5	01	Stop	//
94	Start	16	00	D0	2D	Stop	// THCV241A MIPI setting
95	Start	16	00	D1	11	Stop	//
96	Start	16	00	E5	01	Stop	//
97	Start	16	00	D0	2C	Stop	// THCV241A MIPI setting
98	Start	16	00	D1	01	Stop	//
99	Start	16	00	E5	01	Stop	//

Step		SlvAddr	SubAddr	SubAddr	Data		comment
100	Start	16	00	D0	05	Stop	// THCV241A PLL reset
101	Start	16	00	D1	01	Stop	//
102	Start	16	00	E5	01	Stop	//
103	Start	16	00	D0	06	Stop	// THCV241A Main-Link reset
104	Start	16	00	D1	01	Stop	//
105	Start	16	00	E5	01	Stop	//
106	Start	16	00	10	11	Stop	// Sub-Link Initialization end
107	Start	16	10	10	A1	Stop	// Main-Link setting
108	Start	16	10	11	05	Stop	// Main-Link setting
109	Start	16	10	12	00	Stop	// Main-Link setting
110	Start	16	10	21	20	Stop	// PLL setting
111	Start	16	10	22	02	Stop	// PLL setting
112	Start	16	10	23	11	Stop	// PLL setting
113	Start	16	10	24	00	Stop	// PLL setting
114	Start	16	10	25	00	Stop	// PLL setting
115	Start	16	10	26	00	Stop	// PLL setting
116	Start	16	10	27	07	Stop	// Reserved procedure
117	Start	16	10	28	02	Stop	// MIPI setting
118	Start	16	11	00	01	Stop	// Main-Link / MIPI setting
119	Start	16	11	01	01	Stop	// Main-Link / MIPI setting
120	Start	16	11	02	01	Stop	// Main-Link / MIPI setting
121	Start	16	11	03	00	Stop	// Main-Link / MIPI setting
122	Start	16	11	04	00	Stop	// Main-Link / MIPI setting
123	Start	16	16	09	03	Stop	// MIPI setting
124	Start	16	16	0A	1D	Stop	// MIPI setting
125	Start	16	16	0B	07	Stop	// MIPI setting
126	Start	16	16	0C	02	Stop	// MIPI setting
127	Start	16	16	0D	0C	Stop	// MIPI setting
128	Start	16	16	0E	0B	Stop	// MIPI setting
129	Start	16	16	0F	05	Stop	// MIPI setting
130	Start	16	16	10	03	Stop	// MIPI setting
131	Start	16	16	11	10	Stop	// MIPI setting
132	Start	16	16	12	07	Stop	// MIPI setting
133	Start	16	16	13	40	Stop	// MIPI setting
134	Start	16	16	05	29	Stop	// MIPI setting
135	Start	16	16	06	44	Stop	// MIPI setting
136	Start	16	16	00	1A	Stop	// MIPI reset
137	Start	16	17	03	01	Stop	// PLL reset
138	Start	16	17	04	11	Stop	// Main-Link reset

THCV241A remote initialization from THCV242 by Pass Through mode1 code sample1:594Mbps x4Lane

THCV242 2-wire slave 7bit address is 0b0001011 (0x0B) below, being with write command, 0x16 as 8bit.

THCV242 to THCV241A connection is assumed. 68, 00, FE are all hexadecimal value.

Main-Link input:2.97Gbps 1Lane, MIPI output 594Mbps 4Lane, 2Mpixel YUV422 data, MPRF format

Table 6 THCV241A-242 Initialization code sample1 with Pass Through mode1:594x4Lane

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	16	00	50	51	Stop	// Sub-Link Initialization
2	Start	16	00	04	03	Stop	// Sub-Link Initialization
3	Start	16	00	10	10	Stop	// Sub-Link Initialization
4	Start	16	17	04	01	Stop	// Sub-Link Initialization
5	Start	16	01	02	02	Stop	// Sub-Link Initialization
6	Start	16	01	03	02	Stop	// Sub-Link Initialization
7	Start	16	01	04	00	Stop	// Sub-Link Initialization
8	Start	16	01	05	00	Stop	// Sub-Link Initialization
9	Start	16	01	00	03	Stop	// Sub-Link Initialization
10	Start	16	01	0F	25	Stop	// Sub-Link Initialization
11	Start	16	01	0A	15	Stop	// Sub-Link Initialization
12	Start	16	00	31	02	Stop	// Sub-Link Initialization
13	Start	16	00	32	10	Stop	// Sub-Link Initialization
14	Start	A2	00	FE	11	Stop	// THCV241A Sub-Link Initialization
15	Start	16	00	32	00	Stop	// Sub-Link Initialization
16	Start	A2	F3		00	Stop	// THCV241A Sub-Link Initialization
17	Start	A2	F2		22	Stop	// THCV241A Sub-Link Initialization
18	Start	A2	F0		03	Stop	// THCV241A Sub-Link Initialization
19	Start	A2	FF		19	Stop	// THCV241A Sub-Link Initialization
20	Start	A2	F6		15	Stop	// THCV241A Sub-Link Initialization
21	Start	A2	FE		21	Stop	// THCV241A bank setting
22	Start	A2	0F		01	Stop	// THCV241A PLL setting
23	Start	A2	11		31	Stop	// THCV241A PLL setting
24	Start	A2	12		80	Stop	// THCV241A PLL setting
25	Start	A2	13		00	Stop	// THCV241A PLL setting
26	Start	A2	14		00	Stop	// THCV241A PLL setting
27	Start	A2	15		44	Stop	// THCV241A PLL setting
28	Start	A2	16		01	Stop	// THCV241A PLL setting
29	Start	A2	00		00	Stop	// THCV241A Main-Link setting
30	Start	A2	01		00	Stop	// THCV241A Main-Link setting
31	Start	A2	02		00	Stop	// THCV241A Main-Link setting
32	Start	A2	55		00	Stop	// THCV241A Main-Link setting
33	Start	A2	04		00	Stop	// THCV241A SYNC setting
34	Start	A2	2B		06	Stop	// THCV241A MIPI setting
35	Start	A2	27		00	Stop	// THCV241A MIPI setting
36	Start	A2	07		00	Stop	// THCV241A SYNC setting
37	Start	A2	08		00	Stop	// THCV241A SYNC setting
38	Start	A2	09		00	Stop	// THCV241A SYNC setting
39	Start	A2	0C		00	Stop	// THCV241A SYNC setting
40	Start	A2	0D		00	Stop	// THCV241A SYNC setting
41	Start	A2	2D		13	Stop	// THCV241A MIPI setting
42	Start	A2	2C		01	Stop	// THCV241A MIPI setting
43	Start	A2	05		01	Stop	// THCV241A PLL reset
44	Start	A2	06		01	Stop	// THCV241A Main-Link reset
45	Start	16	00	10	11	Stop	// Sub-Link Initialization end

Step		SlvAddr	SubAddr	SubAddr	Data		comment
46	Start	16	10	10	A1	Stop	// Main-Link setting
47	Start	16	10	11	05	Stop	// Main-Link setting
48	Start	16	10	12	00	Stop	// Main-Link setting
49	Start	16	10	21	20	Stop	// PLL setting
50	Start	16	10	22	02	Stop	// PLL setting
51	Start	16	10	23	21	Stop	// PLL setting
52	Start	16	10	24	00	Stop	// PLL setting
53	Start	16	10	25	00	Stop	// PLL setting
54	Start	16	10	26	00	Stop	// PLL setting
55	Start	16	10	27	07	Stop	// Reserved procedure
56	Start	16	10	28	00	Stop	// MIPI setting
57	Start	16	11	00	01	Stop	// Main-Link / MIPI setting
58	Start	16	11	01	01	Stop	// Main-Link / MIPI setting
59	Start	16	11	02	01	Stop	// Main-Link / MIPI setting
60	Start	16	11	03	00	Stop	// Main-Link / MIPI setting
61	Start	16	11	04	00	Stop	// Main-Link / MIPI setting
62	Start	16	16	09	02	Stop	// MIPI setting
63	Start	16	16	0A	1D	Stop	// MIPI setting
64	Start	16	16	0B	07	Stop	// MIPI setting
65	Start	16	16	0C	02	Stop	// MIPI setting
66	Start	16	16	0D	0C	Stop	// MIPI setting
67	Start	16	16	0E	0B	Stop	// MIPI setting
68	Start	16	16	0F	05	Stop	// MIPI setting
69	Start	16	16	10	02	Stop	// MIPI setting
70	Start	16	16	11	10	Stop	// MIPI setting
71	Start	16	16	12	07	Stop	// MIPI setting
72	Start	16	16	13	40	Stop	// MIPI setting
73	Start	16	16	05	2B	Stop	// MIPI setting
74	Start	16	16	06	44	Stop	// MIPI setting
75	Start	16	16	00	1A	Stop	// MIPI reset
76	Start	16	17	03	01	Stop	// PLL reset
77	Start	16	17	04	11	Stop	// Main-Link reset

THCV241A remote initialization from THCV242 by Pass Through mode1 code sample2:891Mbps x2Lane

THCV242 2-wire slave 7bit address is 0b0001011 (0x0B) below, being with write command, 0x16 as 8bit.

THCV242 to THCV241A connection is assumed. 68, 00, FE are all hexadecimal value.

Main-Link input:2.2275Gbps 1Lane, MIPI output 891Mbps 2Lane, 2Mpixel RAW12 data, MPRF format

Table 7 THCV241A-242 Initialization code sample2 with Pass Through mode1:891x2Lane

Step		SlvAddr	SubAddr	SubAddr	Data		comment
1	Start	16	00	50	51	Stop	// Sub-Link Initialization
2	Start	16	00	04	03	Stop	// Sub-Link Initialization
3	Start	16	00	10	10	Stop	// Sub-Link Initialization
4	Start	16	17	04	01	Stop	// Sub-Link Initialization
5	Start	16	01	02	02	Stop	// Sub-Link Initialization
6	Start	16	01	03	02	Stop	// Sub-Link Initialization
7	Start	16	01	04	00	Stop	// Sub-Link Initialization
8	Start	16	01	05	00	Stop	// Sub-Link Initialization
9	Start	16	01	00	03	Stop	// Sub-Link Initialization
10	Start	16	01	0F	25	Stop	// Sub-Link Initialization
11	Start	16	01	0A	15	Stop	// Sub-Link Initialization
12	Start	16	00	31	02	Stop	// Sub-Link Initialization
13	Start	16	00	32	10	Stop	// Sub-Link Initialization
14	Start	A2	00	FE	11	Stop	// THCV241A Sub-Link Initialization
15	Start	16	00	32	00	Stop	// Sub-Link Initialization
16	Start	A2	F3		00	Stop	// THCV241A Sub-Link Initialization
17	Start	A2	F2		22	Stop	// THCV241A Sub-Link Initialization
18	Start	A2	F0		03	Stop	// THCV241A Sub-Link Initialization
19	Start	A2	FF		19	Stop	// THCV241A Sub-Link Initialization
20	Start	A2	F6		15	Stop	// THCV241A Sub-Link Initialization
21	Start	A2	FE		21	Stop	// THCV241A bank setting
22	Start	A2	0F		01	Stop	// THCV241A PLL setting
23	Start	A2	11		25	Stop	// THCV241A PLL setting
24	Start	A2	12		20	Stop	// THCV241A PLL setting
25	Start	A2	13		00	Stop	// THCV241A PLL setting
26	Start	A2	14		00	Stop	// THCV241A PLL setting
27	Start	A2	15		44	Stop	// THCV241A PLL setting
28	Start	A2	16		01	Stop	// THCV241A PLL setting
29	Start	A2	00		00	Stop	// THCV241A Main-Link setting
30	Start	A2	01		00	Stop	// THCV241A Main-Link setting
31	Start	A2	02		00	Stop	// THCV241A Main-Link setting
32	Start	A2	55		00	Stop	// THCV241A Main-Link setting
33	Start	A2	04		00	Stop	// THCV241A SYNC setting
34	Start	A2	2B		05	Stop	// THCV241A MIPI setting
35	Start	A2	27		00	Stop	// THCV241A MIPI setting
36	Start	A2	07		00	Stop	// THCV241A SYNC setting
37	Start	A2	08		00	Stop	// THCV241A SYNC setting
38	Start	A2	09		00	Stop	// THCV241A SYNC setting
39	Start	A2	0C		00	Stop	// THCV241A SYNC setting
40	Start	A2	0D		00	Stop	// THCV241A SYNC setting
41	Start	A2	2D		11	Stop	// THCV241A MIPI setting
42	Start	A2	2C		01	Stop	// THCV241A MIPI setting
43	Start	A2	05		01	Stop	// THCV241A PLL reset
44	Start	A2	06		01	Stop	// THCV241A Main-Link reset
45	Start	16	00	10	11	Stop	// Sub-Link Initialization end

Step		SlvAddr	SubAddr	SubAddr	Data		comment
46	Start	16	10	10	A1	Stop	// Main-Link setting
47	Start	16	10	11	05	Stop	// Main-Link setting
48	Start	16	10	12	00	Stop	// Main-Link setting
49	Start	16	10	21	20	Stop	// PLL setting
50	Start	16	10	22	02	Stop	// PLL setting
51	Start	16	10	23	11	Stop	// PLL setting
52	Start	16	10	24	00	Stop	// PLL setting
53	Start	16	10	25	00	Stop	// PLL setting
54	Start	16	10	26	00	Stop	// PLL setting
55	Start	16	10	27	07	Stop	// Reserved procedure
56	Start	16	10	28	02	Stop	// MIPI setting
57	Start	16	11	00	01	Stop	// Main-Link / MIPI setting
58	Start	16	11	01	01	Stop	// Main-Link / MIPI setting
59	Start	16	11	02	01	Stop	// Main-Link / MIPI setting
60	Start	16	11	03	00	Stop	// Main-Link / MIPI setting
61	Start	16	11	04	00	Stop	// Main-Link / MIPI setting
62	Start	16	16	09	03	Stop	// MIPI setting
63	Start	16	16	0A	1D	Stop	// MIPI setting
64	Start	16	16	0B	07	Stop	// MIPI setting
65	Start	16	16	0C	02	Stop	// MIPI setting
66	Start	16	16	0D	0C	Stop	// MIPI setting
67	Start	16	16	0E	0B	Stop	// MIPI setting
68	Start	16	16	0F	05	Stop	// MIPI setting
69	Start	16	16	10	03	Stop	// MIPI setting
70	Start	16	16	11	10	Stop	// MIPI setting
71	Start	16	16	12	07	Stop	// MIPI setting
72	Start	16	16	13	40	Stop	// MIPI setting
73	Start	16	16	05	29	Stop	// MIPI setting
74	Start	16	16	06	44	Stop	// MIPI setting
75	Start	16	16	00	1A	Stop	// MIPI reset
76	Start	16	17	03	01	Stop	// PLL reset
77	Start	16	17	04	11	Stop	// Main-Link reset

Sub-Link establishment code from THCV242(Master) to THCV241A(Slave) with Set & Trig. mode1

Sub-Link Tx-Rx PHY settings (e.g. THCV241A Address 0x0072,73 / 0x00F2,F3) are supposed to be optimized before any Sub-Link transaction especially when THCV241A was used under noisy environment. Sub-Link Tx PHY setting can be severer on Sub-Link Slave side because any setting is done through Sub-Link. Below Sub-Link Slave PHY initialize sample code can be repeated from Sub-Link Master if this particular Sub-Link transaction did not succeed before other settings.

Table 8 THCV241A-242 Sub-Link establishment code sample with Set&Trig. Mode1

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x0004	0x01	Sub-Link Mode setting (Set&Trig. mode1)
2	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
3	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Pow er On
4	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
5	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
6	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
7	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
8	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
9	THCV242 (Master)	0xZZ**	0x010F	0x25	
10	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
11	THCV242 (Master)	0xZZ**	0x00E4	0xWW	Sub-Link transaction w rite lane select (e.g. WW=0x01 for Lane0)
12	THCV242 (Master)	0xZZ**	0x00D0	0x00	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0xFE	
	THCV242 (Master)	0xZZ**	0x00D2	0x11	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x10	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
13	THCV242 (Master)	0xZZ**	0x00D0	0xF3	THCV241A (Slave) setting (0x00F3) Sub-Link Rx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
14	THCV242 (Master)	0xZZ**	0x00D0	0xF2	THCV241A (Slave) setting (0x00F2) Sub-Link Tx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x22	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
15	THCV242 (Master)	0xZZ**	0x00D0	0xF0	THCV241A (Slave) setting (0x00F0/FF) Tuning register access Enable
	THCV242 (Master)	0xZZ**	0x00D1	0x03	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
	THCV242 (Master)	0xZZ**	0x00D0	0xFF	
	THCV242 (Master)	0xZZ**	0x00D1	0x19	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
16	THCV242 (Master)	0xZZ**	0x00D0	0xF6	THCV241A (Slave) setting (0x00F6) Sub-Link frequency tuning
	THCV242 (Master)	0xZZ**	0x00D1	0x15	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
17	THCV242 (Master)	0xZZ**	0x0010	0x11	Sub-Link Enable On/Polling ON

**THCV242 i2c slave address depends on AIN settings.

***[7:1]R_2WIRE_DEVADR=ZZ || [0]R_2WIRE_WR=0:w rite. 0x00E0 w rite action can be eliminated from 2nd time because no change occurred from previous setting.

****0x00E1 w rite action can be eliminated because no change occurred from previous setting.

Sub-Link establishment code from THCV242(Master) to THCV241A(Slave) by Pass Through mode1

Sub-Link Tx-Rx PHY settings (e.g. THCV241A Address 0x0072,73 / 0x00F2,F3) are supposed to be optimized before any Sub-Link transaction especially when THCV241A was used under noisy environment. Sub-Link Tx PHY setting can be severer on Sub-Link Slave side because any setting is done through Sub-Link. Below Sub-Link Slave PHY initialize sample code can be repeated from Sub-Link Master if this particular Sub-Link transaction did not succeed before other settings.

Table 9 THCV241A-242 Sub-Link establishment code sample with Pass Through Mode1

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x0050	0xYY	Sub-Link Slave Access Addr. (e.g. YY=0x51)
2	THCV242 (Master)	0xZZ**	0x0004	0x03	Sub-Link Mode setting (Pass Through mode1)
3	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
4	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
5	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
6	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
7	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
8	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
9	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
10	THCV242 (Master)	0xZZ**	0x010F	0x25	
11	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
12	THCV242 (Master)	0xZZ**	0x0031	0x02	Pass Through mode Divided write & Addr. Rename
13	THCV242 (Master)	0xZZ**	0x0032	0x10	Pass Through Divided write/read Addr.=2Byte, Data=1Byte
14	THCV241A (Slave)	0xYY	0x00FE	0x11	Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
15	THCV242 (Master)	0xZZ**	0x0032	0x00	Pass Through Divided write/read Addr.=1Byte, Data=1Byte
16	THCV241A (Slave)	0xYY	0xF3	0x00	(0x00F3) Sub-Link Rx Termination/Drive current
17	THCV241A (Slave)	0xYY	0xF2	0x22	(0x00F2) Sub-Link Tx Termination/Drive current
18	THCV241A (Slave)	0xYY	0xF0	0x03	(0x00F0/FF) Tuning register access Enable
19	THCV241A (Slave)	0xYY	0xFF	0x19	
20	THCV241A (Slave)	0xYY	0xF6	0x15	(0x00F6) Sub-Link frequency tuning
21	THCV242 (Master)	0xZZ**	0x0010	0x11	Sub-Link Enable On/Polling ON

**THCV242 i2c slave address depends on AIN settings.

Setting reset code from THCV242(Master) to THCV241A(Slave) with Set & Trig. mode1

Setting reset may cover inevitable intended THCV241A-242 behavior change in the middle of PDN=High, Normal operation. (Frequency change, for example.) In terms of time management, reset action must be later than the end of previous THCV241A-242 operating condition (Sensor MIPI output, for example.) and must not be the same time as the beginning of following THCV241A-242 operating condition. THCV241A 0x00FE setting is reset to default in order to re-initialize system with the same code as 1st initialize code in reference.

Table 10 Setting reset code from THCV242(Master) to THCV241A(Slave) with Set & Trig. mode1

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x1600	0x00	MIPI Tx Power Down & software reset
2	THCV242 (Master)	0xZZ**	0x1703	0x00	PLL Power Down
3	THCV242 (Master)	0xZZ**	0x1704	0x00	Main-Link / Sub-Link Power Off
4	THCV242 (Master)	0xZZ**	0x1701	0x1D	Main-Link0, DataStreamHandler, MIPI, BASELogic software reset
5	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
6	THCV242 (Master)	0xZZ**	0x00E4	0xWW	Sub-Link transaction write lane select (e.g. WW=0x01 for Lane0)
7	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)**	Sub-Link slave write
8	THCV242 (Master)	0xZZ**	0x00E1	0x00	1Byte addr./ 1Byte data(match THCV241A 0x00FE privious state)
9	THCV242 (Master)	0xZZ**	0x00D0	0xFE	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0x21	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
10	THCV242 (Master)	0xZZ**	0x00D0	0x06	THCV241A (Slave) setting 0x1006 V-by-One® HS Tx software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
11	THCV242 (Master)	0xZZ**	0x00D0	0x05	THCV241A (Slave) setting 0x1005 PLL software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
12	THCV242 (Master)	0xZZ**	0x00D0	0x21	THCV241A (Slave) setting 0x1021 MIPI CSI-2 software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
13	THCV242 (Master)	0xZZ**	0x00D0	0x22	THCV241A (Slave) setting 0x1022 Digital Logic clock software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
14	THCV242 (Master)	0xZZ**	0x00D0	0x23	THCV241A (Slave) setting 0x1023 MIPI clock software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
15	THCV242 (Master)	0xZZ**	0x00D0	0x2D	THCV241A (Slave) setting 0x102D MIPI Data lane Disable
	THCV242 (Master)	0xZZ**	0x00D1	0x03	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
16	THCV242 (Master)	0xZZ**	0x00D0	0x2C	THCV241A (Slave) setting 0x102C MIPI Clock lane Disable
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
17	THCV242 (Master)	0xZZ**	0x00D0	0x21	THCV241A (Slave) setting 0x1021 MIPI CSI-2 software reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
18	THCV242 (Master)	0xZZ**	0x00D0	0x22	THCV241A (Slave) setting 0x1022 Digital Logic clock software reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
19	THCV242 (Master)	0xZZ**	0x00D0	0x23	THCV241A (Slave) setting 0x1023 MIPI clock software reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
20	THCV242 (Master)	0xZZ**	0x00D0	0xFE	THCV241A (Slave) setting Sub-Link Word Addr. 2Byte Access (default) from Master
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	

**THCV242 i2c slave address depends on AIN settings.

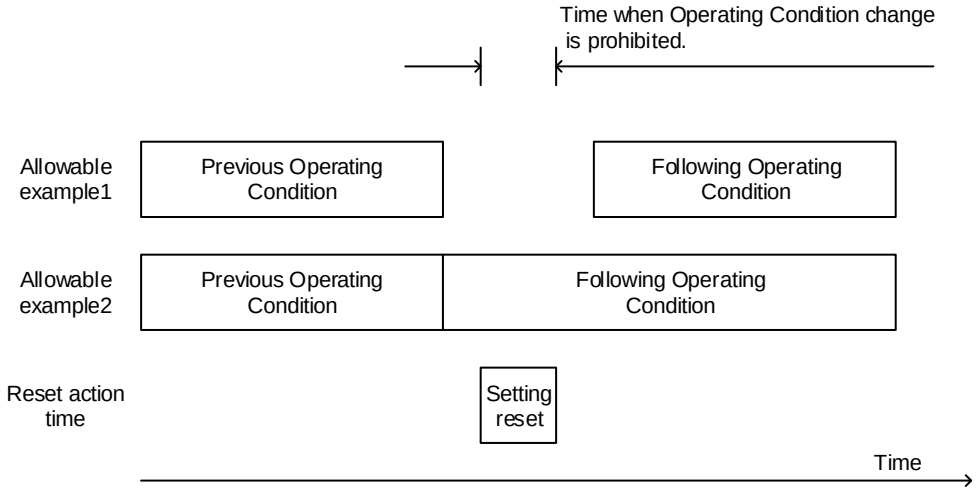


Figure 4 Setting reset time

Setting reset code from THCV242(Master) to THCV241A(Slave) by Pass Through mode1

Setting reset may cover inevitable intended THCV241A-242 behavior change in the middle of PDN=High, Normal operation. (Frequency change, for example.) In terms of time management, reset action must be later than the end of previous THCV241A-242 operating condition (Sensor MIPI output, for example.) and must not be the same time as the beginning of following THCV241A-242 operating condition. THCV241A 0x00FE setting is reset to default in order to re-initialize system with the same code as 1st initialize code in reference.

Table 11 Setting reset code from THCV242(Master) to THCV241A(Slave) by Pass Through mode1

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x1600	0x00	MIPI Tx Power Down & software reset
2	THCV242 (Master)	0xZZ**	0x1703	0x00	PLL Power Down
3	THCV242 (Master)	0xZZ**	0x1704	0x00	Main-Link / Sub-Link Power Off
4	THCV242 (Master)	0xZZ**	0x1701	0x1D	Main-Link0, DataStreamHandler, MIPI, BASELogic software reset
5	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
6	THCV242 (Master)	0xZZ**	0x0031	0x02	Pass Through mode Divided write & Addr. Rename
7	THCV242 (Master)	0xZZ**	0x0032	0x00	1Byte addr./ 1Byte data(match THCV241A 0x00FE privious state)
8	THCV241A (Slave)	0xYY***	0xFE	0x21	Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
9	THCV241A (Slave)	0xYY***	0x06	0x00	0x1006 V-by-One® HS Tx software reset
10	THCV241A (Slave)	0xYY***	0x05	0x00	0x1005 PLL software reset
11	THCV241A (Slave)	0xYY***	0x21	0x00	0x1021 MIPI CSI-2 software reset
12	THCV241A (Slave)	0xYY***	0x22	0x00	0x1022 Digital Logic clock software reset
13	THCV241A (Slave)	0xYY***	0x23	0x00	0x1023 MIPI clock software reset
14	THCV241A (Slave)	0xYY***	0x2D	0x03	0x102D MIPI Data lane Disable
15	THCV241A (Slave)	0xYY***	0x2C	0x00	0x102C MIPI Clock lane Disable
16	THCV241A (Slave)	0xYY***	0x21	0x01	0x1021 MIPI CSI-2 software reset release
17	THCV241A (Slave)	0xYY***	0x22	0x01	0x1022 Digital Logic clock software reset release
18	THCV241A (Slave)	0xYY***	0x23	0x01	0x1023 MIPI clock software reset release
19	THCV241A (Slave)	0xYY***	0xFE	0x00	Sub-Link Word Addr. 2Byte Access (default) from Master

**THCV242 i2c slave address depends on AIN settings.

***Sub-Link Slave Access Addr. (e.g. YY=0x51 match THCV242 0x0050 privious state)

Internal state software reset code from THCV242(Master) to THCV241A(Slave) with Set & Trig. mode1

Internal state software reset may provide recovery from unintended noise effect in the middle of PDNx=High, Normal operation. Sub-Link reset action requires internal wait time for 2-wire control ready so that users must insert wait time in the middle of the code. If software reset is not work enough, hardware reset (PDNx=low) operation is another considerable option for system trouble. In terms of time management, reset action must be later than noise event. THCV241A 0x00FE setting is reset to default in order to re-initialize system with the same code as 1st initialize code in reference.

Table 12 Internal state reset code from THCV242(Master) to THCV241A with Set & Trig. mode1 (1/2)

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x1702	0x01	Register reset
2	THCV242 (Master)	0xZZ**	0x1600	0x00	MIPI Tx Power Down & software reset
3	THCV242 (Master)	0xZZ**	0x1703	0x00	PLL Power Down
4	THCV242 (Master)	0xZZ**	0x1704	0x00	Main-Link / Sub-Link Power Off
5	THCV242 (Master)	0xZZ**	0x1701	0x1D	Main-Link0, DataStreamHandler, MIPI, BASELogic software reset
6	THCV242 (Master)	0xZZ**	0x0001	0x01	Sub-Link software reset
7	wait t11 of THCV242				At least t11 300us must be wait for 2-wire access ready
8	THCV242 (Master)	0xZZ**	0x0004	0x01	Sub-Link Mode setting (Set & Trig. mode1)
9	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
10	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
11	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
12	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
13	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
14	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
15	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
16	THCV242 (Master)	0xZZ**	0x010F	0x25	
17	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
18	THCV242 (Master)	0xZZ**	0x00E4	0xWW	Sub-Link transaction write lane select (e.g. WW=0x01 for Lane0)
19	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)**	Sub-Link slave write
20	THCV242 (Master)	0xZZ**	0x00E1	0x00	1Byte addr./ 1Byte data(match THCV241A 0x00FE privious state)
21	THCV242 (Master)	0xZZ**	0x00D0	0xFE	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0x21	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
22	THCV242 (Master)	0xZZ**	0x00D0	0x06	THCV241A (Slave) setting 0x1006 V-by-One® HS Tx software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
23	THCV242 (Master)	0xZZ**	0x00D0	0x05	THCV241A (Slave) setting 0x1005 PLL software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
24	THCV242 (Master)	0xZZ**	0x00D0	0x21	THCV241A (Slave) setting 0x1021 MIPI CSI-2 software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
25	THCV242 (Master)	0xZZ**	0x00D0	0x22	THCV241A (Slave) setting 0x1022 Digital Logic clock software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
26	THCV242 (Master)	0xZZ**	0x00D0	0x23	THCV241A (Slave) setting 0x1023 MIPI clock software reset
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
27	THCV242 (Master)	0xZZ**	0x00D0	0xFF	THCV241A (Slave) setting 0x10FF Register reset
	THCV242 (Master)	0xZZ**	0x00D1	0xAA	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
28	THCV242 (Master)	0xZZ**	0x00D0	0x00	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0xFE	
	THCV242 (Master)	0xZZ**	0x00D2	0x11	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)	
	THCV242 (Master)	0xZZ**	0x00E1	0x10	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
29	THCV242 (Master)	0xZZ**	0x00D0	0xF3	THCV241A (Slave) setting (0x00F3) Sub-Link Rx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
30	THCV242 (Master)	0xZZ**	0x00D0	0xF2	THCV241A (Slave) setting (0x00F2) Sub-Link Tx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x22	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	

Table 13 Internal state reset code from THCV242(Master) to THCV241A with Set & Trig. mode1 (2/2)

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
31	THCV242 (Master)	0xZZ**	0x00D0	0xF0	THCV241A (Slave) setting (0x00F0/FF) Tuning register access Enable
	THCV242 (Master)	0xZZ**	0x00D1	0x03	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
	THCV242 (Master)	0xZZ**	0x00D0	0xFF	
	THCV242 (Master)	0xZZ**	0x00D1	0x19	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
32	THCV242 (Master)	0xZZ**	0x00D0	0xF6	THCV241A (Slave) setting (0x00F6) Sub-Link frequency tuning
	THCV242 (Master)	0xZZ**	0x00D1	0x15	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
33	THCV242 (Master)	0xZZ**	0x00D0	0xFE	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0x21	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
34	THCV242 (Master)	0xZZ**	0x00D0	0x2D	THCV241A (Slave) setting 0x102D MIPI Data lane Disable
	THCV242 (Master)	0xZZ**	0x00D1	0x03	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
35	THCV242 (Master)	0xZZ**	0x00D0	0x2C	THCV241A (Slave) setting 0x102C MIPI Clock lane Disable
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
36	THCV242 (Master)	0xZZ**	0x00D0	0x21	THCV241A (Slave) setting 0x1021 MIPI CSI-2 softw are reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
37	THCV242 (Master)	0xZZ**	0x00D0	0x22	THCV241A (Slave) setting 0x1022 Digital Logic clock softw are reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
38	THCV242 (Master)	0xZZ**	0x00D0	0x23	THCV241A (Slave) setting 0x1023 MIPI clock softw are reset release
	THCV242 (Master)	0xZZ**	0x00D1	0x01	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
39	THCV242 (Master)	0xZZ**	0x00D0	0xFE	THCV241A (Slave) setting Sub-Link Word Addr. 2Byte Access (default) from Master
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	

**THCV242 i2c slave address depends on AIN settings.

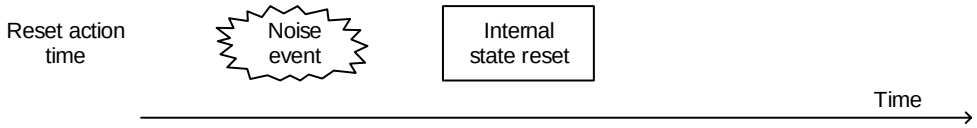


Figure 5 Internal state software reset time

Internal state software reset code from THCV242(Master) to THCV241A(Slave) by Pass Through mode1

Internal state software reset may provide recovery from unintended noise effect in the middle of PDNx=High, Normal operation. Sub-Link reset action requires internal wait time for 2-wire control ready so that users must insert wait time in the middle of the code. If software reset is not work enough, hardware reset (PDNx=low) operation is another considerable option for system trouble. In terms of time management, reset action must be later than noise event. THCV241A 0x00FE setting is reset to default in order to re-initialize system with the same code as 1st initialize code in reference.

Table 14 Internal state reset code from THCV242(Master) to THCV241A with Pass Through mode1

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x1702	0x01	Register reset
2	THCV242 (Master)	0xZZ**	0x1600	0x00	MIPI Tx Power Down & software reset
3	THCV242 (Master)	0xZZ**	0x1703	0x00	PLL Power Down
4	THCV242 (Master)	0xZZ**	0x1704	0x00	Main-Link / Sub-Link Power Off
5	THCV242 (Master)	0xZZ**	0x1701	0x1D	Main-Link0, DataStreamHandler, MIPI, BASELogic software reset
6	THCV242 (Master)	0xZZ**	0x0001	0x01	Sub-Link software reset
7	wait t11 of THCV242				At least t11 300us must be wait for 2-wire access ready
8	THCV242 (Master)	0xZZ**	0x0050	0xYY	Sub-Link Slave Access Addr. (e.g. YY=0x51)
9	THCV242 (Master)	0xZZ**	0x0004	0x03	Sub-Link Mode setting (Pass Through mode1)
10	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
11	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
12	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
13	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
14	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
15	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
16	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
17	THCV242 (Master)	0xZZ**	0x010F	0x25	
18	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
19	THCV242 (Master)	0xZZ**	0x0031	0x02	Pass Through mode Divided write & Addr. Rename
20	THCV242 (Master)	0xZZ**	0x0032	0x00	1Byte addr./ 1Byte data(match THCV241A 0x00FE privious state)
21	THCV241A (Slave)	0xYY	0xFE	0x21	Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
22	THCV241A (Slave)	0xYY	0x06	0x00	0x1006 V-by-One® HS Tx software reset
23	THCV241A (Slave)	0xYY	0x05	0x00	0x1005 PLL software reset
24	THCV241A (Slave)	0xYY	0x21	0x00	0x1021 MIPI CSI-2 software reset
25	THCV241A (Slave)	0xYY	0x22	0x00	0x1022 Digital Logic clock software reset
26	THCV241A (Slave)	0xYY	0x23	0x00	0x1023 MIPI clock software reset
27	THCV241A (Slave)	0xYY	0xFF	0xAA	0x10FF Register reset
28	THCV242 (Master)	0xZZ**	0x0032	0x10	2Byte addr./ 1Byte data(match THCV241A 0x00FE default)
29	THCV241A (Slave)	0xYY	0x00FE	0x11	Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
30	THCV242 (Master)	0xZZ**	0x0032	0x00	Pass Through Divided write/read Addr.=1Byte, Data=1Byte
31	THCV241A (Slave)	0xYY	0xF3	0x00	(0x00F3) Sub-Link Rx Termination/Drive current
32	THCV241A (Slave)	0xYY	0xF2	0x22	(0x00F2) Sub-Link Tx Termination/Drive current
33	THCV241A (Slave)	0xYY	0xF0	0x03	(0x00F0/FF) Tuning register access Enable
34	THCV241A (Slave)	0xYY	0xFF	0x19	
35	THCV241A (Slave)	0xYY	0xF6	0x15	(0x00F6) Sub-Link frequency tuning
36	THCV241A (Slave)	0xYY	0xFE	0x21	Sub-Link Word Addr. Bank=0x10 & 1Byte Access from Master
37	THCV241A (Slave)	0xYY	0x2D	0x03	0x102D MIPI Data lane Disable
38	THCV241A (Slave)	0xYY	0x2C	0x00	0x102C MIPI Clock lane Disable
39	THCV241A (Slave)	0xYY	0x21	0x01	0x1021 MIPI CSI-2 software reset release
40	THCV241A (Slave)	0xYY	0x22	0x01	0x1022 Digital Logic clock software reset release
41	THCV241A (Slave)	0xYY	0x23	0x01	0x1023 MIPI clock software reset release
42	THCV241A (Slave)	0xYY	0xFE	0x00	Sub-Link Word Addr. 2Byte Access (default) from Master

**THCV242 i2c slave address depends on AIN settings.

2 Lane V-by-One® HS receiver establishment register example

2 Lane V-by-One® HS establishment may requires below register setting arrangement.

0x1014

0x12xx

0x1501

0x1704

Main-Link Equalizer setting reference

For most cases, Adaptive Equalizer mode (R_MLINK_AEQENn=1, n=0,1) works stable.

Register LEQOCn(n=0,1) shows automatically selected Adaptive Equalizer strength under current operation.

Main-Link signal integrity condition, receiver Eye-Diagram, is supposed to be examined by oscilloscope.

R_MLINK_LEQCTLRn(n=0,1), Main-Link Equalizer baseline Raise, can arrange signal integrity as secondary parameter. Basically R_MLINK_LEQCTLRn =000 default is supposed to be changed to large baseline gain like R_MLINK_LEQCTLRn =101 or else. Extremely short or long distance cases may require fine tuning of R_MLINK_LEQCTLRn.

R_MLINK_LEQCTLCn(n=0,1) offers capability of manual control on Equalizer strength under static Equalizer mode.

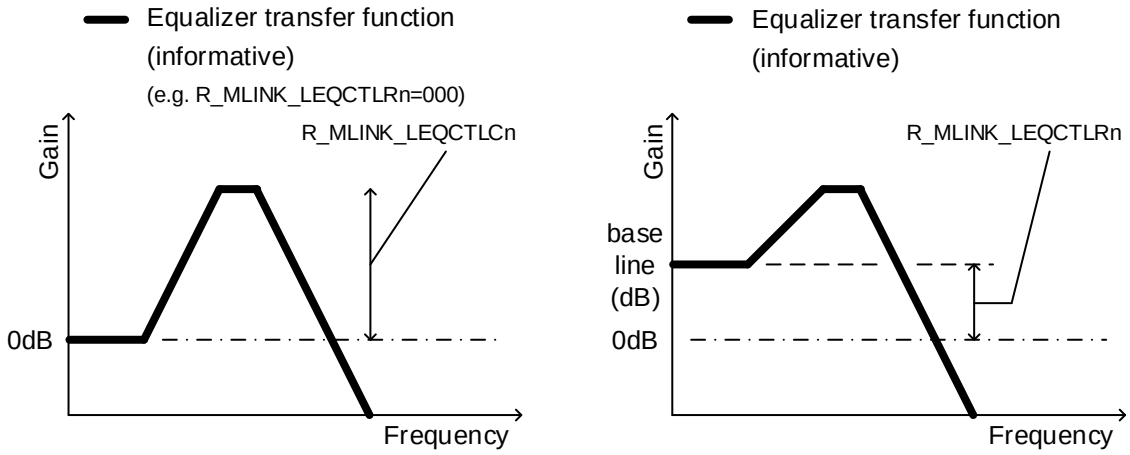


Figure 6 Schematic diagram of Equalizer control behavior

Sub-Link control reference

Sub-Link Master 2-wire Set and Trigger mode1 (2-wire Normal mode)

Below description is applied to Sub-Link Master 2-wire Set&Trigger mode1.

Access to Sub-Link Slave Register with 2-wire Set&Trigger mode

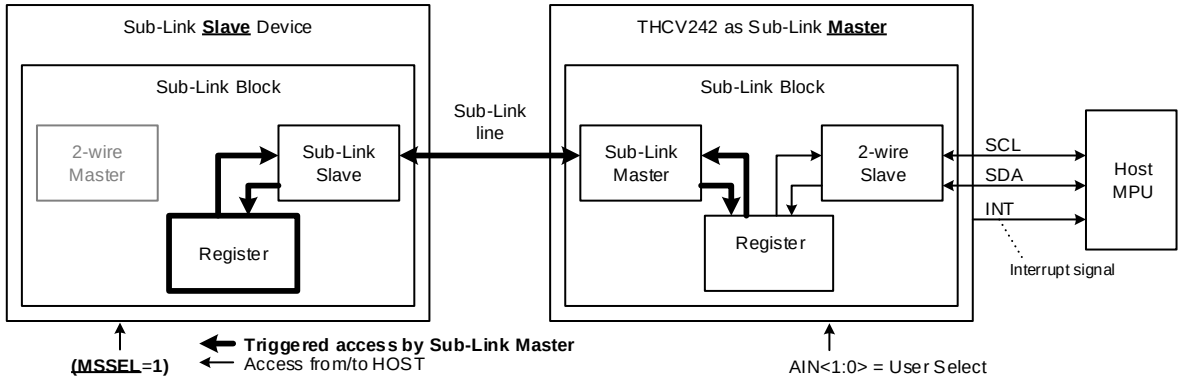


Figure 7 Access to remote SubLink slave register via 2-wire Set&Trigger mode THCV242 configuration

Table 15 Remote Sub-Link slave reg. write by THCV242 2-wire Set&Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear access status register (R_INTC_EXT2WIRE_ACSEND).	W	0x1725/172D[5:4]
2	Set start address of Sub-Link Slave register to write with needed addr. Byte (*1).	W	From 0x00D0
3	Set data for Sub-Link Slave to write, following after step2 address (*1).	W	(0x00Dx)-0x00DF
4	Set Device ID of Sub-Link Master device. (Value corresponding to AIN setting. e.g.[AIN]=[0] → 7'h0B)	W	0x00E0 bit[7:1]
5	Write 0 to indicate remote "write" access	W	0x00E0 bit0
6	Set Sub-Address Byte number of Sub-Link Slave (*1). (Byte num.= register value+1)	W	0x00E1 bit[6:4]
7	Set data Byte number to write to Sub-Link Slave (*1). (Byte num.= register value+1)	W	0x00E1 bit[3:0]
8	Select 2-wire remote access target path Enable on Lane0 and Lane1	W	0x00E4 bit[1:0]
9	Write 1 to R_2WIRE_START. (Start remote write access to Sub-Link Slave side)	W	0x00E5 bit0 (*2)
(10)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed, if R_2WIRE_CLKSEN=1 (Clock stretching Enable).	-	-
10	When write access is completed, R_INT_EXT2WIRE_ACSEND register value become 1 and interrupt occurs (INT=H → L), if R_2WIRE_CLKSEN=0 (No Clock stretching)	-	-
11	If write access was normally ended, R_INTC_EXT2WIRE_ACSEND read is "0x1".	R	0x1715/171D[5:4]

*1 R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd15 is recommended
*2 It is prohibited that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

Table 16 Remote Sub-Link slave reg. read by THCV242 Set&Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear access status register (R_INTC_EXT2WIRE_ACSEND).	W	0x1725/172D[5:4]
2	Set start address of Sub-Link Slave register to read with needed addr. Byte.	W	From 0x00D0
3	Set Device ID of Sub-Link Master device. (Value corresponding to AIN setting. e.g.[AIN]=[0] → 7'h0B)	W	0x00E0 bit[7:1]
4	Write 1 to indicate remote "read" access	W	0x00E0 bit0
5	Set Sub-Address Byte number of Sub-Link Slave. (Byte num.= register value+1)	W	0x00E1 bit[6:4]
6	Set data Byte number to read from Sub-Link Slave(*1) (Byte num.= register value+1)	W	0x00E1 bit[3:0]
7	Select 2-wire remote access target path, Lane0 or Lane1	W	0x00E3 bit[1:0]
8	Write 1 to R_2WIRE_START. (Start remote write access to Sub-Link Slave side)	W	0x00E5 bit0 (*2)
(9)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x00D0-0x00DF), if R_2WIRE_CLKSEN=1 (Clock stretching Enable).	-	-
9	When read access is completed, read data is stored in Sub-Link Master register (Address 0x00D0-0x00DF) and R_INTC_EXT2WIRE_ACSEND register value become 1 and interrupt occurs (INT=H → L), if R_2WIRE_CLKSEN=0 (No Clock stretching)	-	-
10	If read access was normally ended, R_INTC_EXT2WIRE_ACSEND read is "0x1".	R	0x1715/171D[5:4]
11	HOST MPU read data stored in Sub-Link Master register.	R	0x00D0-0x00DF

*1 R_2WIRE_DATA_BYTE < 'd16 (max 16Byte)
*2 It is prohibited that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

Access to 2-wire slave devices connected to Sub-Link Slave with 2-wire Set&Trigger mode

HOST MPU can access to remote side 2-wire serial slave register via THCV242 as Sub-Link Master and Sub-Link Slave by THCV242 as Sub-Link Master register settings on 2-wire Set&Trigger mode. Sub-Link Slave has 2-wire serial master block.

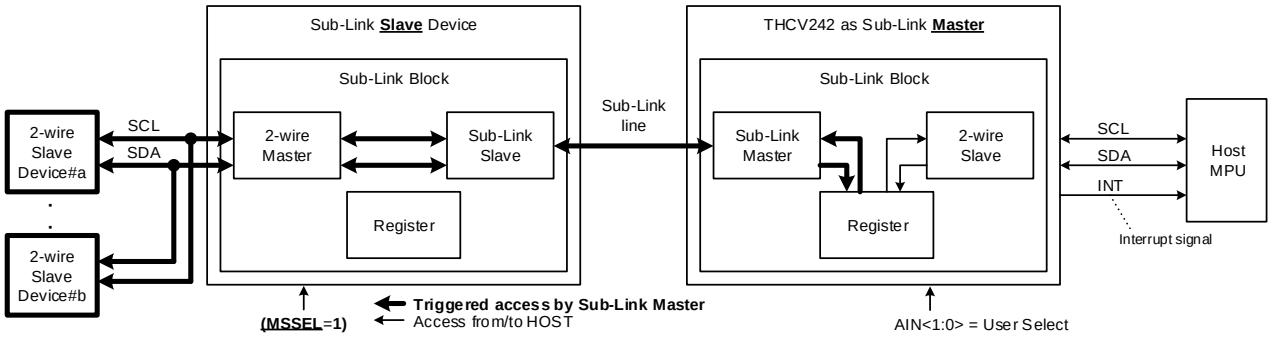


Figure 8 Host MPU to 2-wire slave devices at Sub-Link Slave side via THCV242 access configuration

Table 17 Remote 2-wire slave reg. write by THCV242 2-wire Set&Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear access status register (R_INTC_EXT2WIRE_ACSEND).	W	0x1725/172D[5:4]
2	Set start address of target 2-wire slave register to write with needed addr. Byte (*1).	W	From 0x00D0
3	Set data for target 2-wire slave to write, following after step2 address (*1).	W	(0x00Dx)-0x00DF
4	Set Device ID of target remote 2-wire slave device.	W	0x00E0 bit[7:1]
5	Write 0 to indicate remote “write” access	W	0x00E0 bit0
6	Set Sub-Address Byte number of 2-wire slave (*1). (Byte num.= register value+1)	W	0x00E1 bit[6:4]
7	Set data Byte number to write to 2-wire slave (*1). (Byte num.= register value+1)	W	0x00E1 bit[3:0]
8	Select 2-wire remote access target path Enable on Lane0 and Lane1	W	0x00E4 bit[1:0]
9	Write 1 to R_2WIRE_START. (Start remote write access to Sub-Link Slave side)	W	0x00E5 bit0 (*2)
(10)	2-wire serial slave of Sub-Link Master perform clock stretching until remote 2-wire register access is completed, if R_2WIRE_CLKSEN=1 (Clock stretching Enable).	-	-
10	When write access is completed, R_INT_EXT2WIRE_ACSEND register value become 1 and interrupt occurs (INT=H → L), if R_2WIRE_CLKSEN=0 (No Clock stretching)	-	-
11	If write access was normally ended, R_INT_EXT2WIRE_ACSEND read is “0x1”.	R	0x1715/171D[5:4]

*1 R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd15 is recommended
*2 It is prohibited that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

Table 18 Remote 2-wire slave reg. read by THCV242 Set&Trigger mode Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear access status register (R_INTC_EXT2WIRE_ACSEND).	W	0x1725/172D[5:4]
2	Set start address of 2-wire slave register to read with needed addr. Byte.	W	From 0x00D0
3	Set Device ID of target remote 2-wire slave device.	W	0x00E0 bit[7:1]
4	Write 1 to indicate remote “read” access	W	0x00E0 bit0
5	Set Sub-Address Byte number of target 2-wire Slave. (Byte num.= register value+1)	W	0x00E1 bit[6:4]
6	Set data Byte number to read from 2-wire Slave(*1) (Byte num.= register value+1)	W	0x00E1 bit[3:0]
7	Select 2-wire remote access target path, Lane0 or Lane1	W	0x00E3 bit[1:0]
8	Write 1 to R_2WIRE_START. (Start remote write access to Sub-Link Slave side)	W	0x00E5 bit0 (*2)
(9)	2-wire serial slave of Sub-Link Master perform clock stretching until remote 2-wire register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x00D0-0x00DF), if R_2WIRE_CLKSEN=1 (Clock stretching Enable).	-	-
9	When read access is completed, read data is stored in Sub-Link Master register (Address 0x00D0-0x00DF) and R_INTC_EXT2WIRE_ACSEND register value become 1 and interrupt occurs (INT=H → L), if R_2WIRE_CLKSEN=0 (No Clock stretching)	-	-
10	If read access was normally ended, R_INTC_EXT2WIRE_ACSEND read is “0x1”.	R	0x1715/171D[5:4]
11	HOST MPU read data stored in Sub-Link Master register.	R	0x00D0-0x00DF

*1 R_2WIRE_DATA_BYTE < 'd16 (max 16Byte)
*2 It is prohibited that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

Sub-Link Master 2-wire Pass Through mode1

Below descriptions are details of local and remote side 2-wire operation.

Divided Read operation always read target register by R_2WIREPT_DATA_BYTE defined unit. If R_2WIREPT_DATA_BYTE is not 0 (single read transaction unit is not 1Byte), 2-wire remote read operation may read access the address which originally user intends to read. As a result, 2-wire slave remote device may operate abnormal because of this unintended read action.

2-wire Pass Through mode1 Sub-Link Slave command, write and read

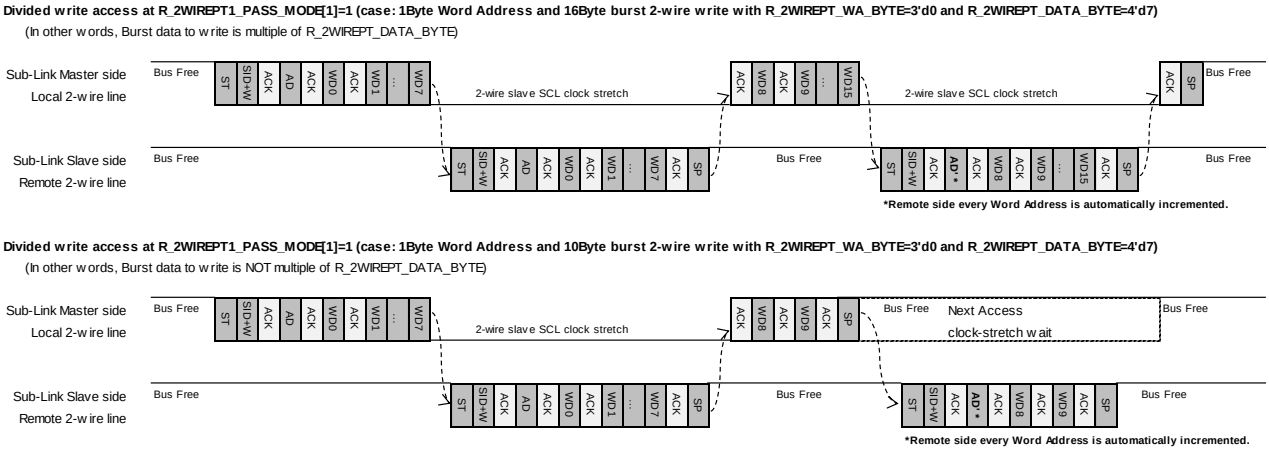
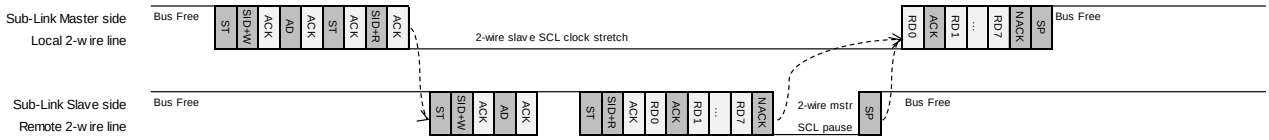


Figure 9 2-wire Pass Through mode1 Sub-Link Slave Divided Write

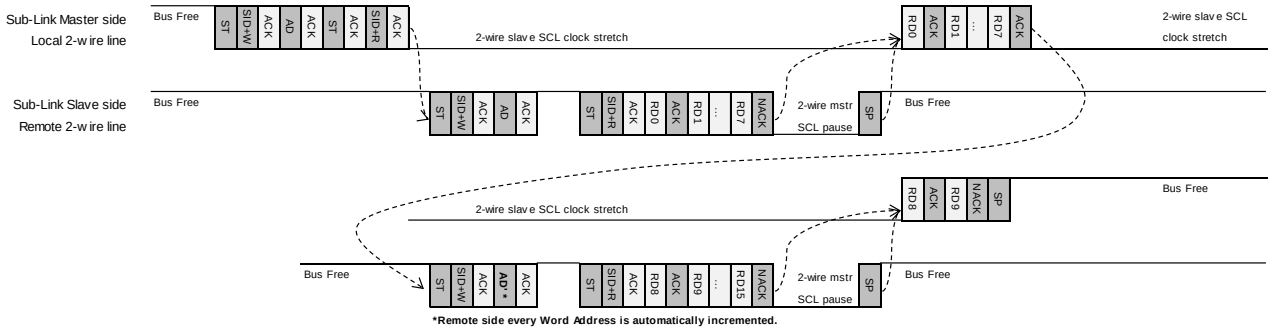
Divided read access at R_2WIREPT1_PASS_MODE[1]=1 (case: 1Byte Word Address and 8Byte burst 2-wire read with R_2WIREPT_WA_BYTE=3'd0 and R_2WIREPT_DATA_BYTE=4'd7)

(In other words, Burst data to read is multiple of R_2WIREPT_DATA_BYTE)



Divided read access at R_2WIREPT1_PASS_MODE[1]=1 (case: 1Byte Word Address and 10Byte burst 2-wire read with R_2WIREPT_WA_BYTE=3'd0 and R_2WIREPT_DATA_BYTE=4'd7)

(In other words, Burst data to read is NOT multiple of R_2WIREPT_DATA_BYTE)



[list of abbreviations]				
ST: Start Condition	ACK: Acknowledge	SID: Slave Address（Device Address）	WD: Write Data	+W: Write command indicator
SP: Stop Condition	NACK: No Acknowledge	AD: Word Address	RD: Read Data	+R: Read command indicator

Figure 10 2-wire Pass Through mode1 Sub-Link Slave Divided Read

Multiple camera synchronization reference

Several schemes to synchronize multiple camera by supplying the same VSYNC signal are prepared.

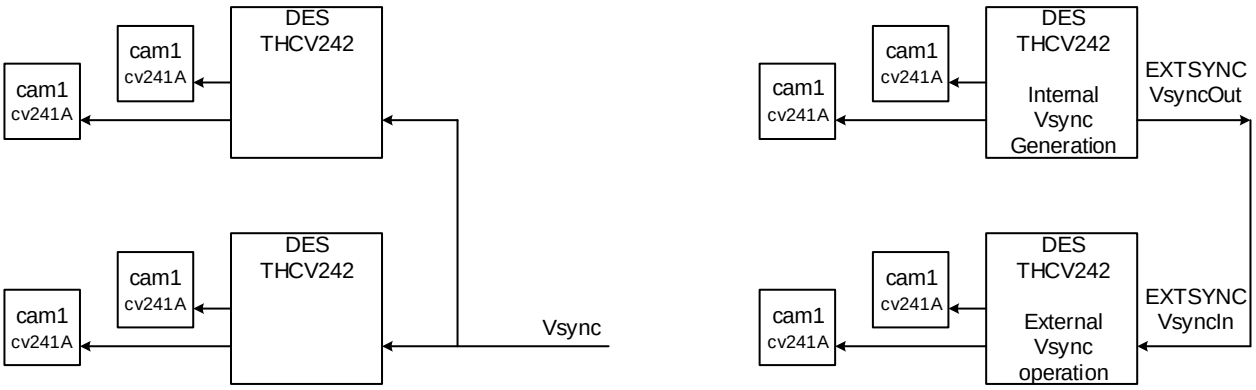


Figure 11 Multiple camera VSYNC synchronization control example

Time accuracy of VSYNC and camera framing can also be achieved by designed control.

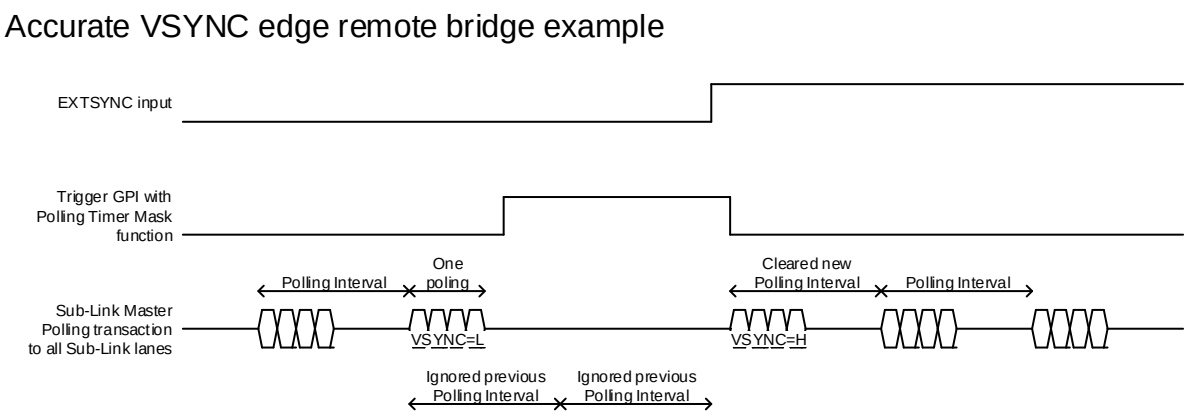


Figure 12 Accurate VSYNC supply timing control example

Polling Time Mask pulse is supposed to be long enough, way more than polling interval time to avoid collision against previous Sub-Link polling cycle in above example.

Through GPIO examples

As a default setting with THCV241A other than Polling strengthen mode, several alternatives of Through GPIO modes for rather time-accurate signals are available. The rest of GPIO can be used as Register GPIO for slow DC signals. Below are some examples.

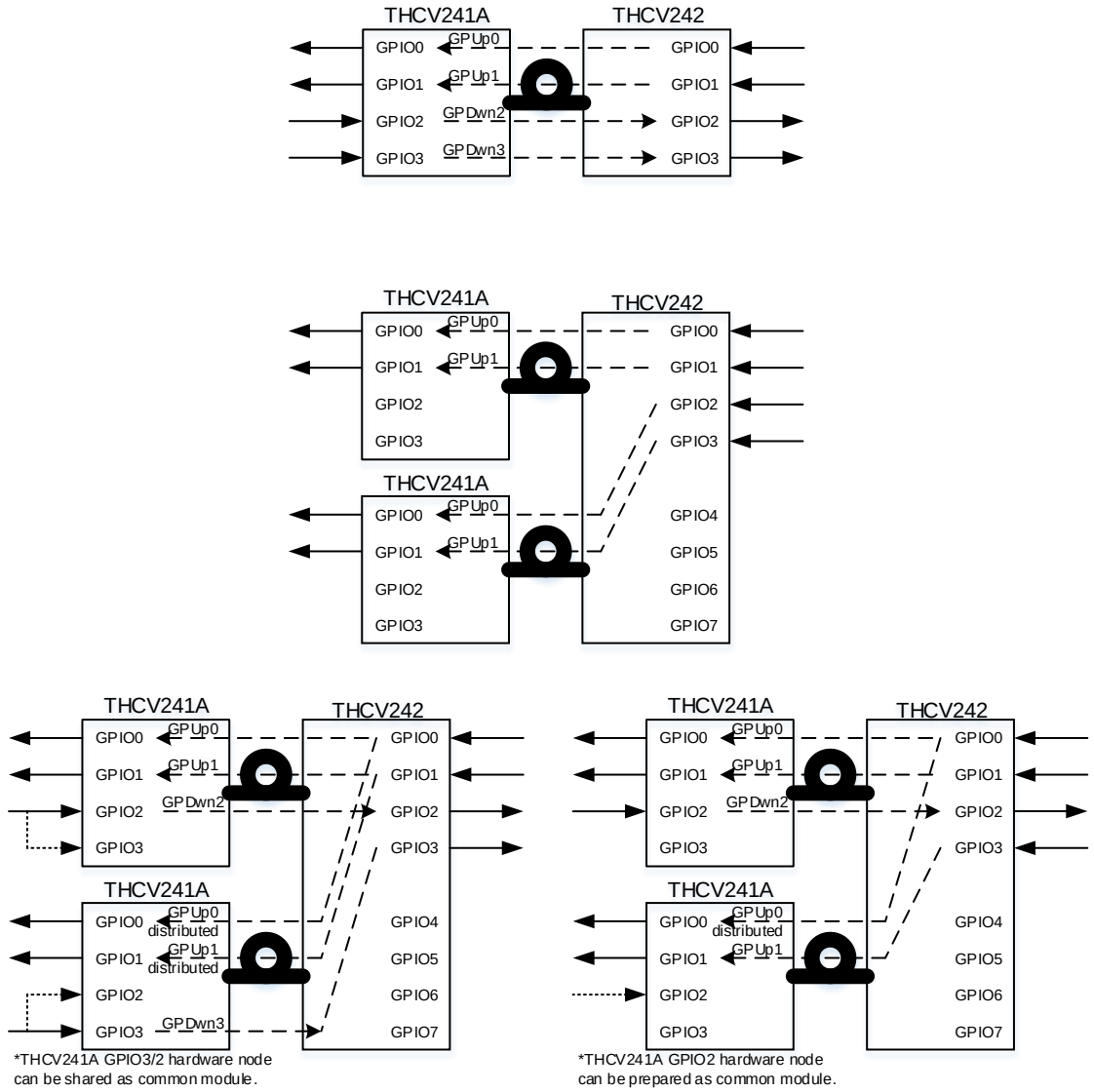


Figure 13 Through GPIO configration examples

Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 0.1uF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. All supply pins need capacitor placement one by one.
- Use the same ground plane for all ground pins including EXPGND.

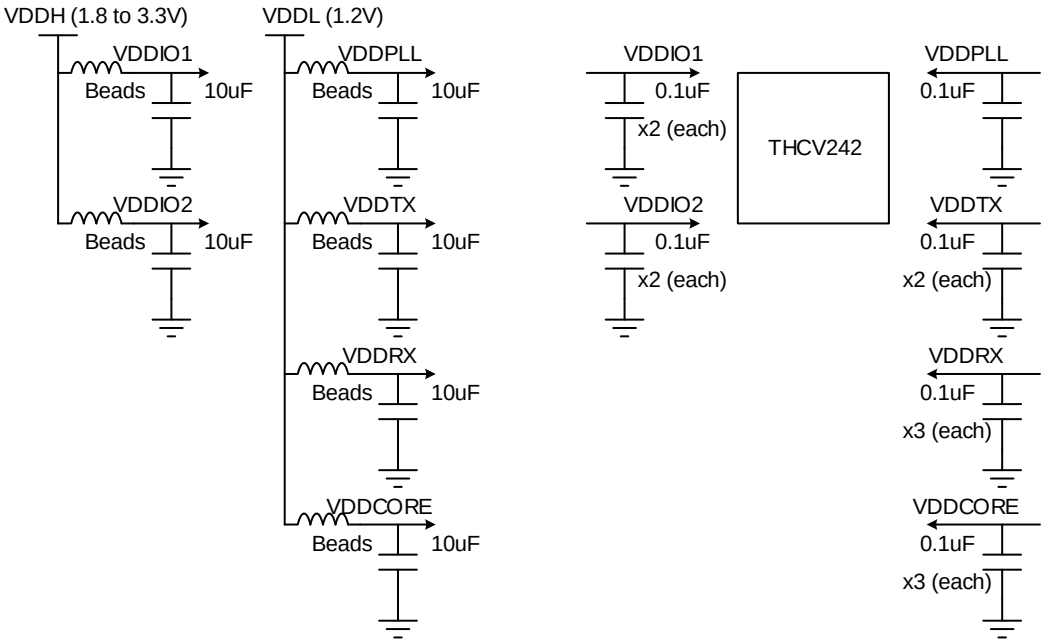


Figure 14 Power supply recommendation

Note

1)Power On Sequence

Don’t input clock nor data before THCV242 is on in order to keep absolute maximum ratings.

2)Cable Connection and Disconnection

Don’t connect and disconnect MIPI, CMOS and CML cable/connector, when power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB where THCV242 and V-by-One® HS transmitter are on it. It is better for EMI reduction to place GND cable as close to CMOS and CML cable as possible.

4)MIPI transmitter AC timing control requirement

MIPI Tx $T_{CLK\text{-}PREPARE}$ and $T_{HS\text{-}PREPARE}$ had better be greater than 85ns as setting value.

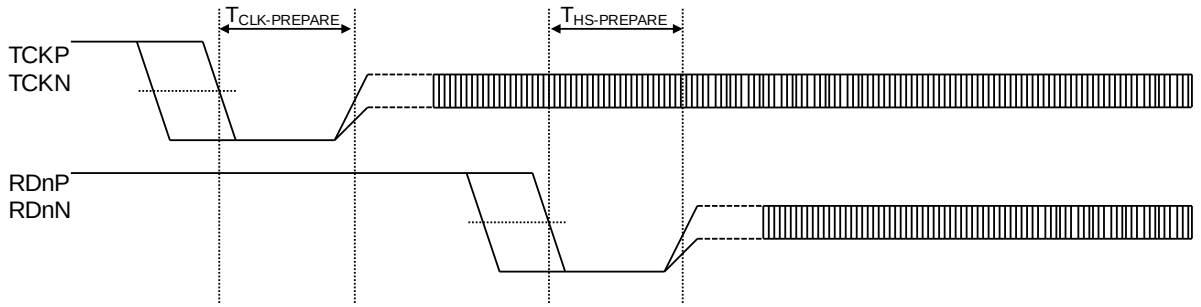


Figure 15 MIPI transmitter TCLK_PREPARE and THS_PREPARE

(Informative)1st Trial setting reference are shown below.

Table 19 MIPI transmitter TCLK_PREPARE and THS_PREPARE 1st trial setting reference

Tclk_prepare	Ths_prepare
CLK lane PrePare period setting	Data lane Prepare period setting
time period setting by [{1/F(OUT)}*8]	time period setting by [{1/F(OUT)}*8]
arrangement with counterpart MIPI Rx is required.	arrangement with counterpart MIPI Rx is required.
(informative)setting reference with data-rate	(informative)setting reference with data-rate
(informative)0x06 from 1.5Gbps to 1.3Gbps	(informative)0x06 from 1.5Gbps to 1.4Gbps
(informative)0x05 from 1.3Gbps to 1.2Gbps	(informative)0x05 from 1.4Gbps to 1.2Gbps
(informative)0x05 from 1.2Gbps to 1.1Gbps	(informative)0x04 from 1.2Gbps to 1Gbps
(informative)0x04 from 1.1Gbps to 1Gbps	(informative)0x03 from 1Gbps to 700Mbps
(informative)0x03 from 1Gbps to 750Mbps	(informative)0x02 from 700Mbps to 450Mbps
(informative)0x02 from 750Mbps to 500Mbps	(informative)0x01 from 450Mbps to 80Mbps
(informative)0x01 from 500Mbps to 250Mbps	
(informative)0x00 from 250Mbps to 80Mbps	

(Informative)When above setting is not optimum with result observation, back up alternatives are shown below. Intermediate setting value may be available. Long time setting of $T_{CLK\text{-}PREPARE}$ and $T_{HS\text{-}PREPARE}$ may require connectivity check with counterpart MIPI receiver timing margin.

Table 20 MIPI transmitter TCLK_PREPARE and THS_PREPARE back up setting reference

Tclk_prepare	Ths_prepare
Back up setting reference for several data-rate	Back up setting reference for several data-rate
Arrangement with counterpart MIPI Rx is required.	Arrangement with counterpart MIPI Rx is required.
(informative)setting reference with data-rate	(informative)setting reference with data-rate
(informative)0x10 for 1.5Gbps	(informative)0x10 for 1.5Gbps
(informative)0x0F for 1.4Gbps	(informative)0x0F for 1.4Gbps
(informative)0x0E for 1.3Gbps	(informative)0x0E for 1.3Gbps
(informative)0x0C for 1.2Gbps	(informative)0x0C for 1.2Gbps
(informative)0x0B for 1.1Gbps	(informative)0x0B for 1.1Gbps
(informative)0x0A for 1Gbps	(informative)0x0A for 1Gbps
(informative)0x09 for 900Mbps	(informative)0x09 for 900Mbps
(informative)0x08 for 750Mbps	(informative)0x08 for 750Mbps
(informative)0x07 for 680Mbps	(informative)0x07 for 700Mbps
(informative)0x06 for 600Mbps	(informative)0x06 for 600Mbps
(informative)0x05 for 500Mbps	(informative)0x05 for 500Mbps
(informative)0x04 for 400Mbps	(informative)0x05 for 450Mbps
(informative)0x03 for 320Mbps	(informative)0x04 for 400Mbps
(informative)0x02 for 250Mbps	(informative)0x03 for 320Mbps
(informative)0x01 for 160Mbps	(informative)0x03 for 250Mbps
(informative)0x00 for 80Mbps	(informative)0x02 for 160Mbps
	(informative)0x01 for 80Mbps

5)Local and remote 2-wire serial access requirement

Local and remote 2-wire serial access at the same time may be prohibited on Sub-Link Slave device. For multiple controller application, command collision avoidance scheme is supposed to be prepared.

Below figure is an example of schematic diagram of time domain or indicator driven command separation.

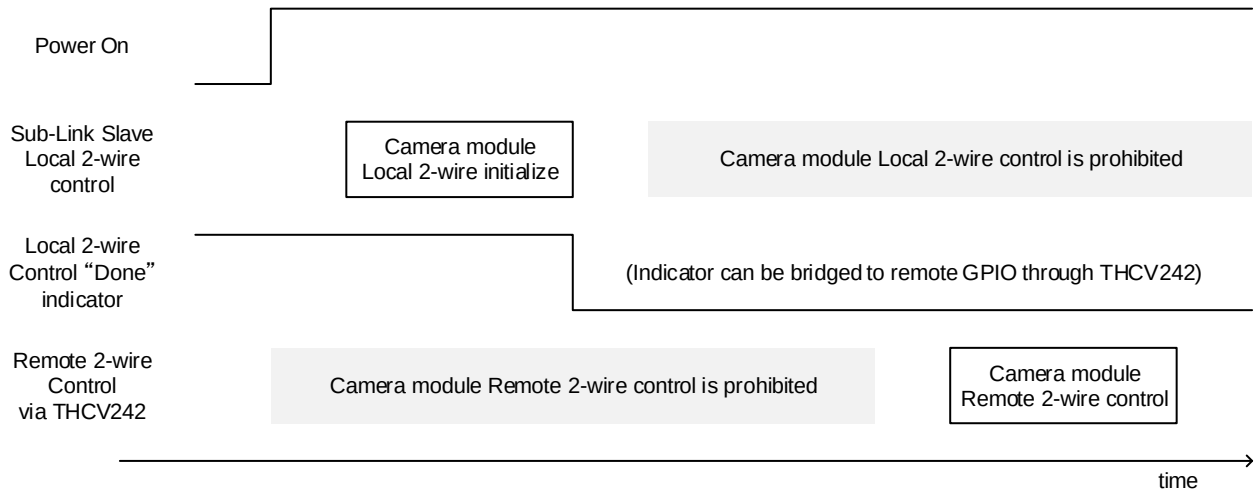


Figure 16 2-wire local and remote access timing chart

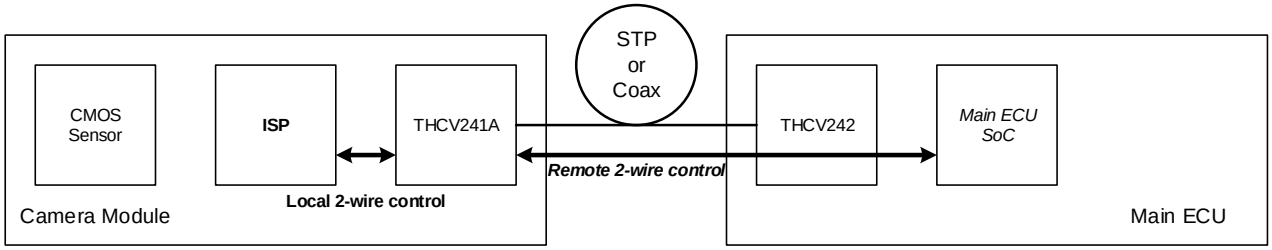


Figure 17 2-wire local and remote access configuration

6)ERR detect function transition time behavior

Main-Link Rx ERR detect fault at LOCKN=H=>L and LOCKN=L=>H=>L transition time. ERR detection is reasonable on this time period because at the beginning of transition, Main-Link is not yet logically stable before all the training is done, while Main-Link Rx ERR detection already starts as normal behavior.

User must ignore Main-Link Rx ERR detection on this time period.

7)INT function initialization

INT interrupt function is supposed to be cleared before start monitoring any desired status because INT status may change at power on condition and THCV242 internal boot up procedure.

8)Sub-Link PHY setting at the beginning of Sub-Link transaction

Sub-Link Tx PHY setting (ex. THCV242 Address 0x0102/0x0103) is supposed to be optimized before any Sub-Link transaction especially when THCV242 was used under noisy environment. Sub-Link Tx PHY setting can be severer in case counterpart THCV241A is Sub-Link Slave because any setting is done through Sub-Link. Below Sub-Link PHY initialize sample code can be repeated from Sub-Link Master if this particular Sub-Link transaction did not succeed before other settings.

----- Here is at the beginning of THCV241A-242 initialization by 2-wire Pass Through mode1 example -----

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x0050	0xYY	Sub-Link Slave Access Addr. (e.g. YY=0x51)
2	THCV242 (Master)	0xZZ**	0x0004	0x03	Sub-Link Mode setting (Pass Through mode1)
3	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
4	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
5	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
6	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
7	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
8	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
9	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
10	THCV242 (Master)	0xZZ**	0x010F	0x25	
11	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
12	THCV242 (Master)	0xZZ**	0x0031	0x02	Pass Through mode Divided write & Addr. Rename
13	THCV242 (Master)	0xZZ**	0x0032	0x10	Pass Through Divided write/read Addr.=2Byte, Data=1Byte
14	THCV241A (Slave)	0xYY	0x00FE	0x11	Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
15	THCV242 (Master)	0xZZ**	0x0032	0x00	Pass Through Divided write/read Addr.=1Byte, Data=1Byte
16	THCV241A (Slave)	0xYY	0xF3	0x00	(0x00F3) Sub-Link Rx Termination/Drive current
17	THCV241A (Slave)	0xYY	0xF2	0x22	(0x00F2) Sub-Link Tx Termination/Drive current
18	THCV241A (Slave)	0xYY	0xF0	0x03	(0x00F0/FF) Tuning register access Enable
19	THCV241A (Slave)	0xYY	0xFF	0x19	
20	THCV241A (Slave)	0xYY	0xF6	0x15	(0x00F6) Sub-Link frequency tuning
21	THCV242 (Master)	0xZZ**	0x0010	0x11	Sub-Link Enable On/Polling ON

**THCV242 i2c slave address depends on AIN settings.

----- Other settings continue from here. -----
----- Other settings -----
----- Other settings -----

----- Here is at the beginning of THCV241A-242 initialization by 2-wire Set&Trigger mode1 example -----

Step	Device (M/S)	i2c Slv. Address	Sub Address	Write Data	memo
1	THCV242 (Master)	0xZZ**	0x0004	0x01	Sub-Link Mode setting (Set&Trig. mode1)
2	THCV242 (Master)	0xZZ**	0x0010	0x10	Sub-Link Enable On/Polling OFF
3	THCV242 (Master)	0xZZ**	0x1704	0x01	Sub-Link Power On
4	THCV242 (Master)	0xZZ**	0x0102	0x02	Sub-Link Tx Termination Lane0
5	THCV242 (Master)	0xZZ**	0x0103	0x02	Sub-Link Tx Drive current Lane0
6	THCV242 (Master)	0xZZ**	0x0104	0x00	Sub-Link Rx Termination Lane0
7	THCV242 (Master)	0xZZ**	0x0105	0x00	Sub-Link Rx Drive current Lane0
8	THCV242 (Master)	0xZZ**	0x0100	0x03	Tuning register access Enable
9	THCV242 (Master)	0xZZ**	0x010F	0x25	
10	THCV242 (Master)	0xZZ**	0x010A	0x15	Sub-Link frequency tuning
11	THCV242 (Master)	0xZZ**	0x00E4	0xWW	Sub-Link transaction write lane select (e.g. WW=0x01 for Lane0)
12	THCV242 (Master)	0xZZ**	0x00D0	0x00	THCV241A (Slave) setting Sub-Link Word Addr. Bank=0x00 & 1Byte Access from Master
	THCV242 (Master)	0xZZ**	0x00D1	0xFE	
	THCV242 (Master)	0xZZ**	0x00D2	0x11	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x10	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
13	THCV242 (Master)	0xZZ**	0x00D0	0xF3	THCV241A (Slave) setting (0x00F3) Sub-Link Rx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x00	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
14	THCV242 (Master)	0xZZ**	0x00D0	0xF2	THCV241A (Slave) setting (0x00F2) Sub-Link Tx Termination/Drive current
	THCV242 (Master)	0xZZ**	0x00D1	0x22	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
15	THCV242 (Master)	0xZZ**	0x00D0	0xF0	THCV241A (Slave) setting (0x00F0/FF) Tuning register access Enable
	THCV242 (Master)	0xZZ**	0x00D1	0x03	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
	THCV242 (Master)	0xZZ**	0x00D0	0xFF	
	THCV242 (Master)	0xZZ**	0x00D1	0x19	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
16	THCV242 (Master)	0xZZ**	0x00D0	0xF6	THCV241A (Slave) setting (0x00F6) Sub-Link frequency tuning
	THCV242 (Master)	0xZZ**	0x00D1	0x15	
	THCV242 (Master)	0xZZ**	0x00E0	0x(ZZ || 0)***	
	THCV242 (Master)	0xZZ**	0x00E1	0x00****	
	THCV242 (Master)	0xZZ**	0x00E5	0x01	
17	THCV242 (Master)	0xZZ**	0x0010	0x11	Sub-Link Enable On/Polling ON

**THCV242 i2c slave address depends on AIN settings.

***[7:1]R_2WIRE_DEVADR=ZZ || [0]R_2WIRE_WR=0:write. 0x00E0 write action can be eliminated from 2nd time because no change occurred from previous setting.

****0x00E1 write action can be eliminated because no change occurred from previous setting.

----- Other settings continue from here. -----

----- Other settings -----

----- Other settings -----

9)Data stream handler reset control requirement under severe noise event

Data stream handler may stop operation so that MIPI output from THCV242 output no signal under severe noise event such as Electro Static Discharge, etc.

For robust operation against noisy environment, external MCU as redundancy safety mechanism is supposed to be prepared and do the following steps.

As first step, MCU must watch and detect interrupt event of data stream handler error, R_INTR_DSHNDLRx[4], which can be monitored as external pin output or 2-wire register read.

As second step, when the data stream handler error is detected, MCU must reset data stream handler block by 2-wire register control to R_DSHNDLR_RST.

10)Data stream handler error detection interrupt control proper setting

Data stream handler error Interrupt detection requires appropriate condition teaching.

Table 21 Data stream Handler error interrupt condition teaching

Adr	bit	Register Name	width	R/W	init	Description
0x17 0F	[7:2]	reserved	6	-	-	-
0x17 0F	[1:0]	R_DSHNDLR_INTSEL	2	R/W	2'd3	Data stream Handler Interrpution Detection condition teaching 0:Main-Link side input upstream is faster 1:MIPI side output dow nstream is faster 2,3:Both stream is the same speed

$$\text{Main-Link side input upstream} = [F(\text{Main-Link input})] = [PCLK.input] = [F(\text{upstream})]$$

$$\text{MIPI side output downstream} = [F(\text{downstream})] = \frac{[F(\text{MIPI output})]}{8}$$

Table 22 Data stream Handler error interrupt condition teaching example

Format	[F(dow nstream)] / [F(upstream)] frequency ratio			
	[Main-Link input lane#]=1		[Main-Link input lane#]=2	
	Distribution=off	Distribution=on	Distribution=off	Distribution=on
MPRF	1	2	2	4
RGB888	*3/4*	6/4	6/4	3
YUV422 Normal	*2/4*	1	1	2
YUV422 Demux	1	2	2	4
RAW8 Normal	*2/4*	1	1	2
RAW8 Demux	1	2	2	4
RAW10 Normal	*10/32*	*20/32*	*20/32*	40/32
RAW10 Demux	*20/32*	40/32	40/32	80/32
RAW12 Normal	*12/32*	*24/32*	*24/32*	48/32
RAW12 Demux	*24/32*	48/32	48/32	96/32

	R_DSHNDLR_INTSEL setting
	0:Main-Link side input upstream is faster
	1:MIPI side output dow nstream is faster
1	2,3:Both stream is the same speed

11)Sub-Link Master 2-wire Pass Through mode Read Byte setting care

Divided Read operation always read target register by R_2WIREPT_DATA_BYTE defined unit. If R_2WIREPT_DATA_BYTE is not 0 (single read transaction unit is not 1Byte), 2-wire remote read operation may read access the address which originally user intends to read. As a result, 2-wire slave remote device may operate abnormal because of this unintended read action.

12)Sub-Link remote 2-wire access command transmission failure handling

Sub-Link 2-wire access in noisy environment may collapse as single transaction against fair enough access success rate. Informative several functional safety mechanism will be shown here.

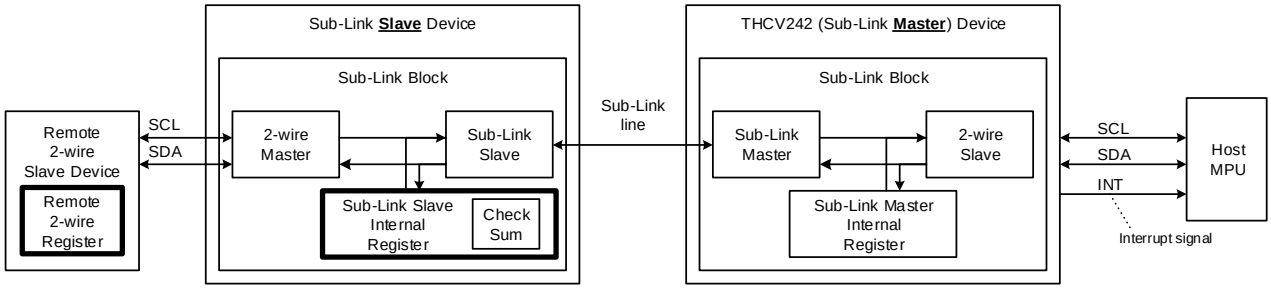


Figure 18 Sub-Link 2-wire remote access configuration

One option is to place MCU on remote Sub-Link Slave side. Internal PCB communication can eliminate external module noise bothersome elements. Sub-Link, still, provide best-effort remote command communication channel.

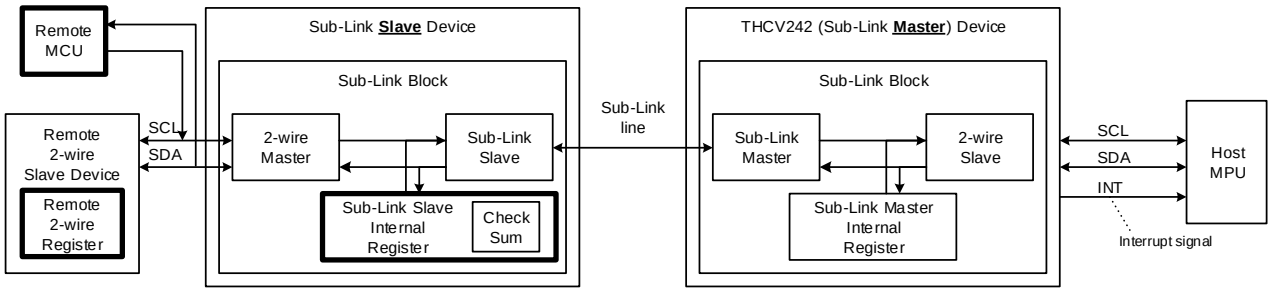


Figure 19 Sub-Link 2-wire remote access configuration

Another option is “action, confirm, re-action, and reconfirm” redandant command access procedure. As informative content, collapsed read action is likely to return 0x00 data, while collapsed read action is not likely to return “just right” data. Repeat read results gives statistical estimate value of access target. Sub-Link Slave device may have checksum information of all internal register so that checksum data can be used for total register status.

Write example						
	Write	=>	Read	=>	Read	=>	Re-write if expected value is not read
Read example						
	Read	=>	Read	=>	Read	=>	Filter outlier and process statistically

13)Sub-Link basic protocol setting change in the middle of active operation

Except initialization procedure, R_SLINK_MODE (THCV242 register address 0x0004) change in the middle of active operation requires Sub-Link operation suspension by R_SLINK_EN or R_SLINK_PLO_EN (THCV242 register address 0x0010). After R_SLINK_MODE change action in the middle of Sub-Link suspension, Sub-Link operation can be resumed.

14)Power On Reset Control requirement

Power On Reset control is required.
One thing for sure is that VDDH must precedes VDD12 supply by t1.
2nd thing for sure is that VDD12 must precedes PDN control by t2.

Since logic reset is governed by VDD12 power domain, PDN control must be delayed after VDD12 ready state. While, on the other hands, PDN pin itself belongs to VDDH power domain. Power On Reset control is supposed to care about relationships not only VDDH but also VDD12 power on sequence.

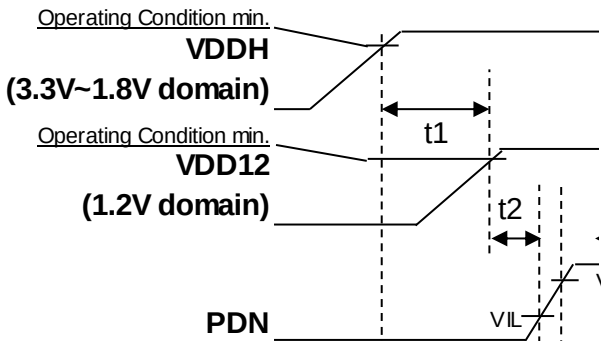


Figure 20 Power On Reset requirement

(Informative) About 1ms order delay from VDDH power supply to PDN Low keeping is considerable. Even in this case, VDD12 supply must precede PDN control as described. In addition, passive Low Path Filter configuration like below-left figure especially with high resistor could be “NOT appropriate” in particular cases where noise robust operation against EMC Immunity or ESD noise is required for mass production model.

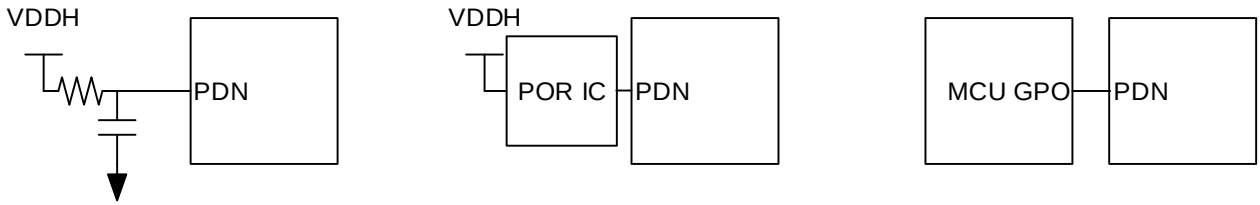


Figure 21 Power On Reset alternatives

15)MIPI HS-zero arrangement for distribution mode operation

When using distribution mode, MIPI HS_zero Data Lane ZERO period setting may be required to be arranged on each MIPI output lanes.

Vertical belt-like abnormal image on left or right edge of video frame may have relationship with HS zero.

16)Temperature and Voltage drift environment care on V-by-One® HS offset cancell function

Temperature and voltage drift can change the optimized setting of V-by-One® HS receiver, while offset cancell function autonomous setting establishment is held at the beginning of reset operation. For example, when temperature is severely drifted from -40degrees Celsius to 105degrees Celsius by system itself heat in hard winter, Main-Link CRC error or LOCKN unlock happens because of this opetimized-at-the-beginning-but-not-suited-at-the-end offset cancel setting of V-by-One® HS receiver.

Main-Link CRC or LOCKN states are supposed to be monitored by MCU and V-by-One® HS block had better be reset by register control under the temperature and voltege drift severe environment.

17)Frequency change care on V-by-One® HS

Basically active frequency change in the middle of normal operaion is not allowed.

If and only if frequency change in the middle of operation is inevitable, V-by-One® HS block is required to be reset by register control after target operaion frequency stabled status.

PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

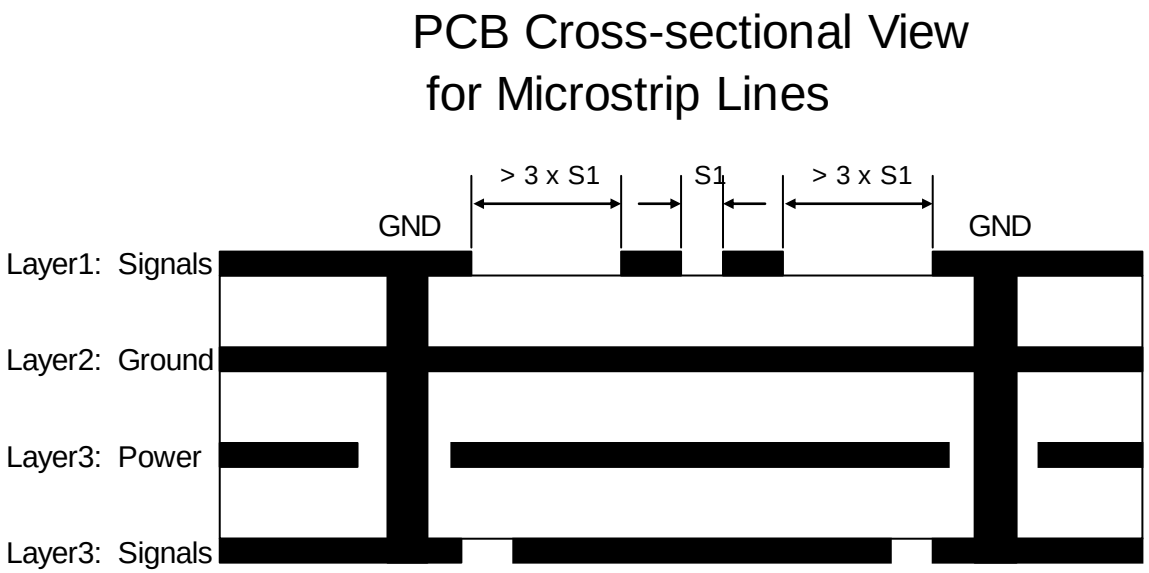


Figure 22 PCB cross-sectional view

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2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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