Application Note	*THCV233-234_Design Guide_Rev.2.00_E*

THCV233/THCV234 Application Note

System Diagram and PCB Design Guideline

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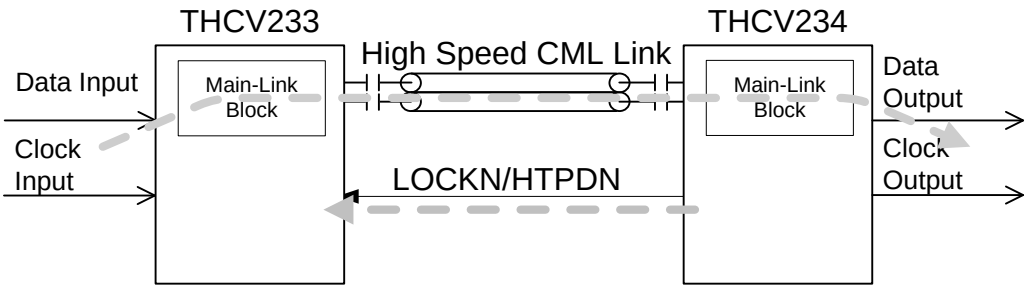
Selection table

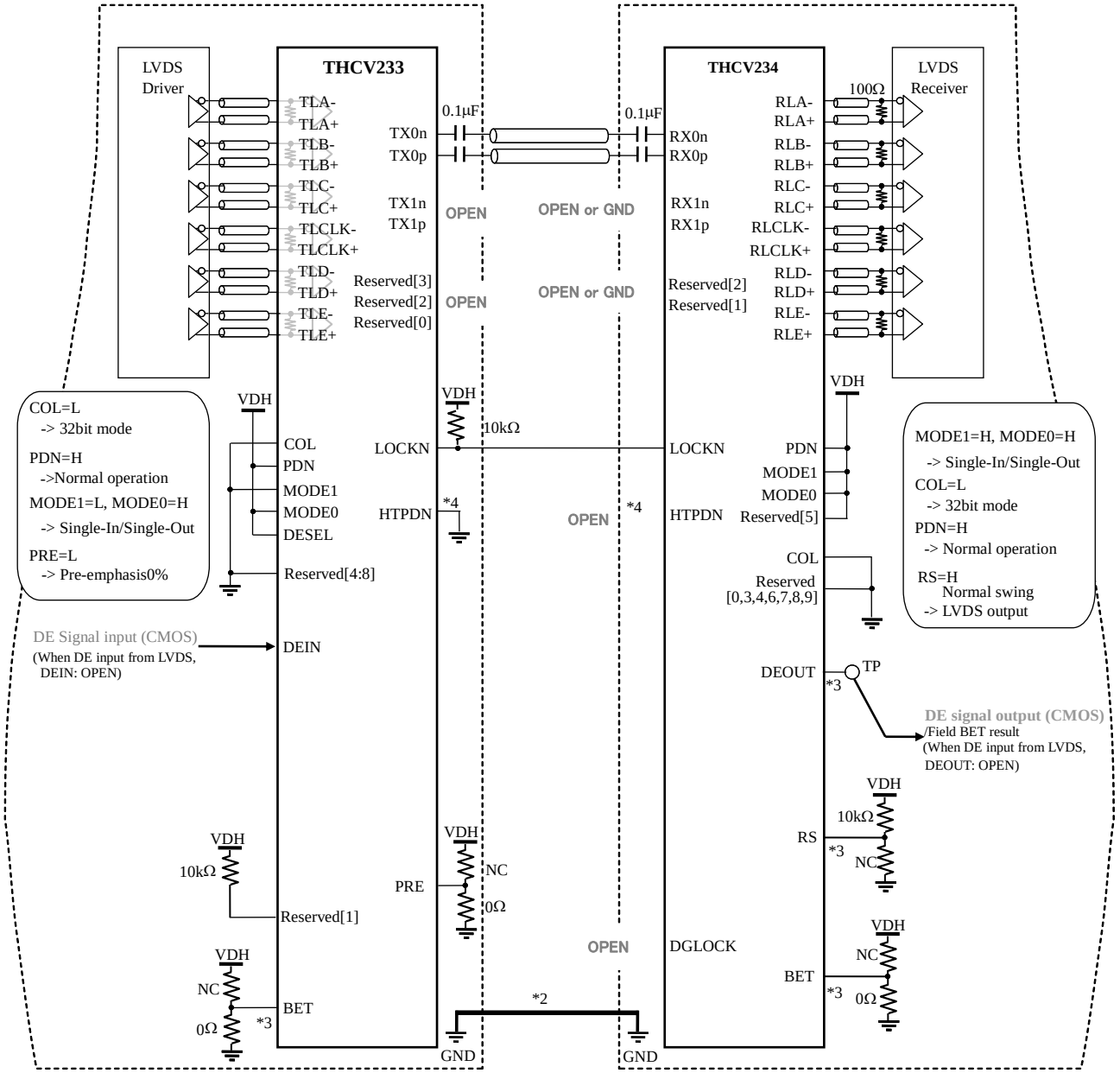
*High Speed CML Link



High Speed CML Link Operation		Case No. Page No.
THCV233	THCV234	
Single-In/Single-Out 32bit @85MHz LVDS → 3.4G	Single-In/Single-Out 3.4G → 32bit @85MHz LVDS	**Case 1 →Page 5**
Single-In/Dual-Out 32bit @85MHz LVDS → 1.7G, 1.7G	Dual-In/Single-Out 1.7G, 1.7G → 32bit @85MHz LVDS	**Case 2 →Page 6**
Single-In/Single-Out * 2 32bit @85MHz LVDS → 3.4G 32bit @85MHz LVDS → 3.4G	Dual-In/Selected Single-Out 3.4G, 3.4G → 32bit @85MHz LVDS	**Case 3 →Page 7**
Single-In/Distributed Dual-Out 32bit @85MHz LVDS → 3.4G, 3.4G	Single-In/Single-Out * 2 3.4G → 32bit @85MHz LVDS 3.4G → 32bit @85MHz LVDS	**Case 4 →Page 8**

Application Diagram (Case1)

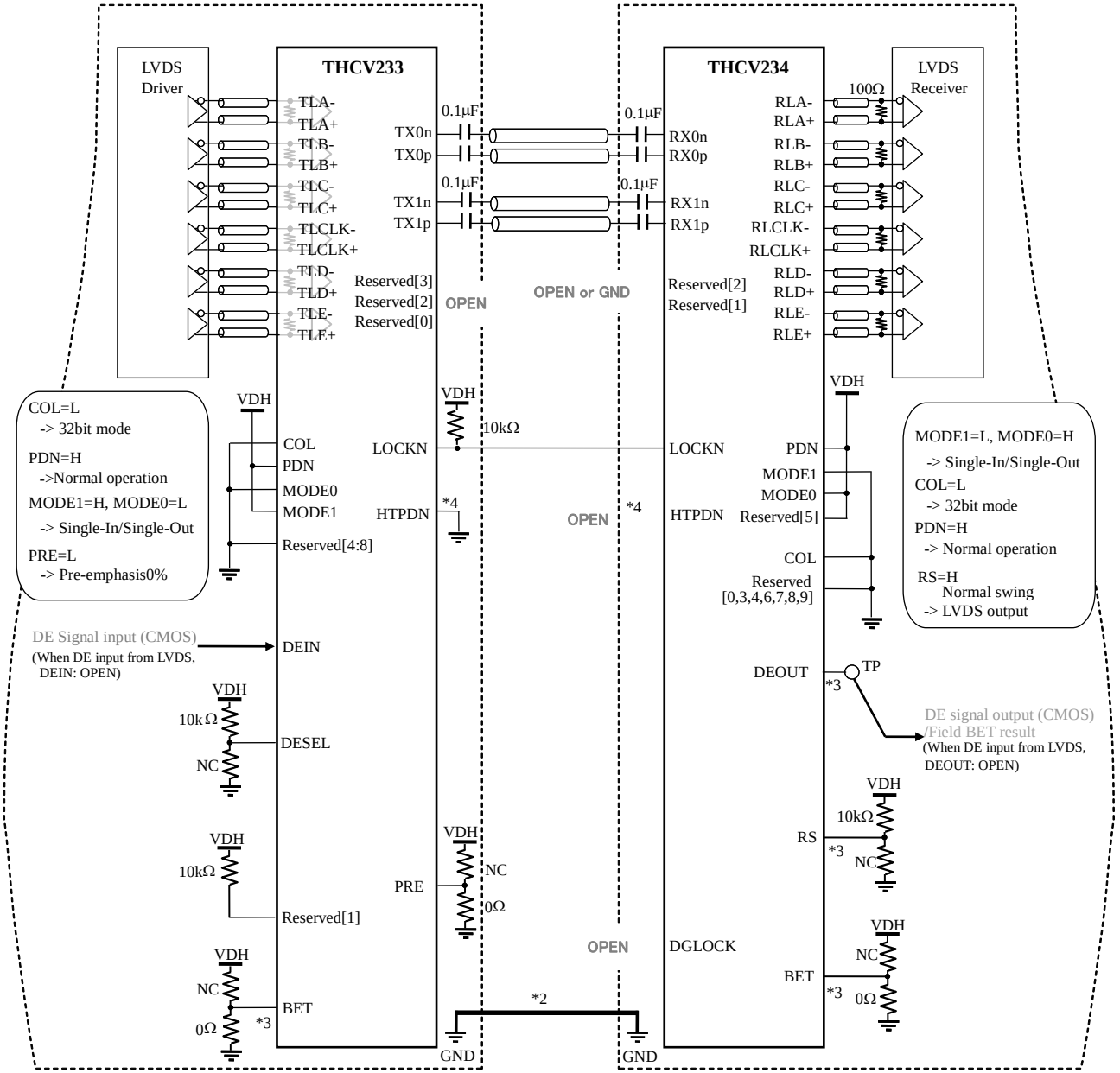
Case1	High Speed CML-Link
THCV233	Single-In/Single-Out
THCV234	Single-In/Single-Out



*1 indicates micro-strip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)
*4 No HTPDN connection option. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)

Application Diagram (Case2)

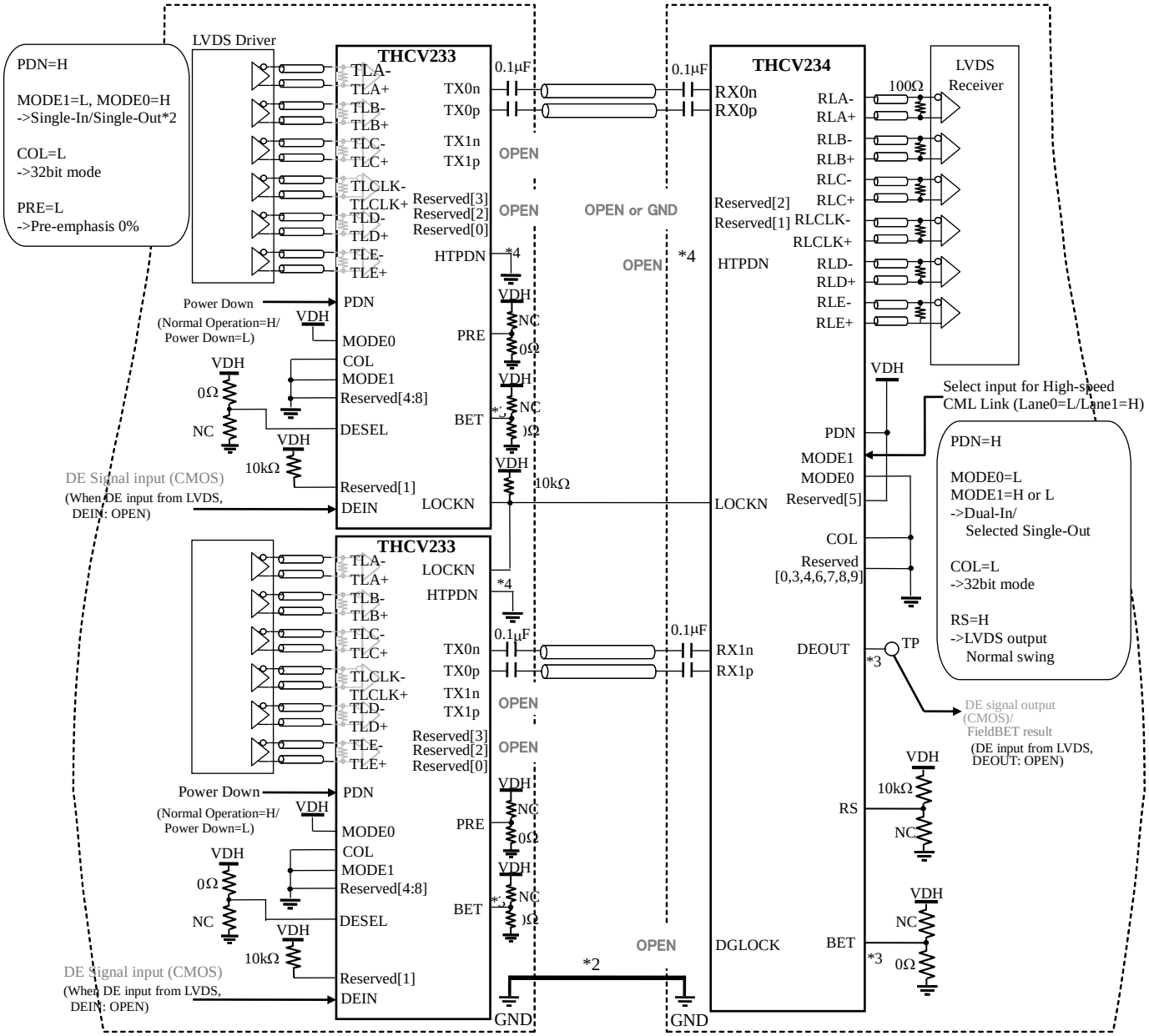
Case2	High Speed CML-Link
THCV233	Single-In/Dual-Out
THCV234	Dual-In/Single-Out



*1 indicates micro-strip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)
*4 No HTPDN connection option. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)

Application Diagram (Case3)

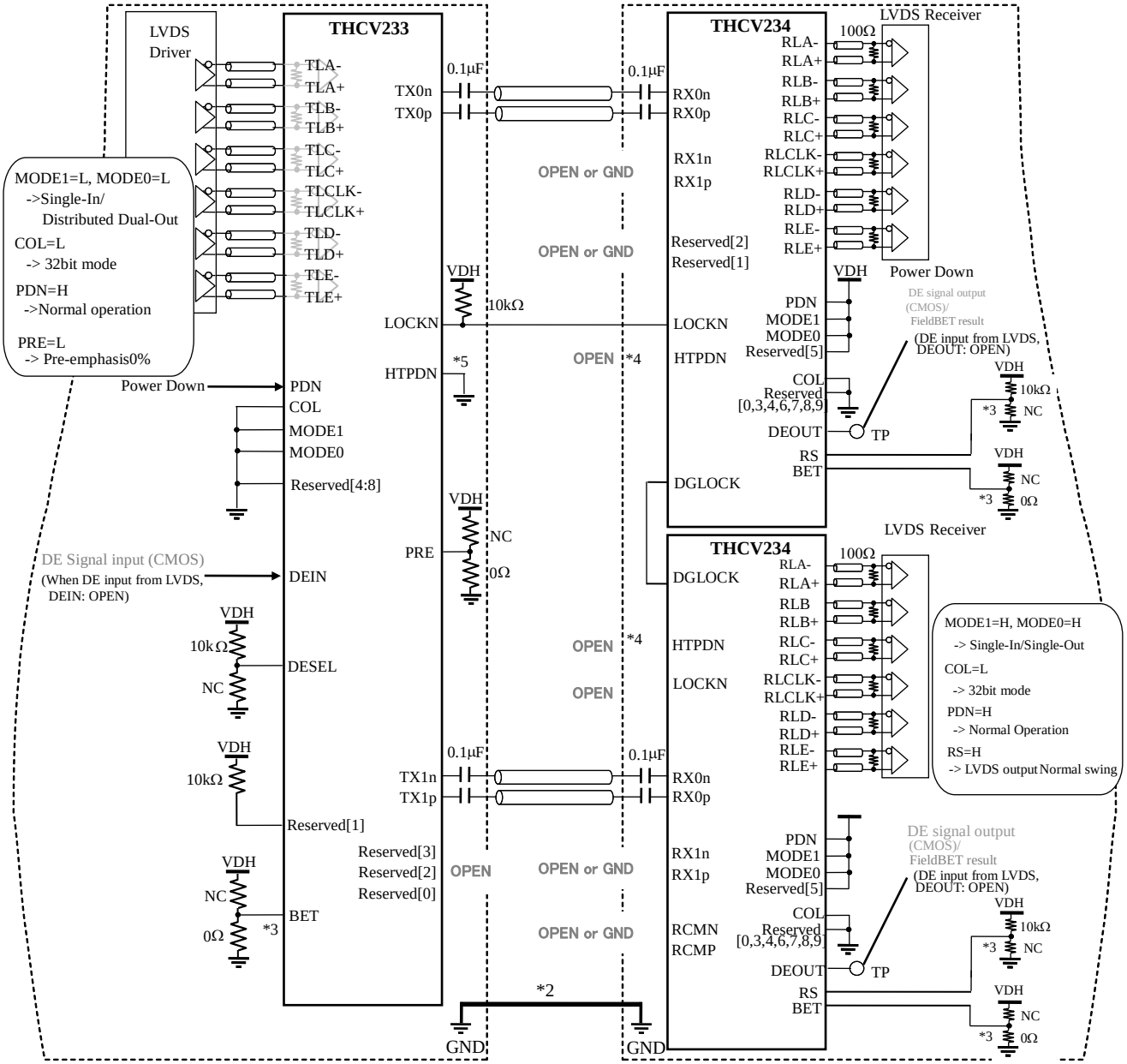
Case3	High Speed CML-Link
THCV233	Single-In/Single-Out*2
THCV234	Dual-In/Selected Single-Out



*1 indicates micro-strip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)
*4 No HTPDN connection option. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)

Application Diagram (Case4)

Case4	High Speed CML-Link
THCV233	Single-In/Distributed Dual-Out
THCV234	Single-In/ Single-Out*2

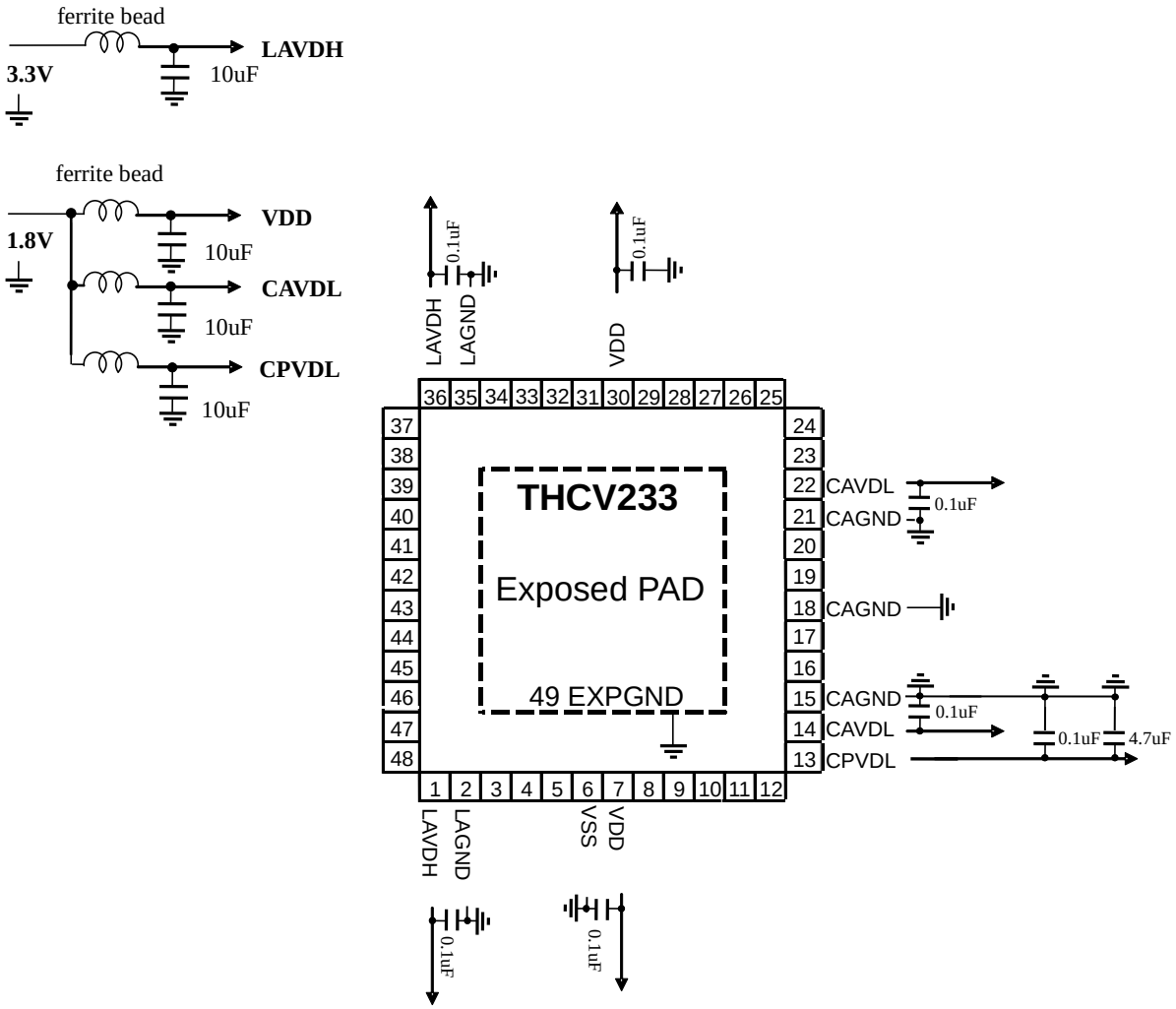


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)
*4 No HTPDN connection option. Please see the datasheet for details. (THCV233-234_Rev.x.xx_E.pdf)

Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 10nF or 0.1µF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible.
- Adding 4.7µF capacitors to PLL's power pins, along with the smaller bypass capacitors, is recommended.

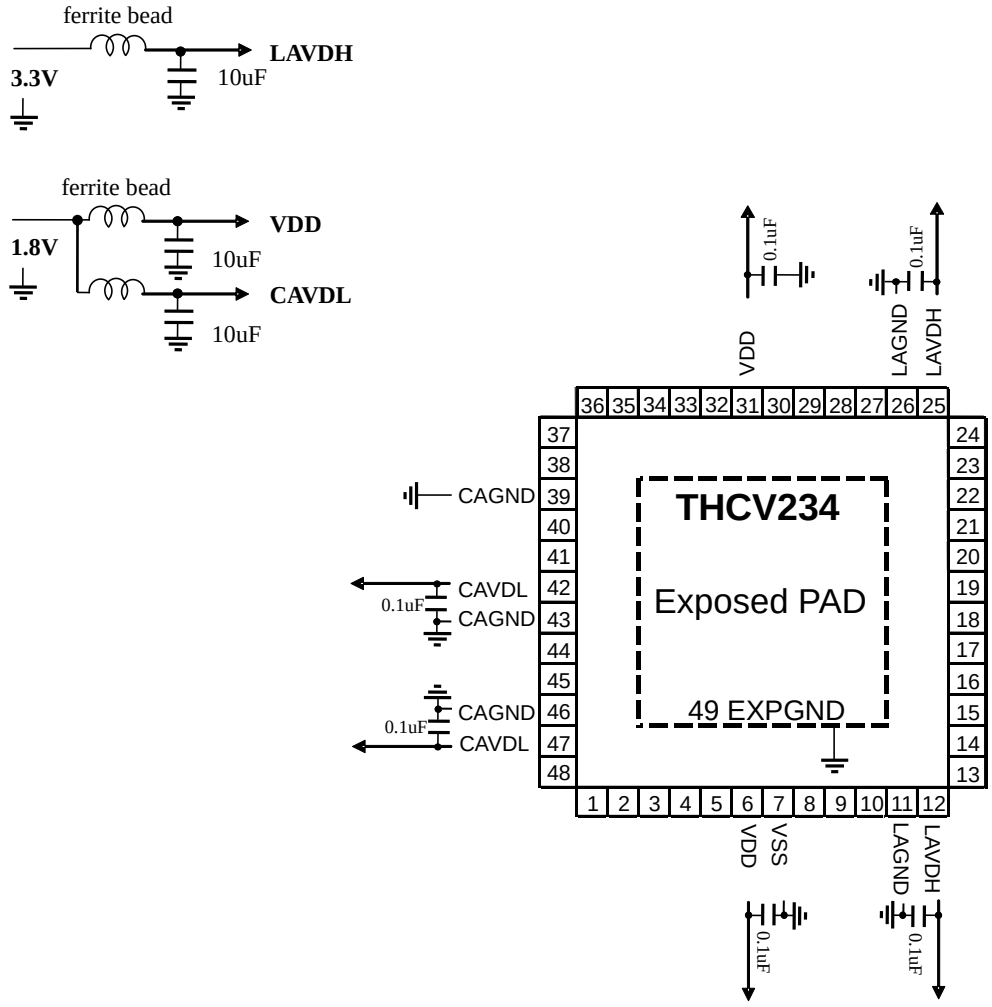
Recommended Power Supply for THCV233



Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 10nF or 0.1µF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible.

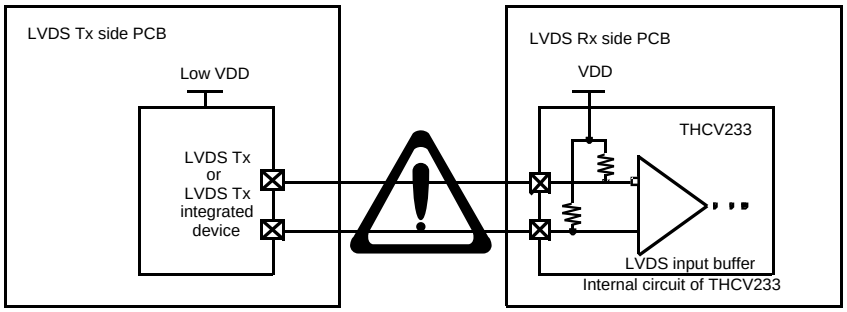
Recommended Power Supply for THCV234



Note

1)LVDS input pin connection

When LVDS line is not driven from the previous device, the line is pulled up to 3.3V internally in THCV233. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THCV233. One solution for this problem is PDN=L control during no LVDS input period because pull-up resistors are cut off at power down state.



2)Power On Sequence

Do not apply VDH before VDL. VDL and VDH can be applied at the same time.

3)Data Input Sequence

Don't input TLCLK+/- before THCV233 is on in order to keep absolute maximum ratings.

4)Cable Connection and Disconnection

Don't connect and disconnect the LVDS and CML cable, when the power is supplied to the system.

5)GND Connection

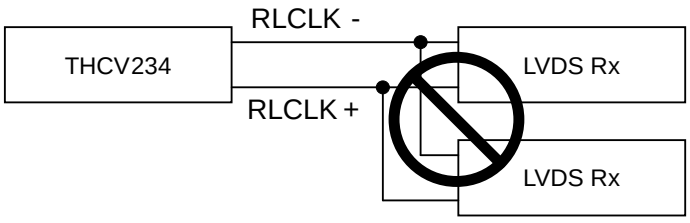
Connect the each GND of the PCB which Transmitter, Receiver and THCV233 on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

6) Low Input Pulse into PDN Period Requirement

Don't Input Low Pulse within 1msec into PDN.

7) Multi Drop Connection

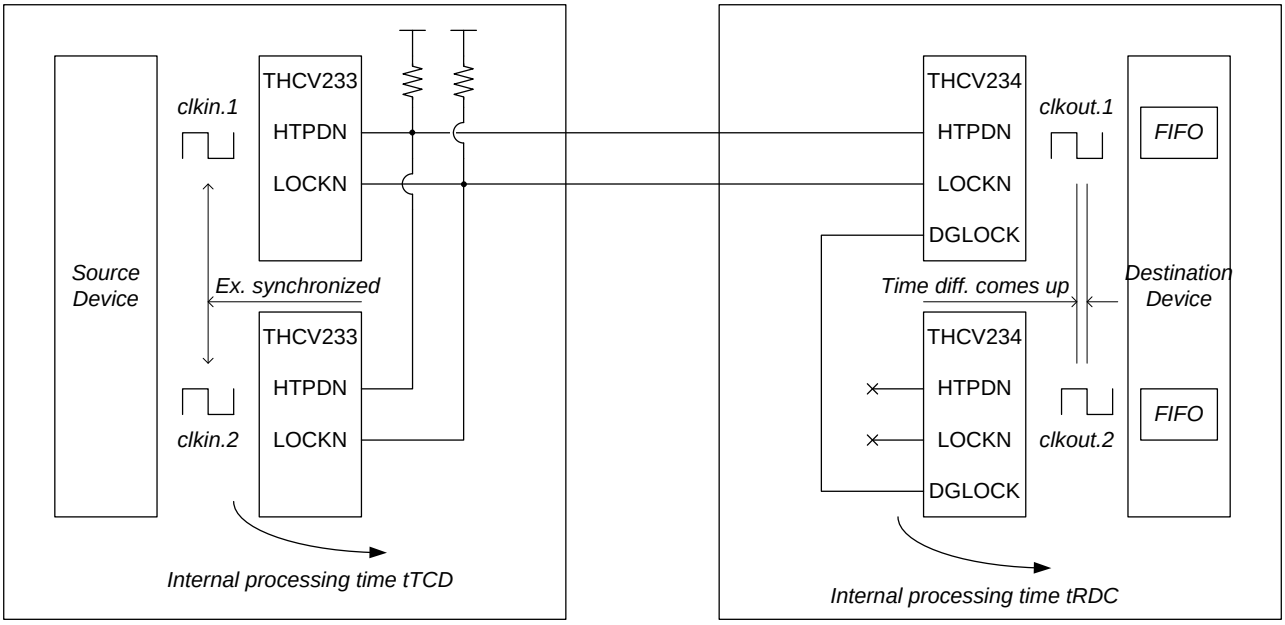
Multi drop connection is not recommended.



8)Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.
LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.
LOCKN of Tx side can be simply split to multiple Tx.
THCV234 DGLOCK connection is appropriate for multiple Rx use.

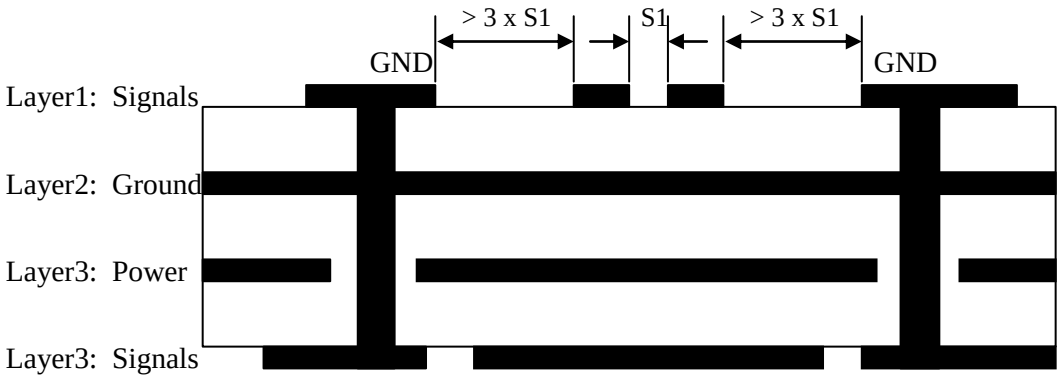
Also possible time difference of internal processing time (Data sheet THCV233 tTCD and THCV234 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV234, which may have internal FIFO.



PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

PCB Cross-sectional View
for Microstrip Lines



Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

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4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
   5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. (“THine”) accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
   5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.
sales@thine.co.jp