THCV226 Application Note

System Diagram and PCB Design Guideline

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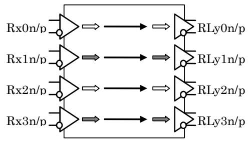
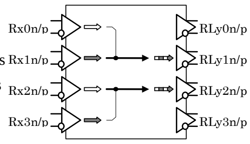
Normal LVDS Mode THCV226 V-by-One® HS 10bit Mode : up to 3.4Gbps 8bit Mode : up to 2.7Gbps  LVDS 10bit Mode : up to 85MHz 8bit Mode : up to 90MHz	**High-speed LVDS Mode** THCV226 V-by-One® HS 10bit Mode : up to 3.14Gbps 8bit Mode : up to 2.36Gbps  HSLVDS 10bit Mode : up to 157MHz 8bit Mode : up to 157MHz
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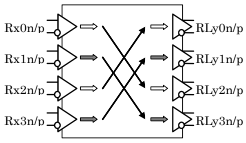
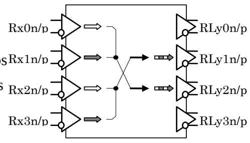
Normal LVDS with Crossing Mode THCV226 V-by-One® HS 10bit Mode : up to 3.4Gbps 8bit Mode : up to 2.7Gbps  LVDS 10bit Mode : up to 85MHz 8bit Mode : up to 90MHz	**High-speed LVDS with Crossing Mode** THCV226 V-by-One® HS 10bit Mode : up to 3.14Gbps 8bit Mode : up to 2.36Gbps  HSLVDS 10bit Mode : up to 157MHz 8bit Mode : up to 157MHz
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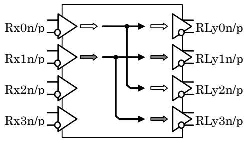
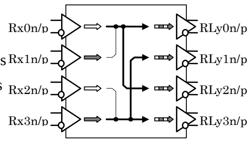
Normal LVDS with Distribution Mode 1 THCV226 V-by-One® HS 10bit Mode : up to 3.4Gbps 8bit Mode : up to 2.7Gbps  LVDS 10bit Mode : up to 85MHz 8bit Mode : up to 90MHz	**High-speed LVDS with Distribution Mode 1** THCV226 V-by-One® HS 10bit Mode : up to 3.14Gbps 8bit Mode : up to 2.36Gbps  HSLVDS 10bit Mode : up to 157MHz 8bit Mode : up to 157MHz
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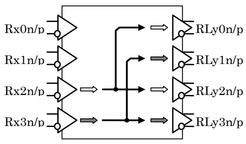
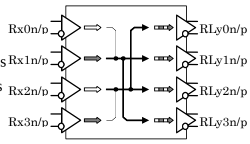
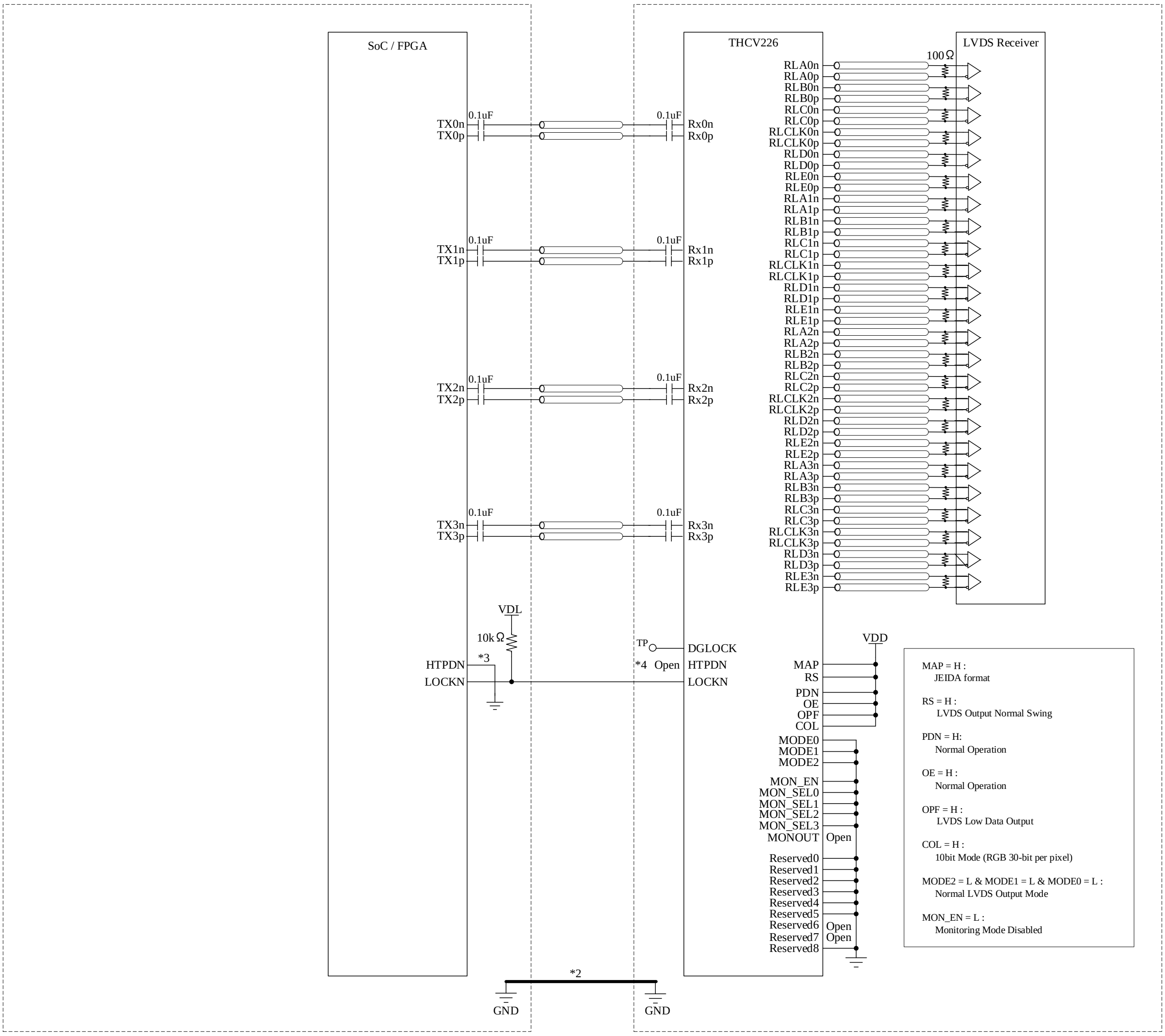
Normal LVDS with Distribution Mode 2 THCV226 V-by-One® HS 10bit Mode : up to 3.4Gbps 8bit Mode : up to 2.7Gbps  LVDS 10bit Mode : up to 85MHz 8bit Mode : up to 90MHz	**High-speed LVDS with Distribution Mode 2** THCV226 V-by-One® HS 10bit Mode : up to 3.14Gbps 8bit Mode : up to 2.36Gbps  HSLVDS 10bit Mode : up to 157MHz 8bit Mode : up to 157MHz

Application Diagram (Case1)

Normal LVDS Mode



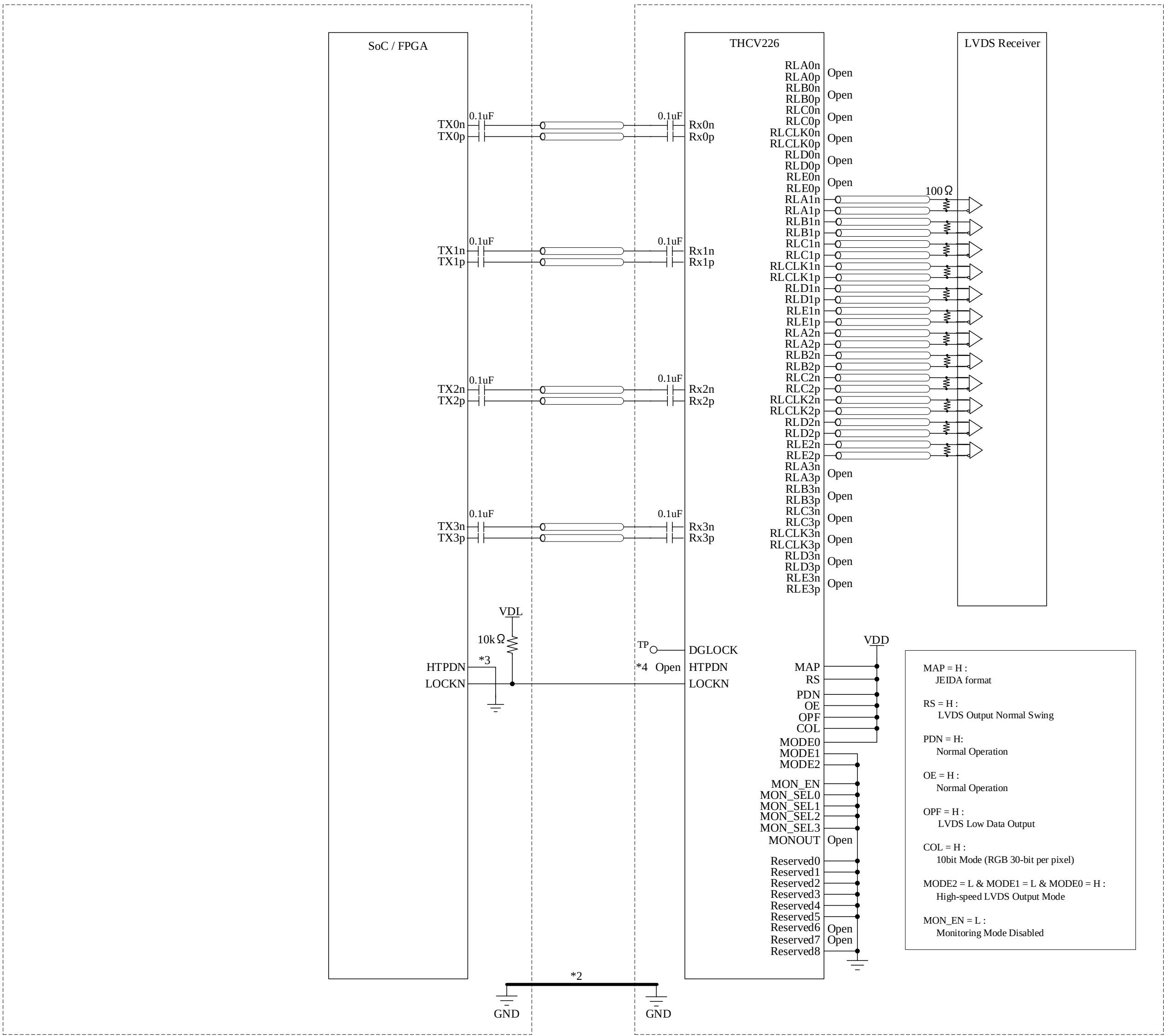
*1 [microstrip symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.

*2 Connect GNDs of both Tx and Rx PCB.

*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case2)

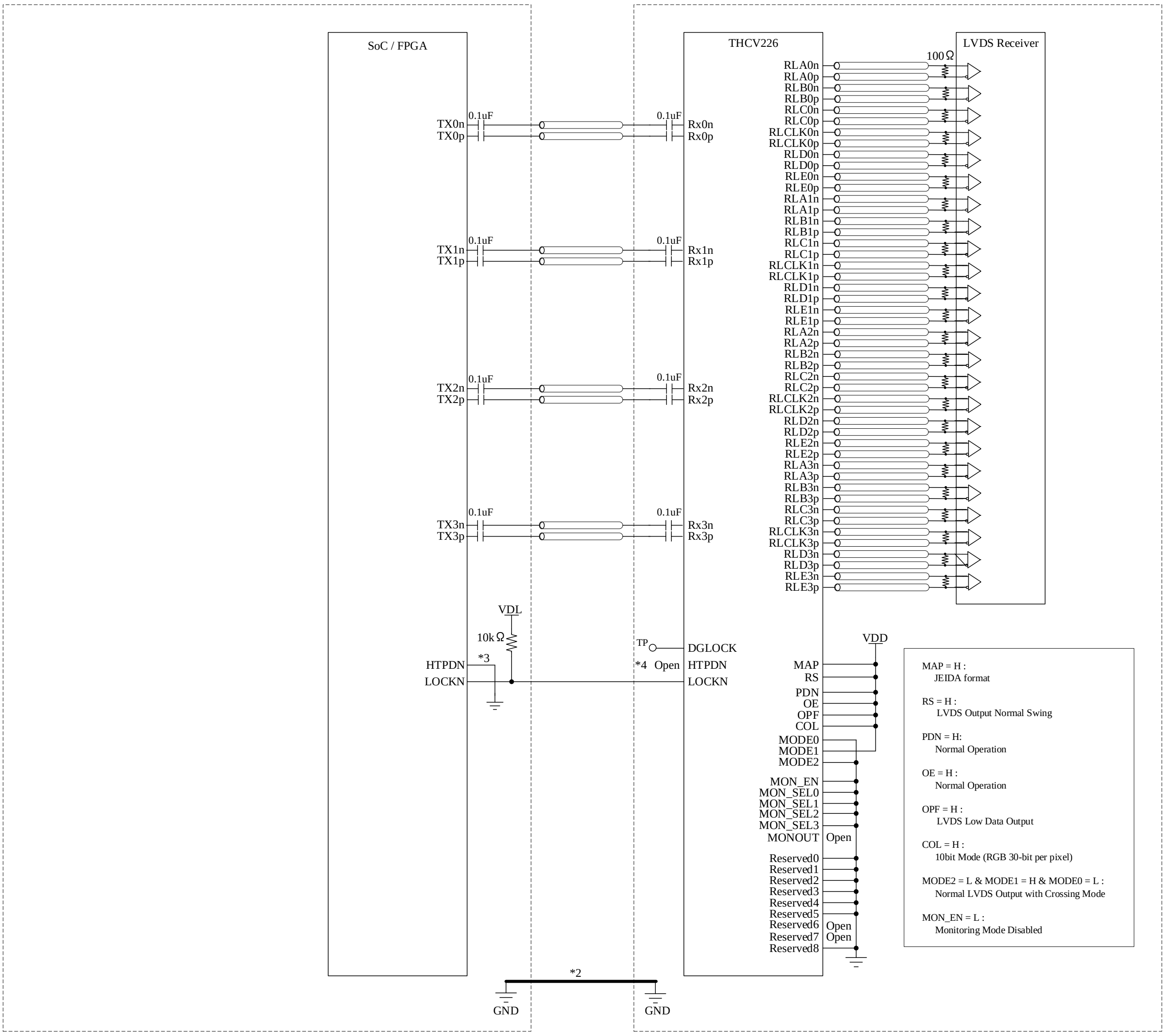
HSLVDS Mode



*1 [microstrip symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case3)

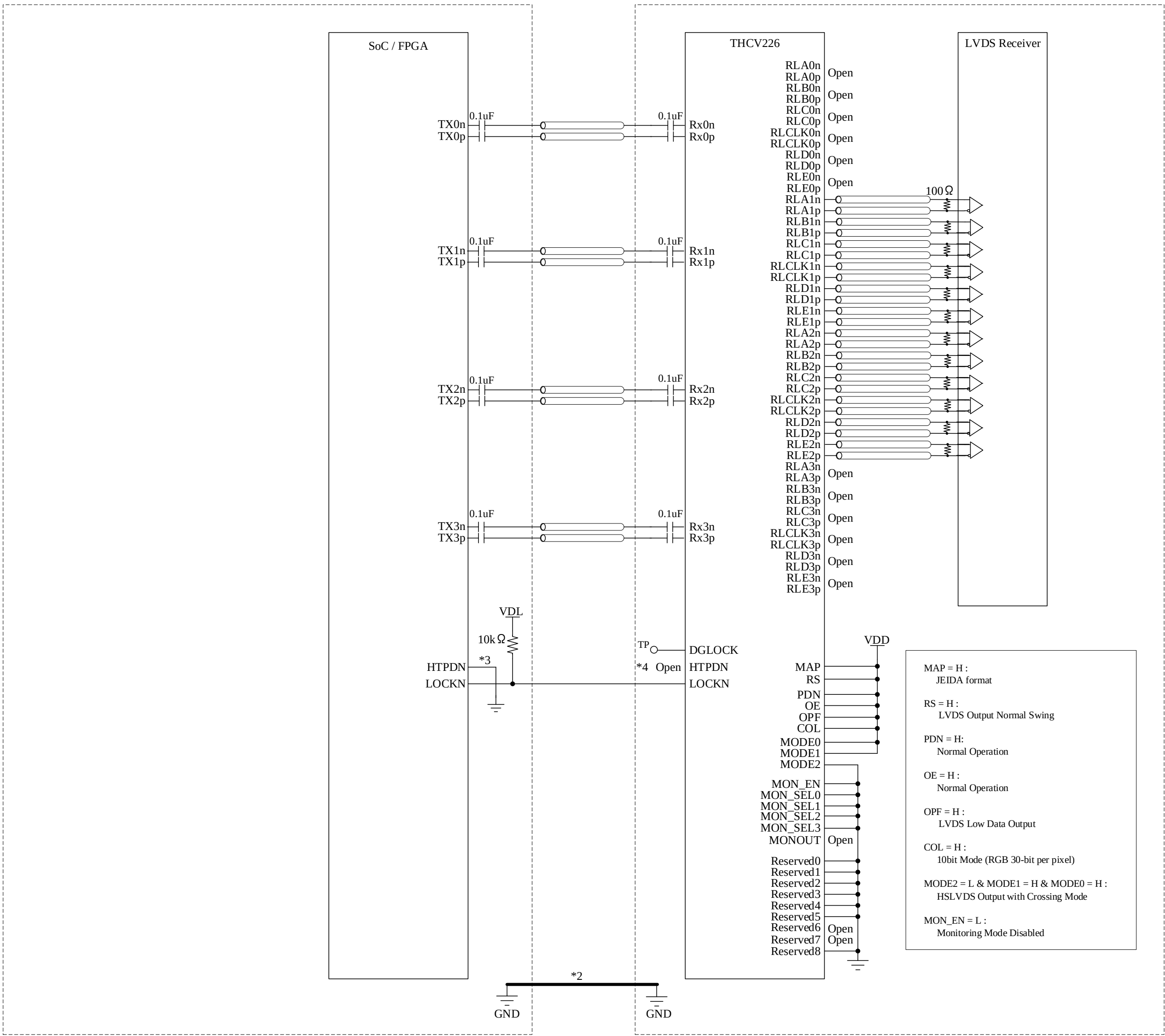
Normal LVDS with Crossing Mode



*1 [microstrip symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case4)

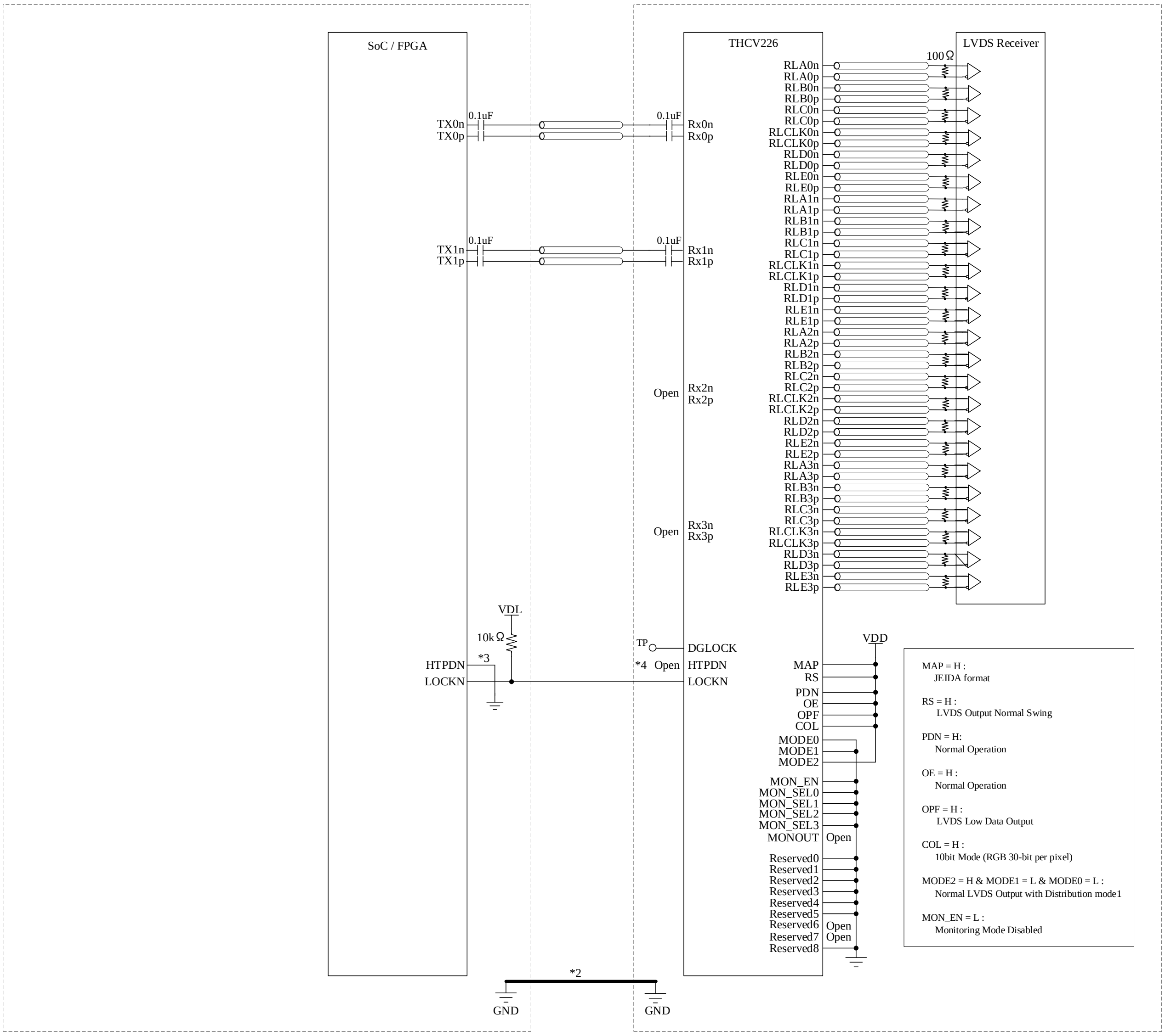
HSLVDS with Crossing Mode



*1 [symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case5)

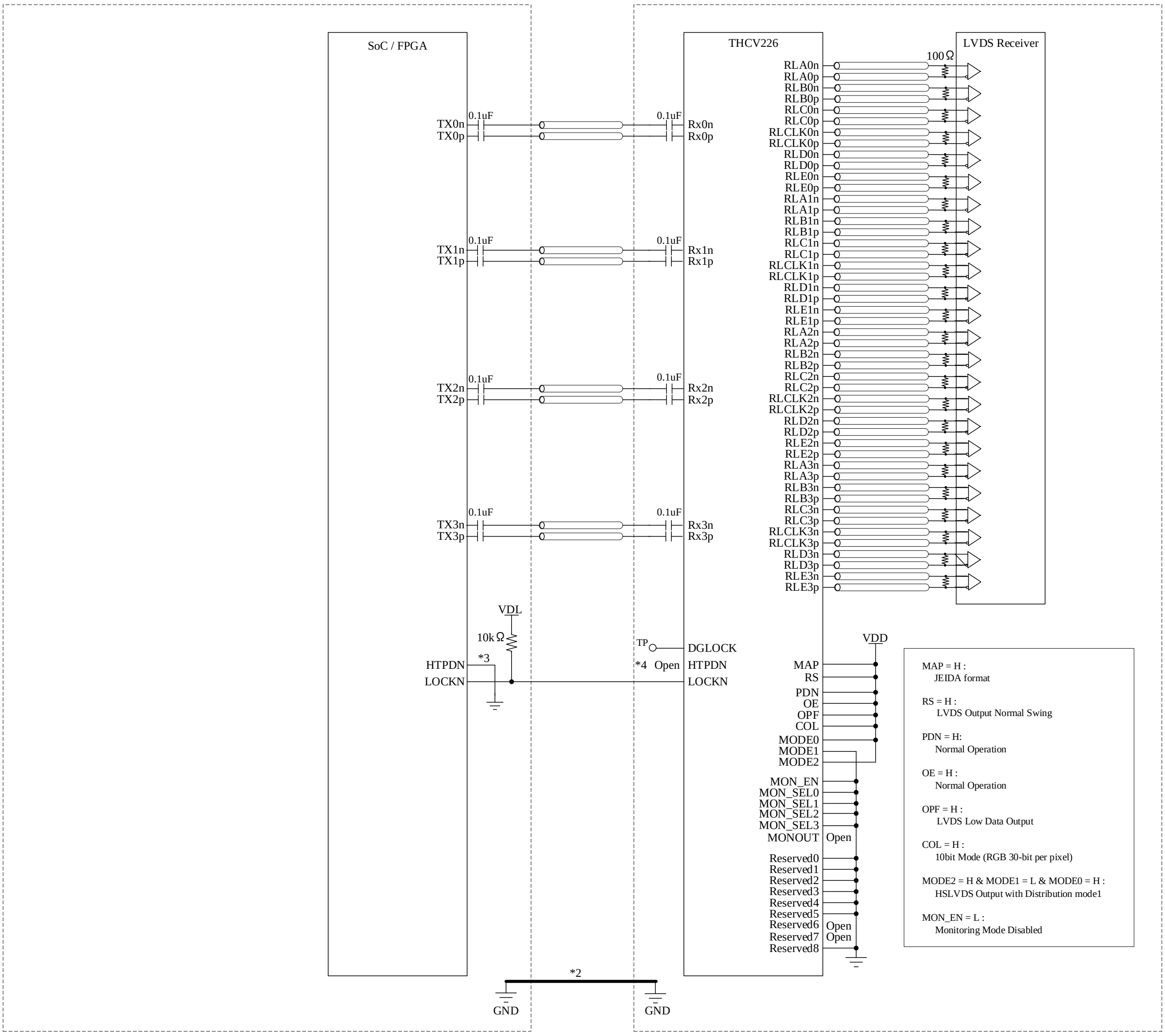
Normal LVDS with Distribution Mode 1



*1 [symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case6)

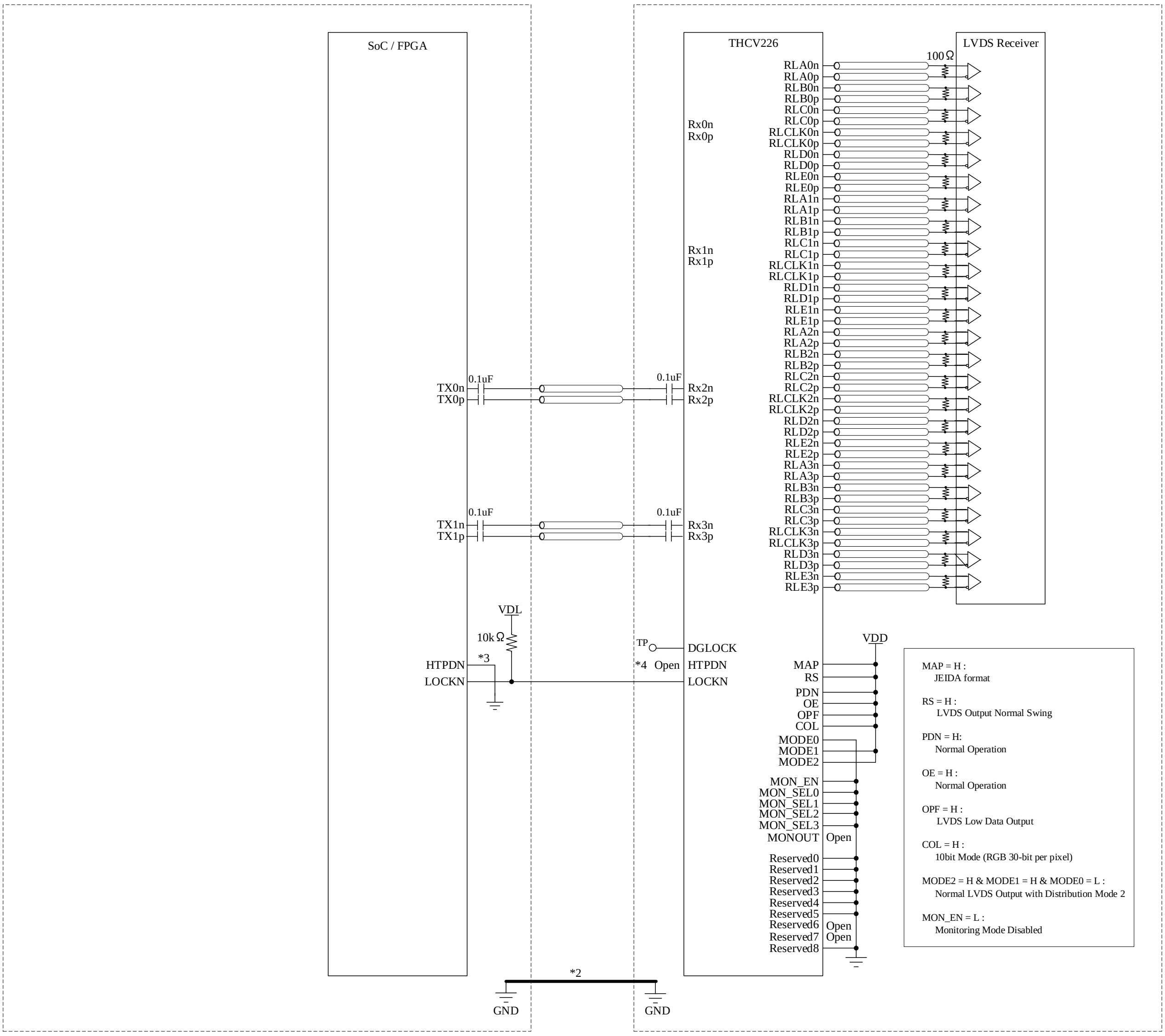
HSLVDS with Distribution Mode 1



*1 [symbol] indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case7)

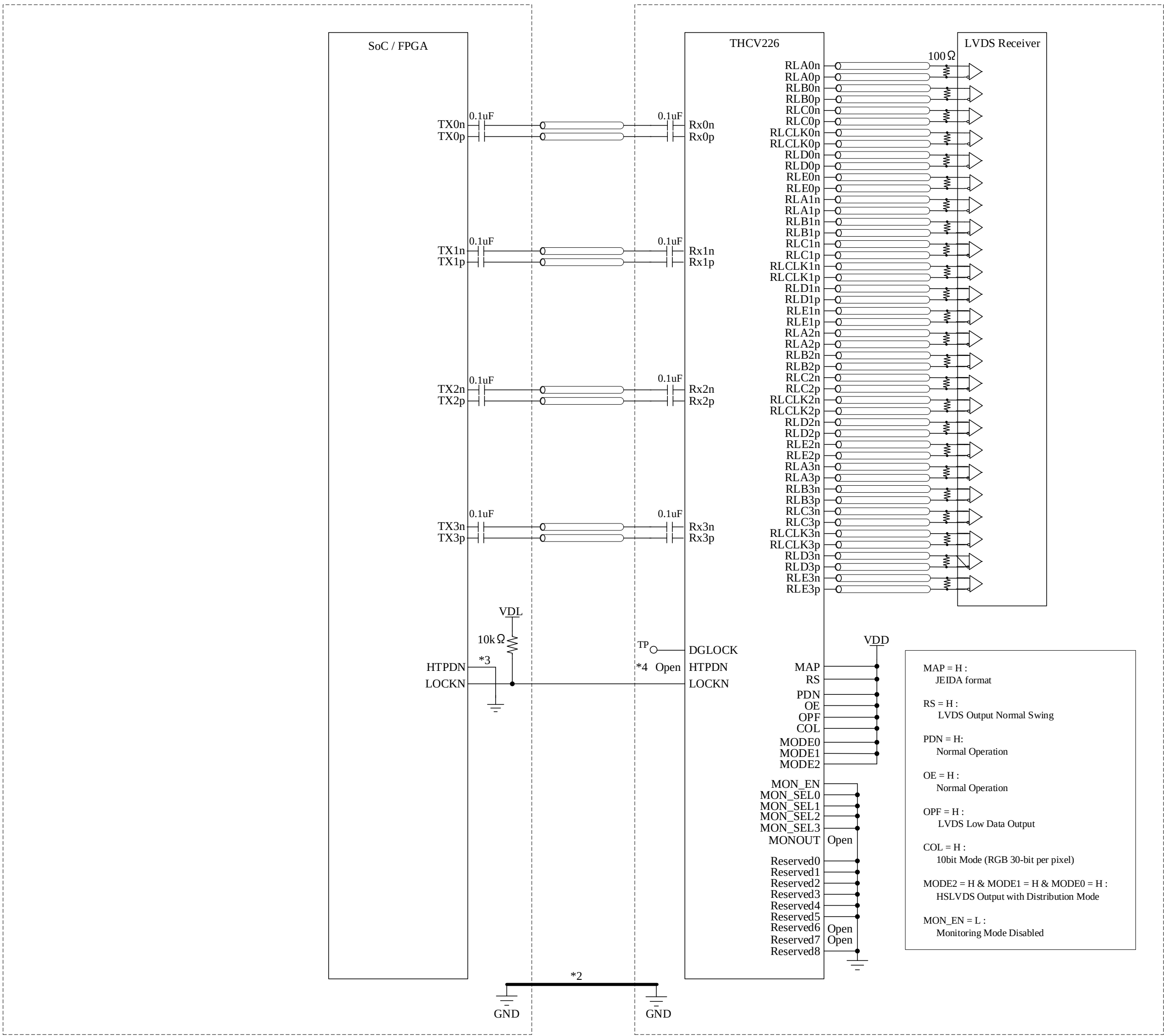
Normal LVDS with Distribution Mode 2



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Application Diagram (Case8)

HSLVDS with Distribution Mode 2

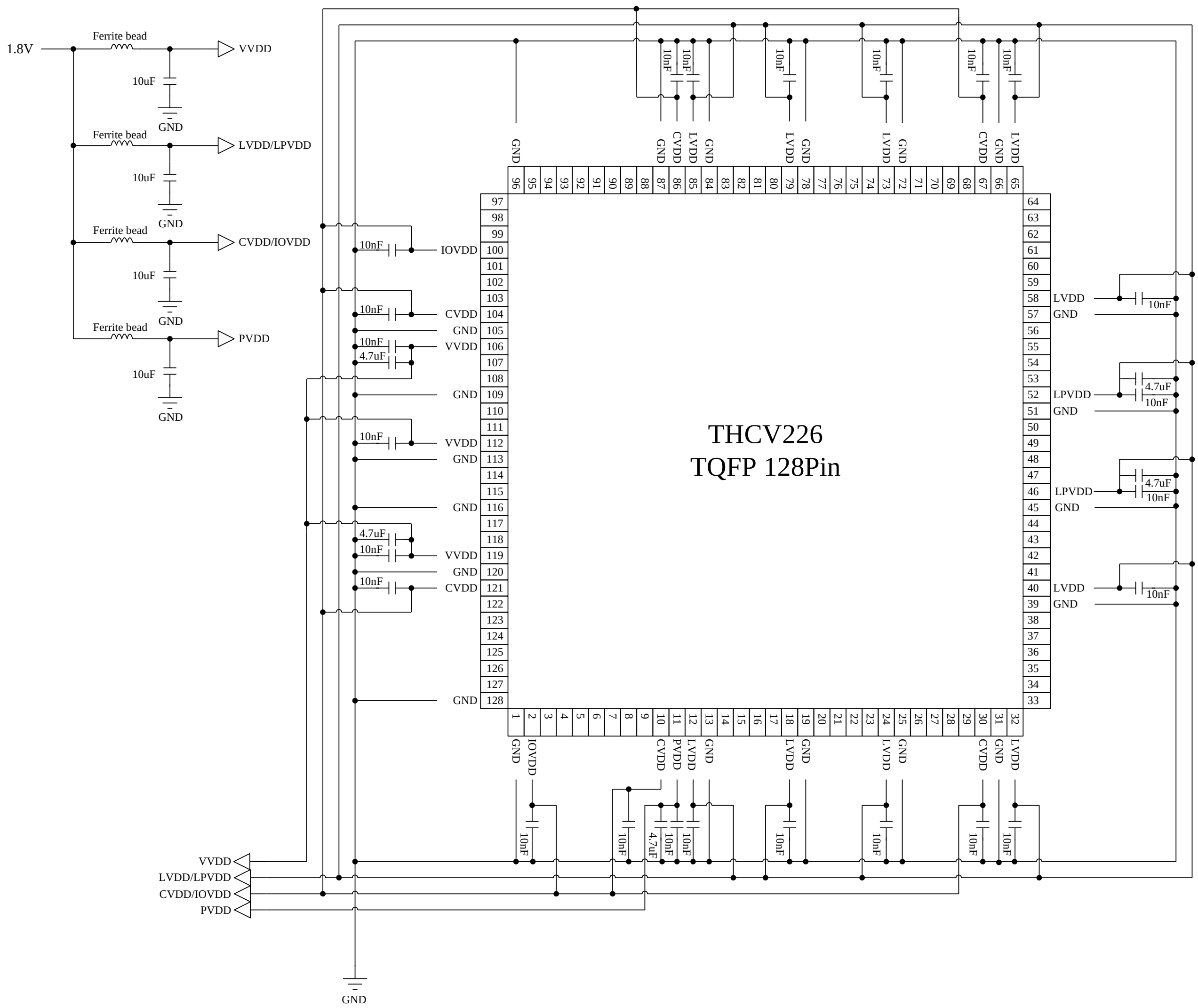


*1 (symbol) indicates microstrip lines or cables with their differential characteristic impedance being 100Ω.
*2 Connect GNDs of both Tx and Rx PCB.
*3 No HTPDN connection option. Please refer to the datasheet for details.

Recommendations for Power Supply

- Separate the power domains into VVDD, LVDD(/LPVDD), CVDD(/IOVDD), and PVDD in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 10nF or 0.1μF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible.
- Adding 4.7μF capacitors to PLL's power pins including V-by-One® HS power domain, along with the smaller bypass capacitors, is recommended.

Recommended Power Supply for THCV226

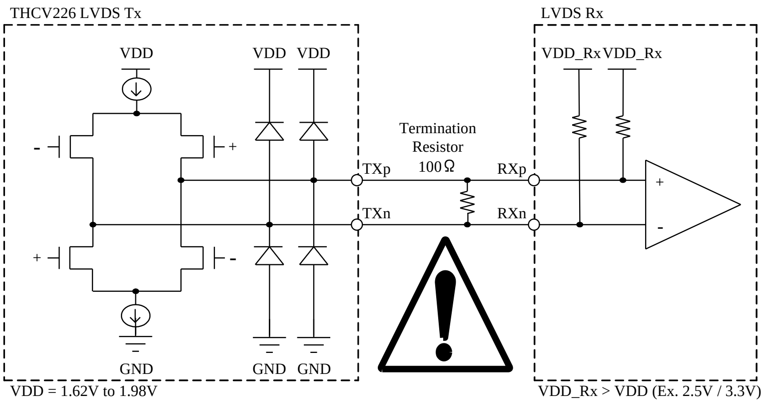


Note

1) LVDS Output Pin Connection

In case that the LVDS Rx of destination device is equipped with pull-up resistors connected to higher than THCV226's VDD voltage, this can cause violation of absolute maximum ratings to THCV226. This phenomenon may be happened at power-on phase and Hi-Z state of the whole system including LVDS Rx device.

One solution for this problem is power-down control for LVDS Rx device during no LVDS input or Hi-Z state period, if its pull-up resistors can be cut off at power-down state. Another solution is to set THCV226's OPF option pin to VDD. This setting provides low fixed data output mode at PDN = H, not Hi-Z state mode.



2) Cable Connection and Disconnection

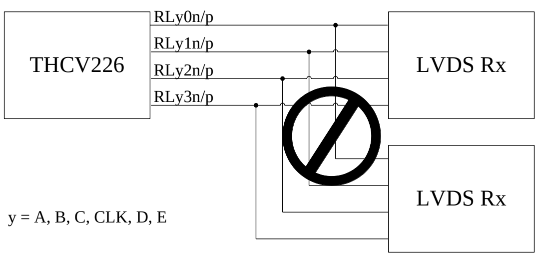
Do Not connect and disconnect the LVDS and CML cable, when the power is supplied to the system.

3) GND Connection

Connect the each GND of the PCB which Transmitter and THCV226 on it. It is better for EMI reduction to place GND cable as close to LVDS and CML cable as possible.

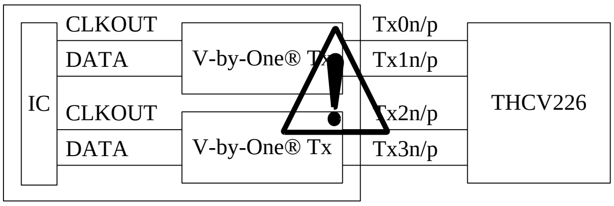
4) Multi-drop Connection

Multi-drop connection is not recommended.



5) Multiple Counterpart Use

Multiple counterpart use such as the following system is not recommended. If it is not avoidable, please check whether tRISK and tRIJT spec of THCV226 can be kept or not.

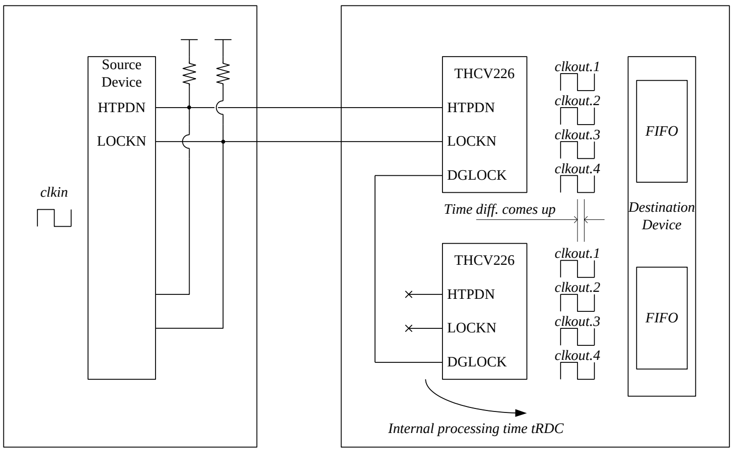


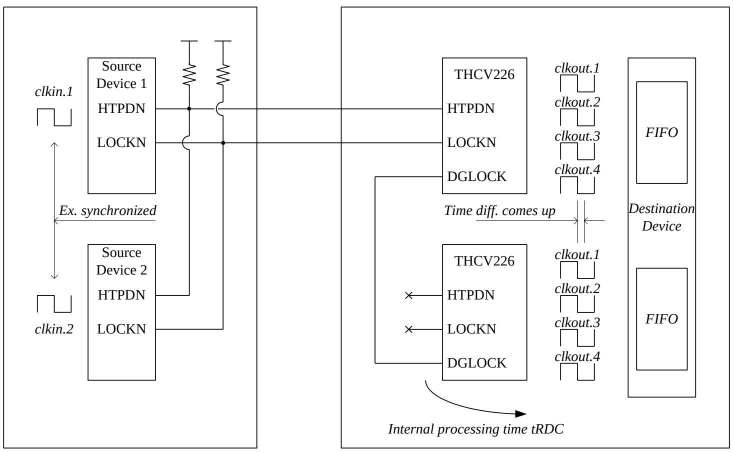
6) Multiple Device Connection

HTPDN and LOCKN signals are supposed to be connected properly for their purpose like the following figure.

HTPDN should be from just one THCV226 to multiple Tx devices because its purpose is only ignition of all Tx devices. LOCKN should be connected so as to indicate that CDR status of all Rx devices becomes ready to receive normal operation data. LOCKN of Tx side can be simply split to multiple Tx devices. THCV226's DGLOCK is appropriate for multiple Rx use.

Also possible time difference of internal processing time (THCV226 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV226 chips, which may have internal FIFO.

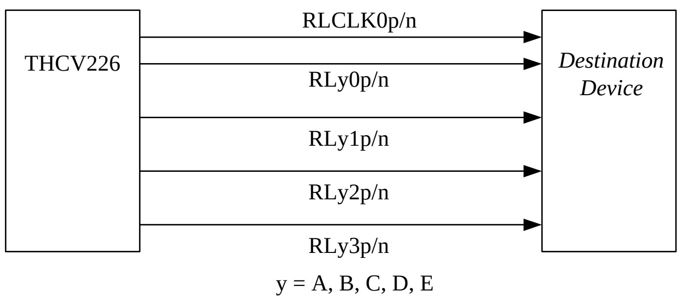


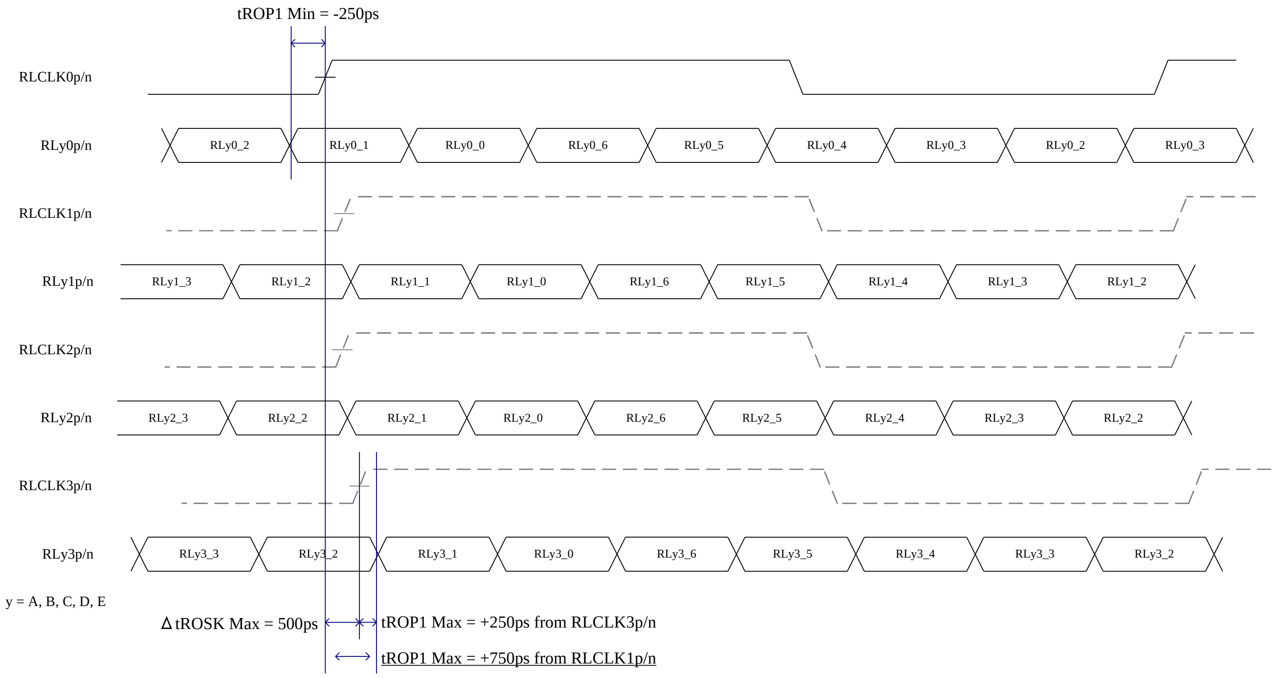


7) LVDS Link Skew Consideration
Single Chip Case in use of Only One Clock Signal out of LVDS Channels :

Let tRCOP = 13.47ns (74.25MHz) at normal LVDS mode.

As a result, the total amount of LVDS skew, tROP1, is calculated as +/- 750ps in use of only one clock signal out of LVDS channels for the connection between THCV226 and destination device.

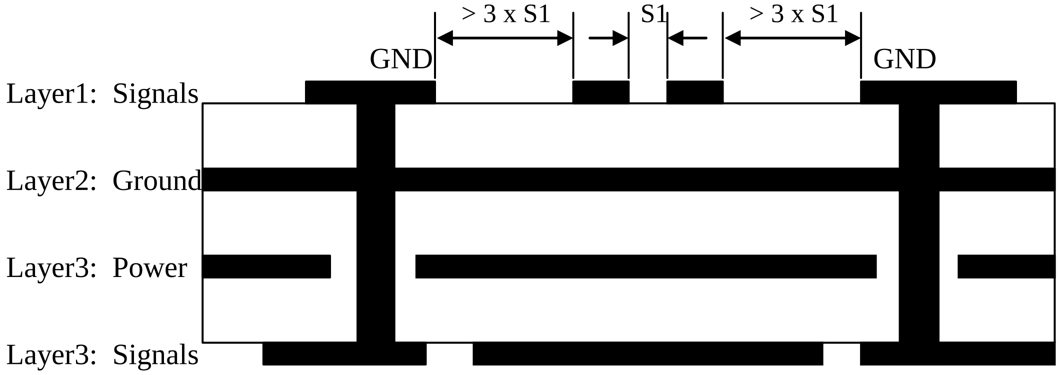




PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables, also causes reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

PCB Cross-sectional View
for Microstrip Lines



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