Application Note	*THAN0089_Rev.1.60_E*

THCV217/THCV218 Application Note

System Diagram and PCB Design Guideline

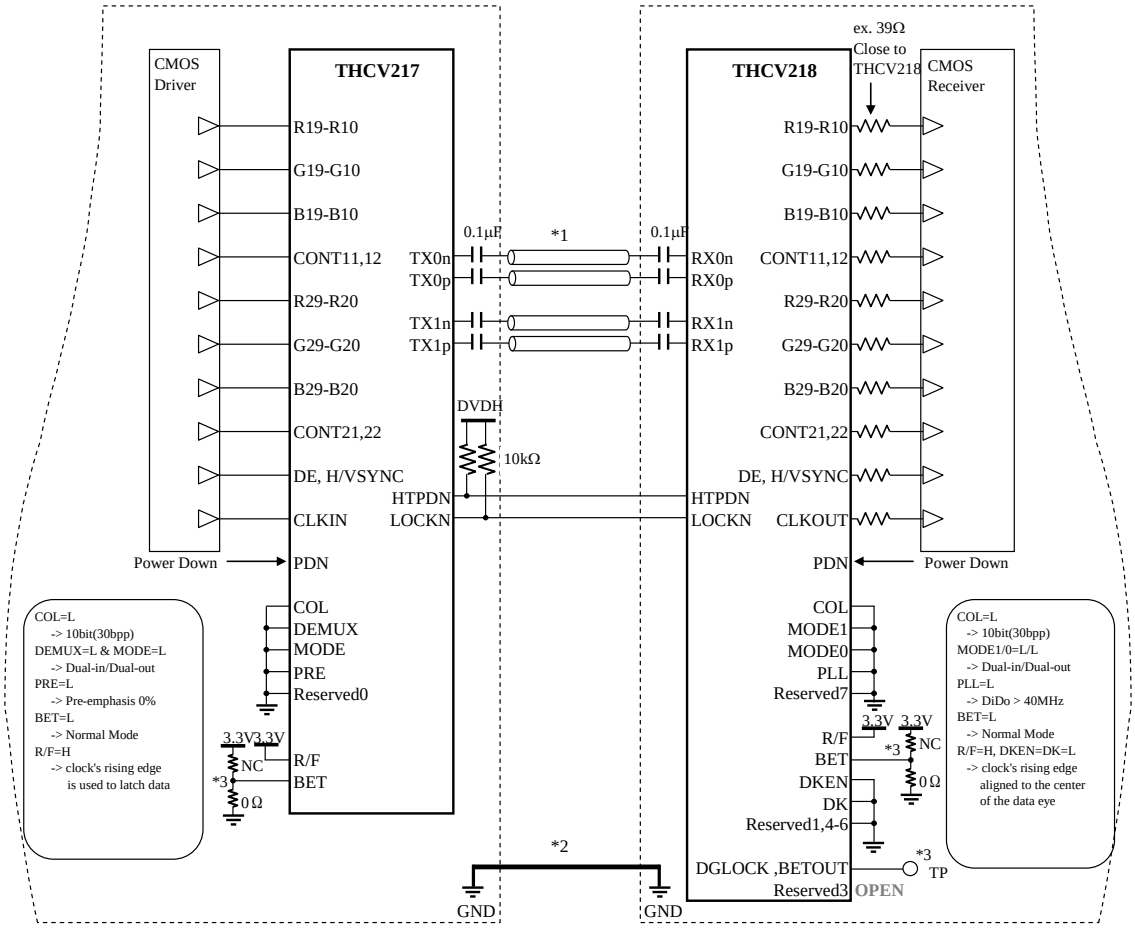
Contents

Application Diagrams

Dual-in/Dual-out, 10bit (30bit per pixel) without Pre-emphasis

[THCV217]
Set the COL pin **LOW** to place the chip in the 10 bit operation mode.
Set the DEMUX pin **LOW** and MODE pin **LOW** for the Dual-in/Dual-out operation mode.
Set the PRE pin **LOW** when pre-emphasis is not needed.
Set the BET pin **LOW** for the normal operation.
Set reserved pin accordingly.

[THCV218]
Set the COL pin **LOW** to place the chip in the 10 bit operation mode.
Set the MODE1 pin **LOW** and MODE0 pin **LOW** for the Dual-in/Dual-out operation mode.
Set the PLL **LOW** when the pixel clock rate is above 40MHz.
Set the BET pin **LOW** for the normal operation.
Set reserved pins accordingly.
Place damping resistors close to data output pins to reduce unwanted ringing or reflection.

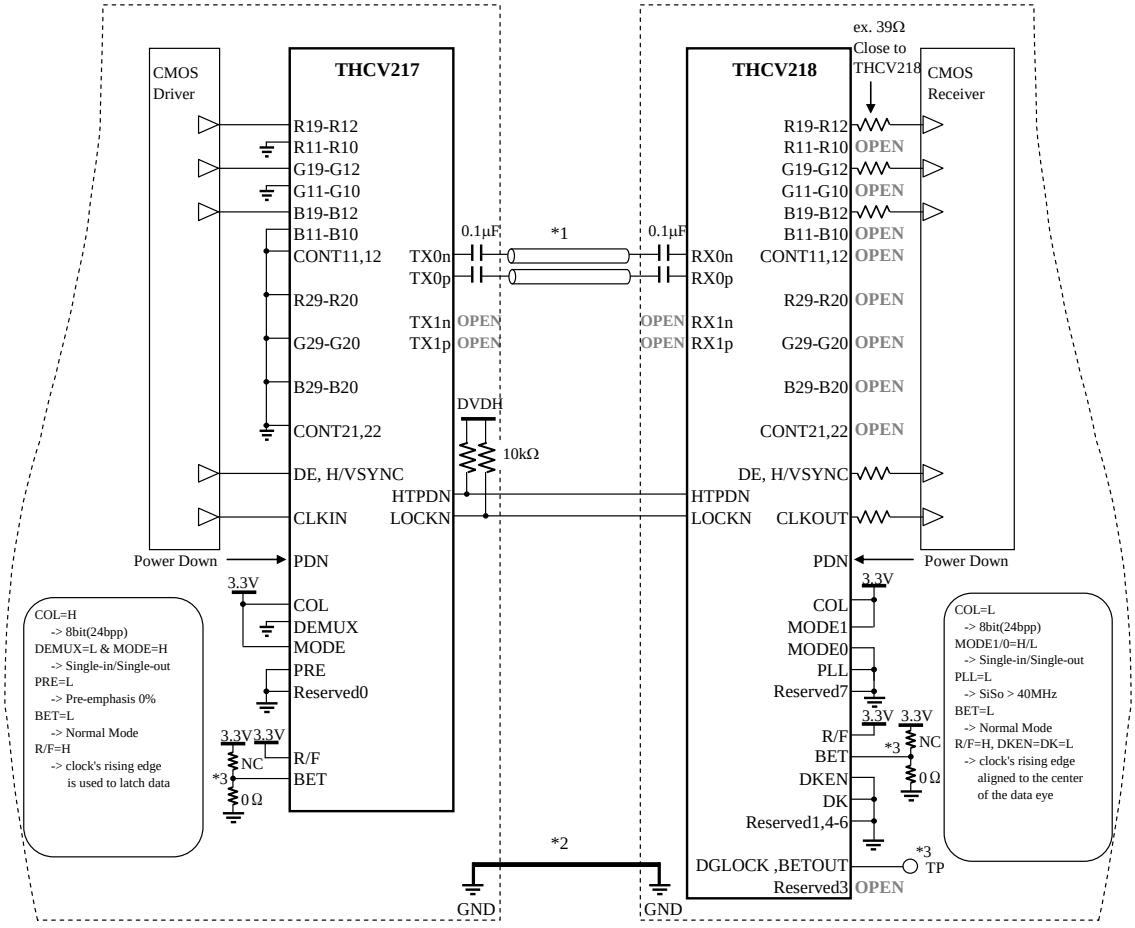


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV217-218_Rev.x.xx_E.pdf)

Single-in/Single-out, 8bit (24bit per pixel) without Pre-emphasis

[THCV217]
Set the COL pin **HIGH** to place the chip in the 8 bit operation mode.
Set the DEMUX pin **LOW** and MODE pin **HIGH** for the Single-in/Single-out operation mode.
Set the PRE pin **LOW** when pre-emphasis is not needed.
Set the BET pin **LOW** for the normal operation.
Set reserved pin accordingly.

[THCV218]
Set the COL pin **HIGH** to place the chip in the 8 bit operation mode.
Set the MODE1 pin **HIGH** and MODE0 pin **LOW** for the Single-in/Single-out operation mode.
Set the PLL **LOW** when the pixel clock rate is above 40MHz.
Set the BET pin **LOW** for the normal operation.
Set reserved pins accordingly.
Place damping resistors close to data output pins to reduce unwanted ringing or reflection.

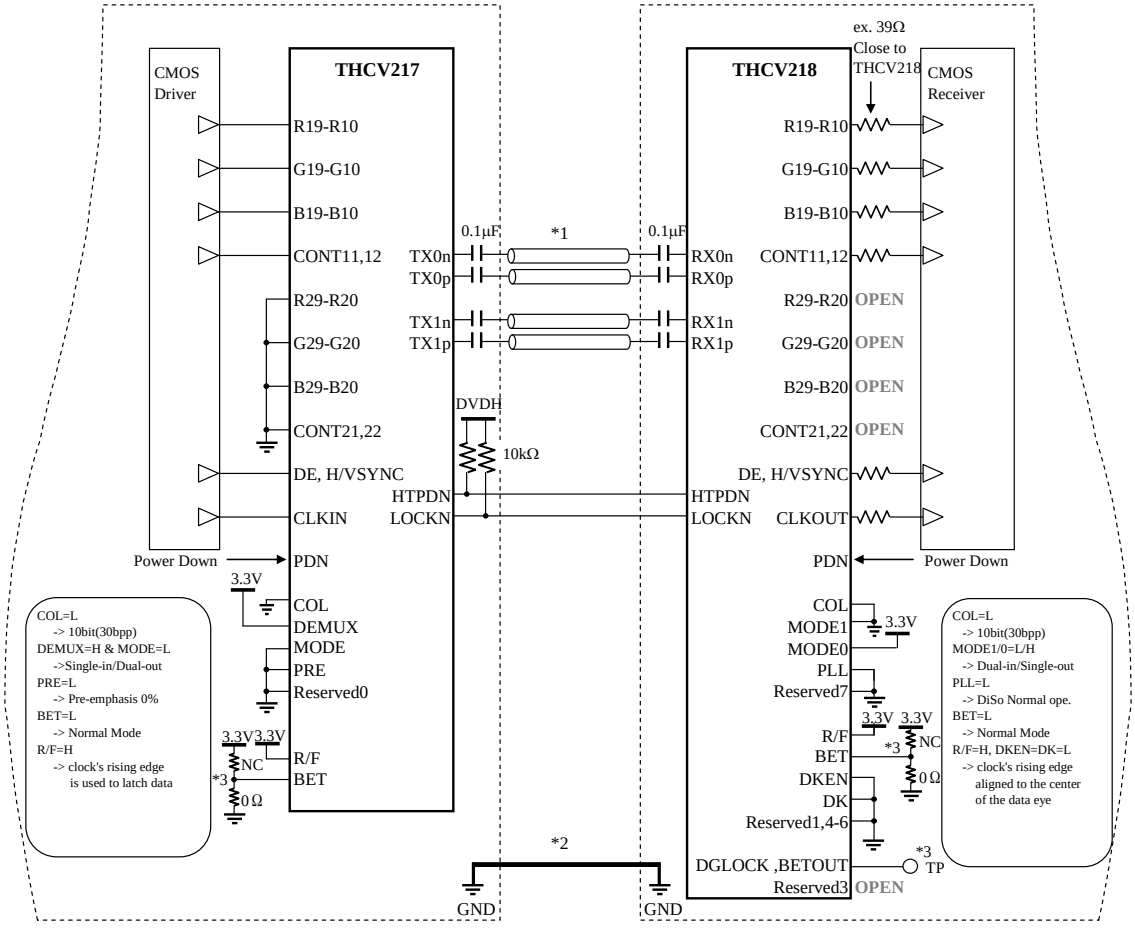


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV217-218_Rev.x.xx_E.pdf)

Single-in/Dual-out to Dual-in/Single-out, 10bit (30bit per pixel) without Pre-emphasis

[THCV217]
Set the COL pin **LOW** to place the chip in the 10 bit operation mode
Set the DEMUX pin **HIGH** and MODE pin **LOW** for the Single-in/Dual-out operation mode.
Set the PRE pin **LOW** when pre-emphasis is not needed.
Set the BET pin **LOW** for the normal operation.
Set reserved pin accordingly.

[THCV218]
Set the COL pin **LOW** to place the chip in the 10 bit operation mode
Set the MODE1 pin **LOW** and MODE0 pin **HIGH** for the Dual-in/Single-out operation mode.
Set the PLL **LOW** for any clock rate for the Dual-in/Single-out mode.
Set the BET pin **LOW** for the normal operation.
Set reserved pins accordingly.
Place damping resistors close to data output pins to reduce unwanted ringing or reflection.



*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV217-218_Rev.x.xx_E.pdf)

CCIR 601/656, 8bit and HS/VS camera image over 100MHz with only two pair, meters distance

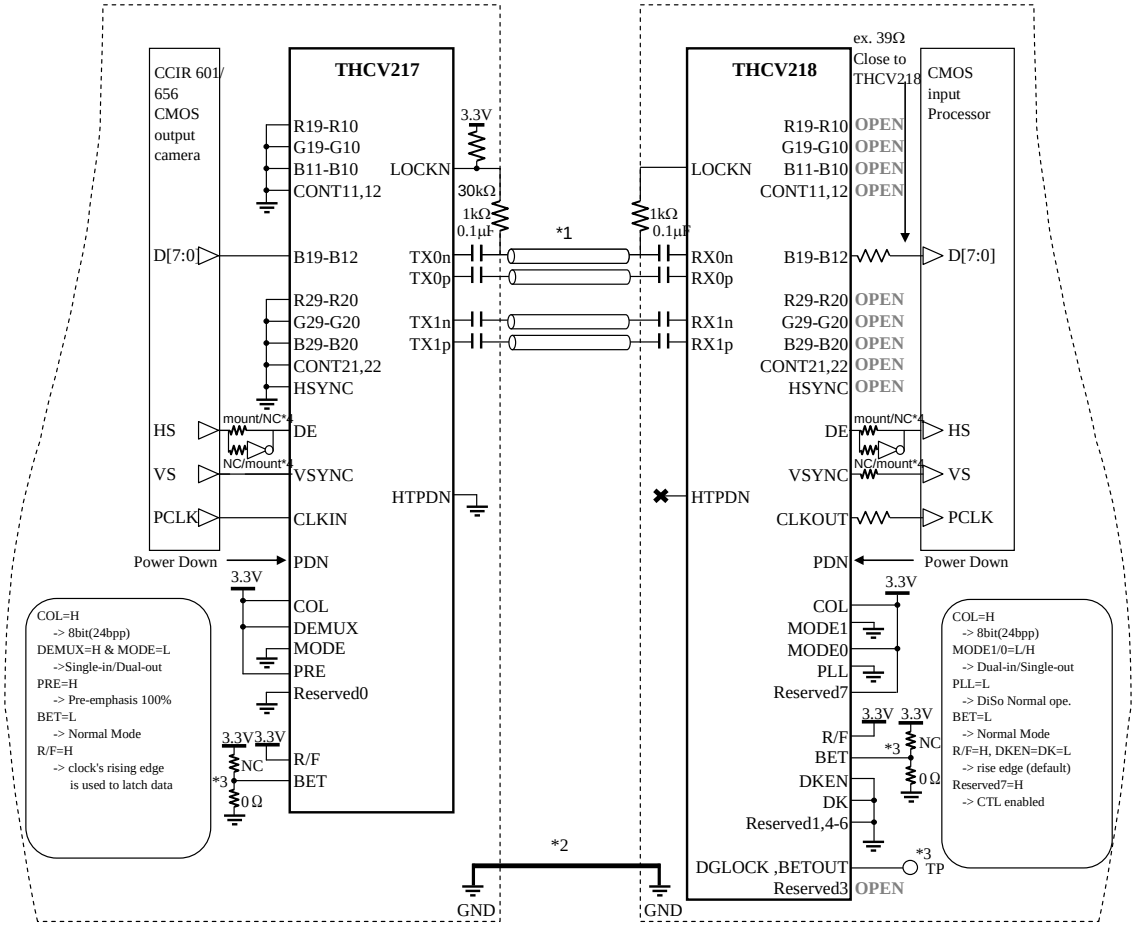
THCV217 HTPDN is tied to GND. LOCKN can be shared with V-by-One® HS trace via two 1kohm. Camera HSYNC should be connected THCV217-218 DE and polarity must be cared properly outside.

[THCV217]

Set the COL pin **HIGH** to place the chip in the 8 bit operation mode. It helps long distance transmission.
Set the DEMUX pin **HIGH** and MODE pin **LOW** for the Single-in/Dual-out operation mode.
Set the PRE pin **HIGH** because pre-emphasis is usually needed over meters long distance transmission.
Set the BET pin **LOW** for the normal operation.
Remind if the RF pin setting matches to the system. Set reserved pin accordingly.

[THCV218]

Set the COL pin **HIGH** to place the chip in the 8bit operation mode. It helps long distance transmission.
Set the MODE1 pin **LOW** and MODE0 pin **HIGH** for the Dual-in/Single-out operation mode.
Set the PLL **LOW** for any clock rate for the Dual-in/Single-out mode.
Set the BET pin **LOW** for the normal operation.
Remind if the RF pin setting matches to the system. Set reserved pins accordingly. Place damping resistors.

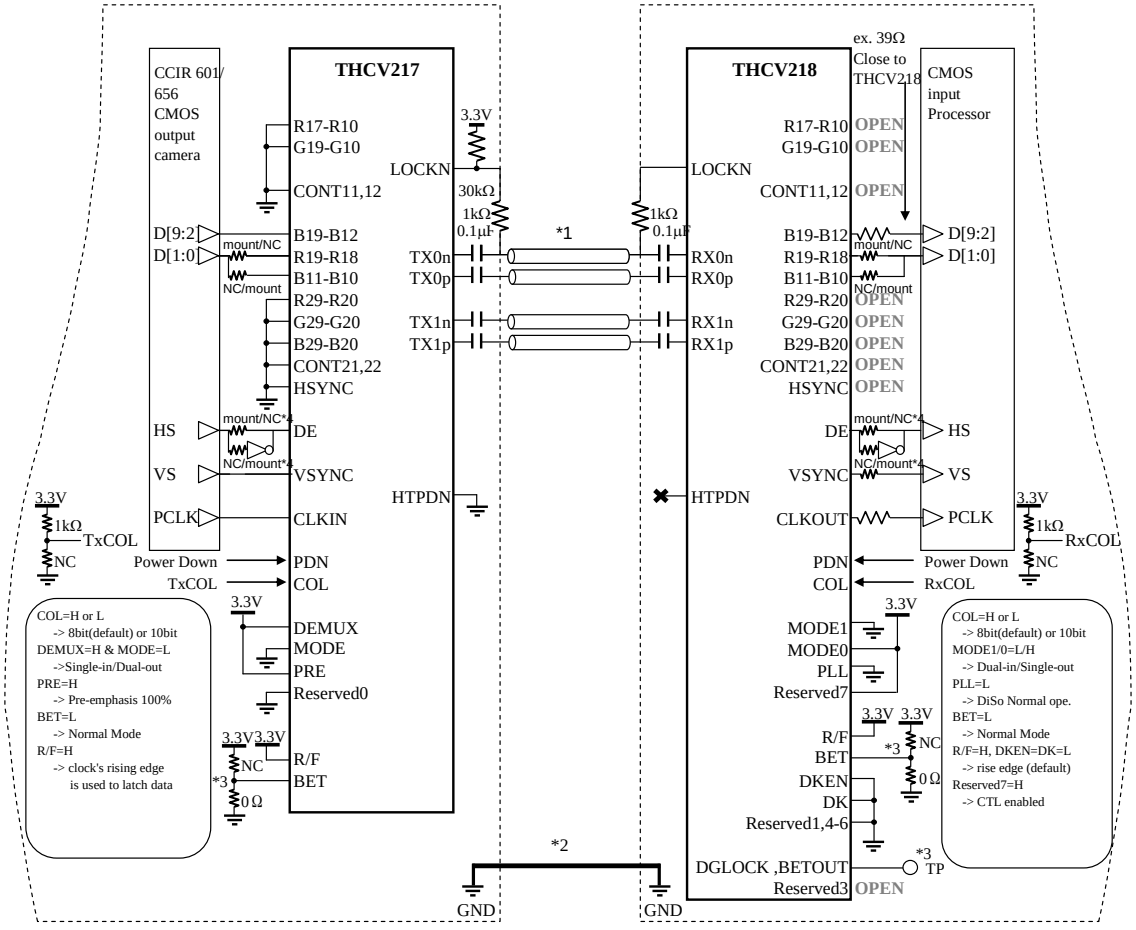


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV217-218_Rev.x.xx_E.pdf)
*4 System HSYNC signal should be matched to Vx1HS DE requirement. Active image should be during DE=H

CCIR 601/656, 10bit and HS/VS camera image over 100MHz with only two pair, meters distance

THCV217 HTPDN is tied to GND. LOCKN can be shared with V-by-One® HS trace via two 1kohm.
Camera HSYNC should be connected THCV217-218 DE and polarity must be cared properly outside.

10 bit least significant two bits are allocated to R19-R18 (default) and B11-B10 (CTL packet in 10 bit mode).
8 bit mode is recommended for long distance transmission; however, sometimes CTL in 10 bit mode are needed.
[THCV217]
Set the COL pin **HIGH** to place the chip in the 8 bit operation mode. If needed, change it to 10bit mode.
Set the DEMUX pin **HIGH** and MODE pin **LOW** for the Single-in/Dual-out operation mode.
Set the PRE pin **HIGH** because pre-emphasis is usually needed over meters long distance transmission.
Remind if the RF pin setting matches to the system. Set reserved pin accordingly.
[THCV218]
Set the COL pin **HIGH** to place the chip in the 8bit operation mode. If needed, change it to 10bit mode.
Set the MODE1 pin **LOW** and MODE0 pin **HIGH** for the Dual-in/Single-out operation mode.
Set the PLL **LOW** for any clock rate for the Dual-in/Single-out mode.
Remind if the RF pin setting matches to the system. Set reserved pins accordingly. Place damping resistors.

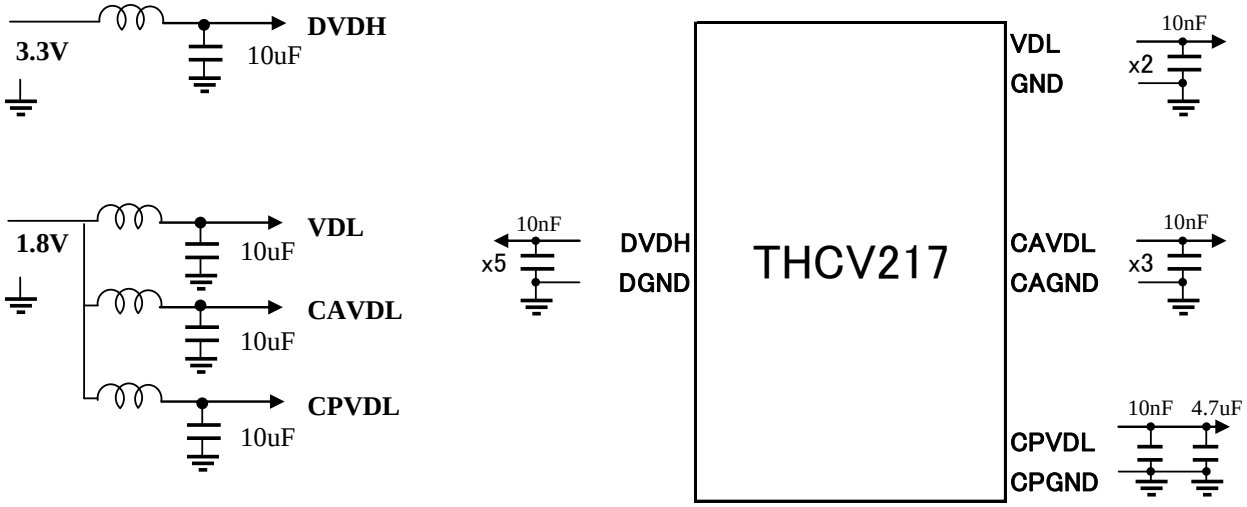


*1 indicates microstrip lines or cables with their differential characteristic impedance being 100Ω
*2 Connect GNDs of both Tx and Rx PCB
*3 Field BET Operation. Please see the datasheet for details. (THCV217-218_Rev.x.xx_E.pdf)
*4 System HSYNC signal should be matched to Vx1HS DE requirement. Active image should be during DE=H

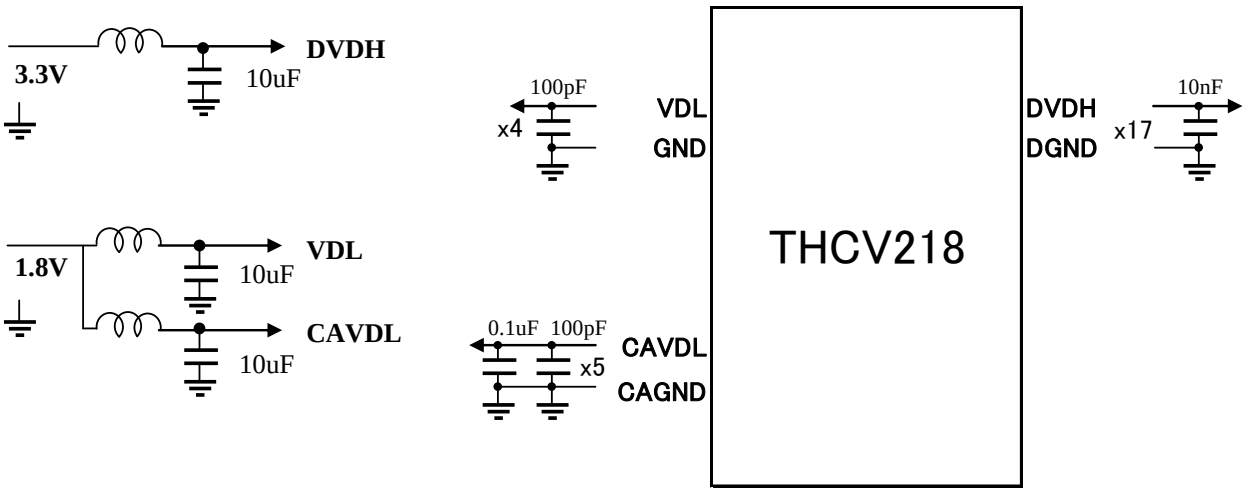
Recommendations for Power Supply

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 100pF or 10nF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. 100pF capacitors, along with 0.1uF capacitors, are recommended for 218's CAVDL.
- Adding 4.7μF capacitors to PLL's power pins, along with the smaller bypass capacitors, is recommended.
- Use the same ground plane for all ground pins.

Recommended Power Supply for THCV217



Recommended Power Supply for THCV218



Note

1)Cable Connection and Disconnection

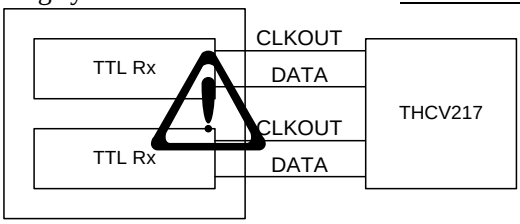
Don't connect and disconnect the LVDS and CML cable, when the power is supplied to the system.

2)GND Connection

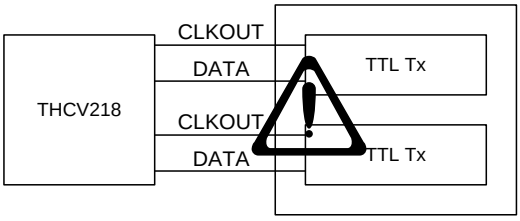
Connect the each GND of the PCB which Transmitter, Receiver and THCV217 on it. It is better for EMI reduction to place GND cable as close to LVDS and CML cable as possible.

3)Asynchronous use

Asynchronous use such as following system are not recommended. Data sheet p.18 tRS/tRH should be kept.



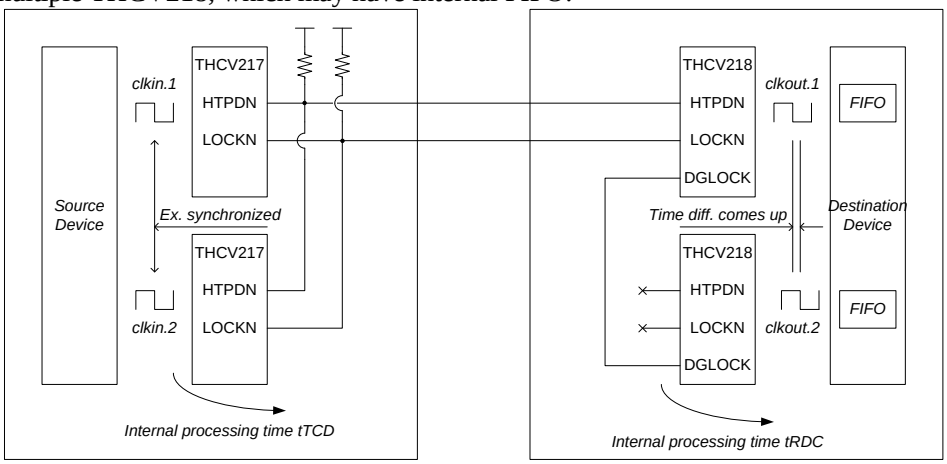
Asynchronous use such as following system are not recommended.



4)Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.
LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.
LOCKN of Tx side can be simply split to multiple Tx. THCV218 DGLOCK is appropriate for multiple Rx use.

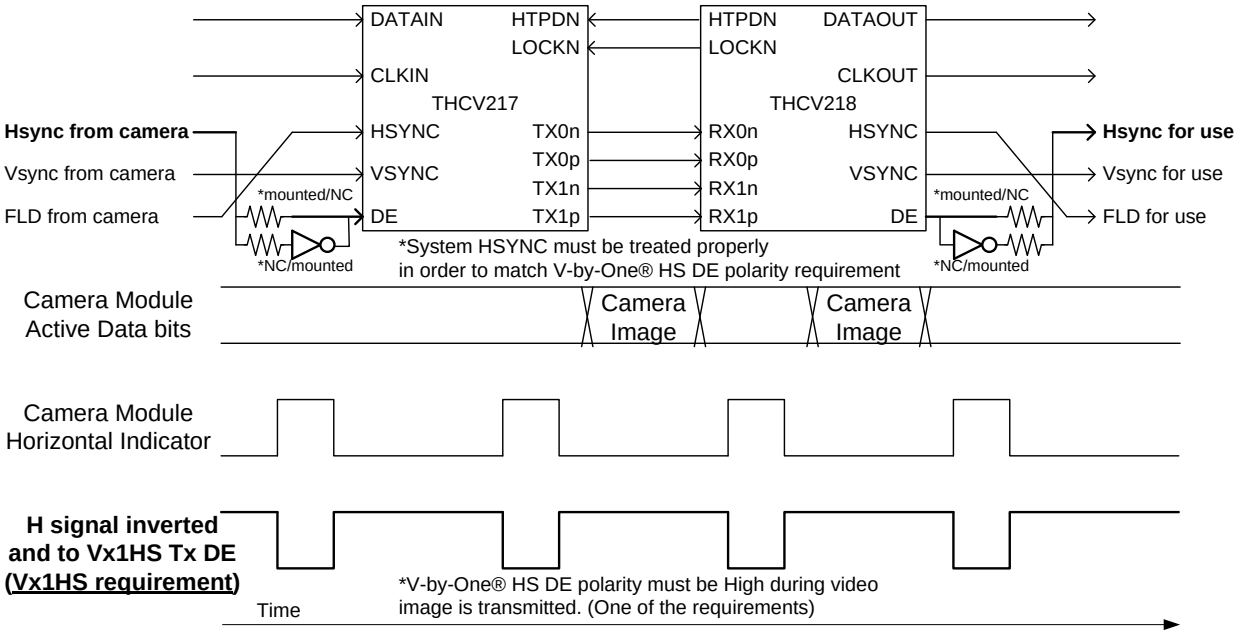
Also possible time difference of internal processing time (Data sheet p.19 THCV217 tTCD and THCV218 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV218, which may have internal FIFO.



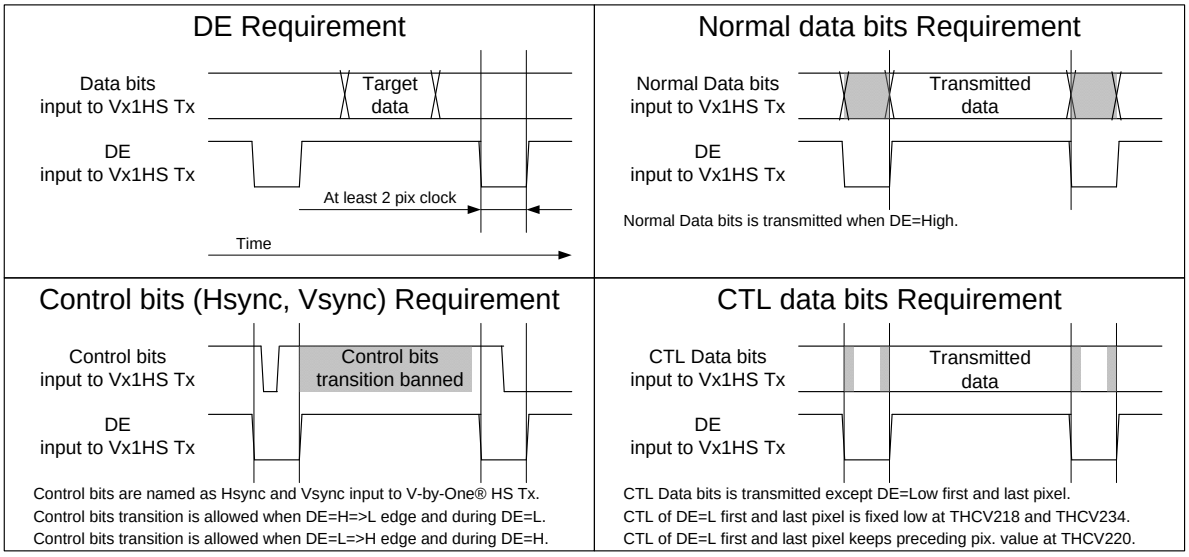
5)In case of No DE in video signal stream

V-by-One® HS transmission always requires DE, while some system has only HSync and VSync.

Sometimes Hsync should be connected to DE and other treatment is at the same time required.
DE polarity on active data transmission period must be High, which sometimes needs external inverter.



Below are consideration points if there is no DE signal on original data format.



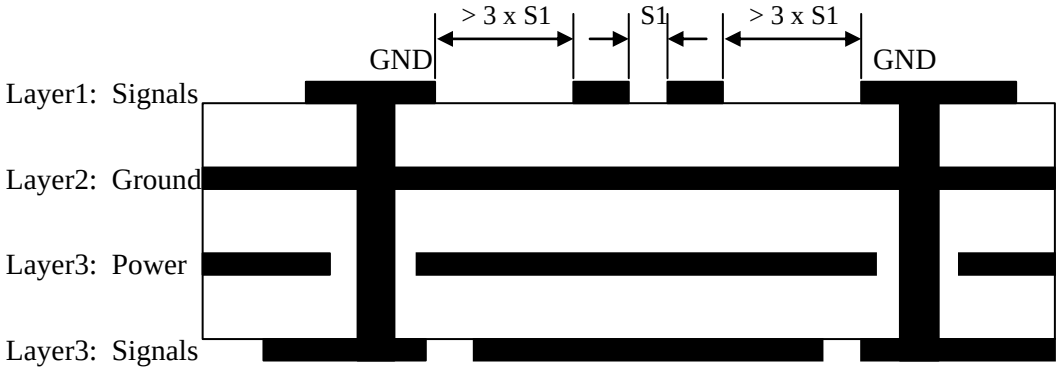
If this kind of configuration is required, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity. Mismatch among impedances of PCB traces, connectors, or cables also causes reflection, limiting the bandwidth of the high-speed channels.

PCB Cross-sectional View
for Microstrip Lines



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1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

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5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
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   5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.
sales@thine.co.jp