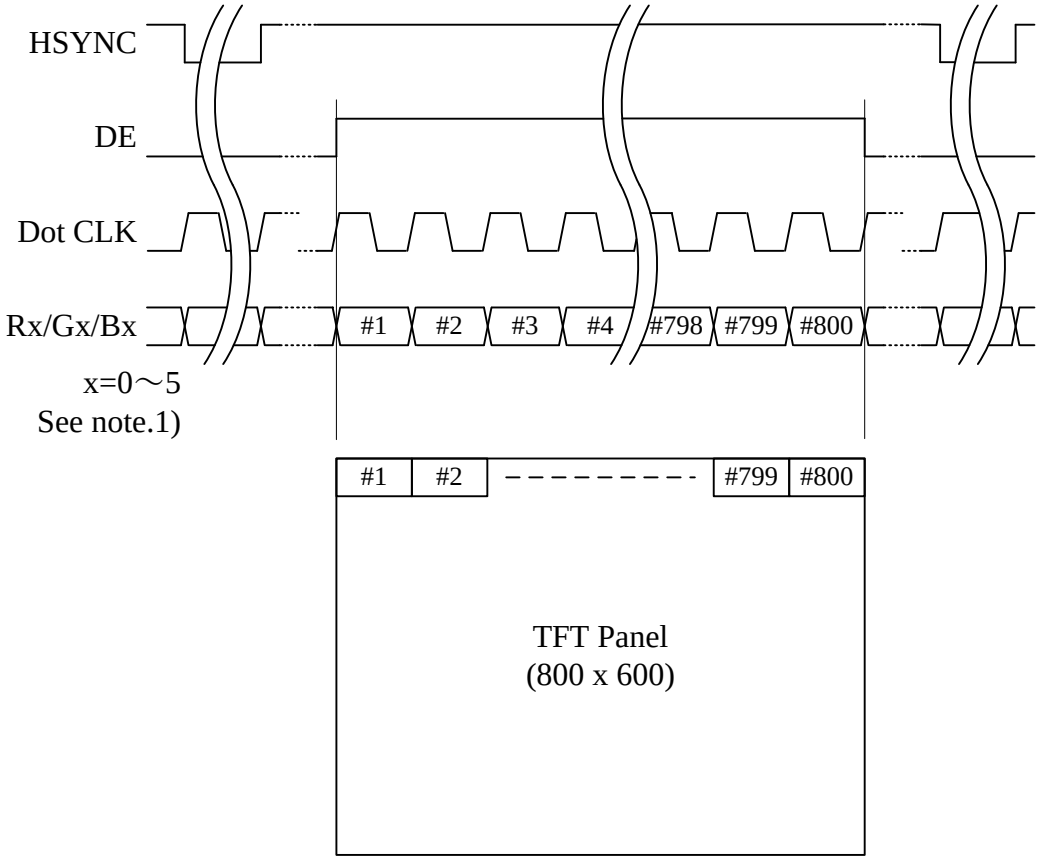
THCV213/THCV214 Application Note

System Diagram and PCB Design Guideline

1) TTL DATA Timing Diagram

The following is THCV213 TTL data input timing example for SVGA(800 x 600).



Note.

1) RGB signal Assignments.

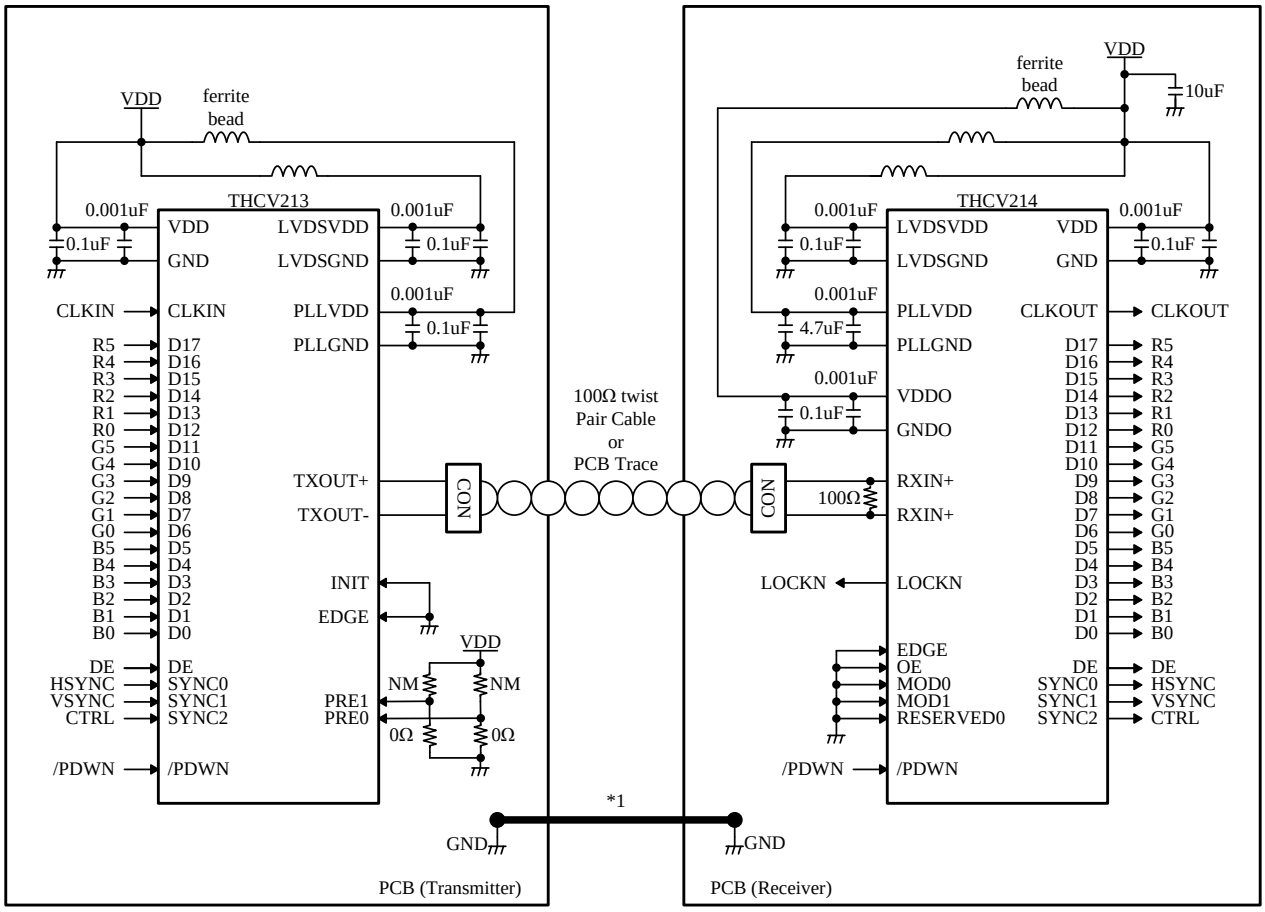
	Red	Green	Blue
MSB	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
	R2	G2	B2
	R1	G1	B1
6bit LSB	R0	G0	B0

2) Min. pulse widths for HSYNC/VSYNC/DE are 2pixels.

2) Examples of System Diagram

(i) Normal Mode

Example:
THCV213: Falling edge / without pre-emphasis.
THCV214: Falling edge / Normal Mode.



Note:

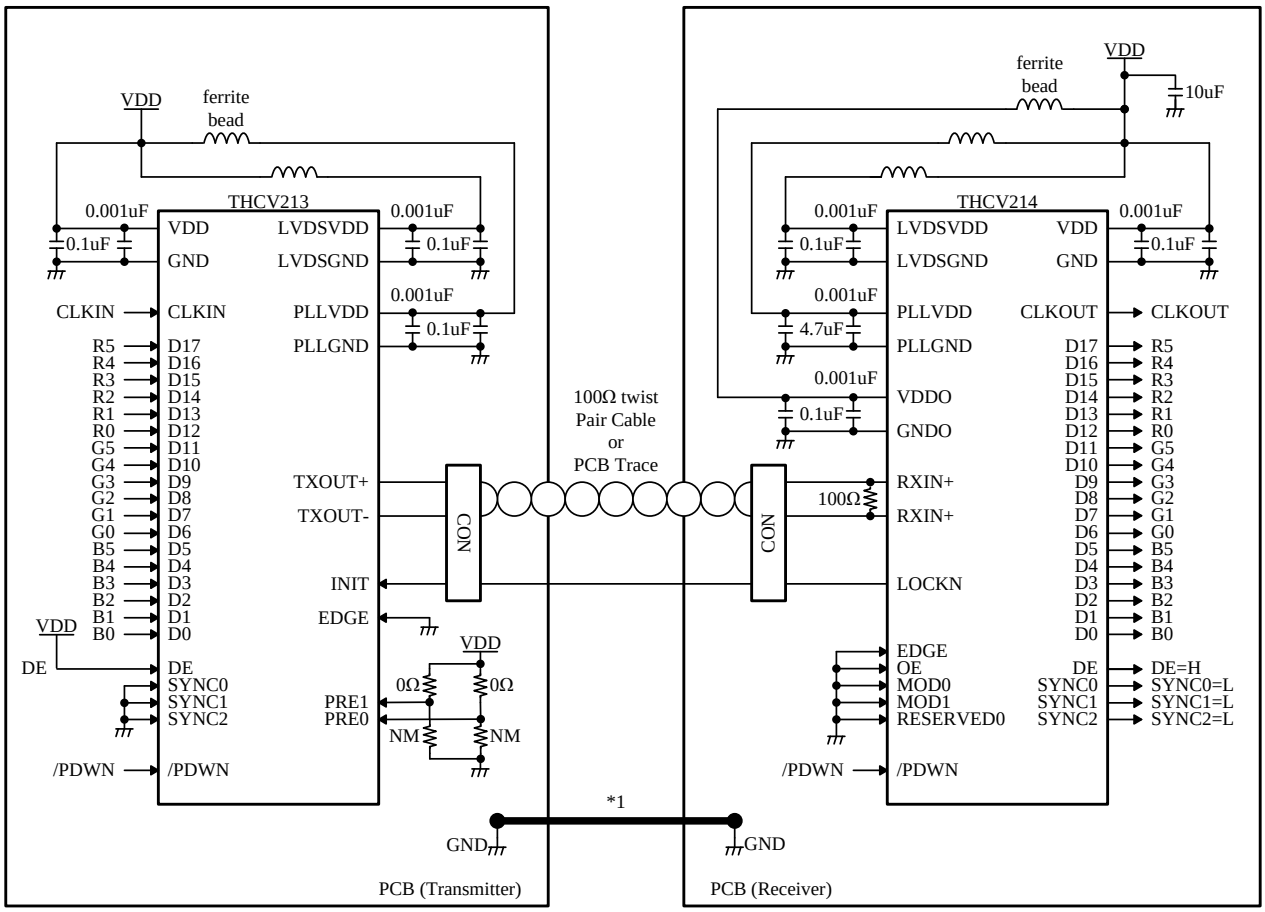
DE signal must meet the following requirements:

1) Min. of DE=L duration is 50 Clocks
2) Max. of DE=H pulse width is 80us, Min.of DE=H pulse width is 2clocks

*1: Connect each PCB GND

(ii) Shake Hand Mode

Example:
THCV213: Falling edge / Pre-emphasis (100%) mode.
THCV214: Falling edge / Shake Hand Mode.



Note:
If there is no DE input, you must keep DE of THCV213 high and set SYNC2-0 low.

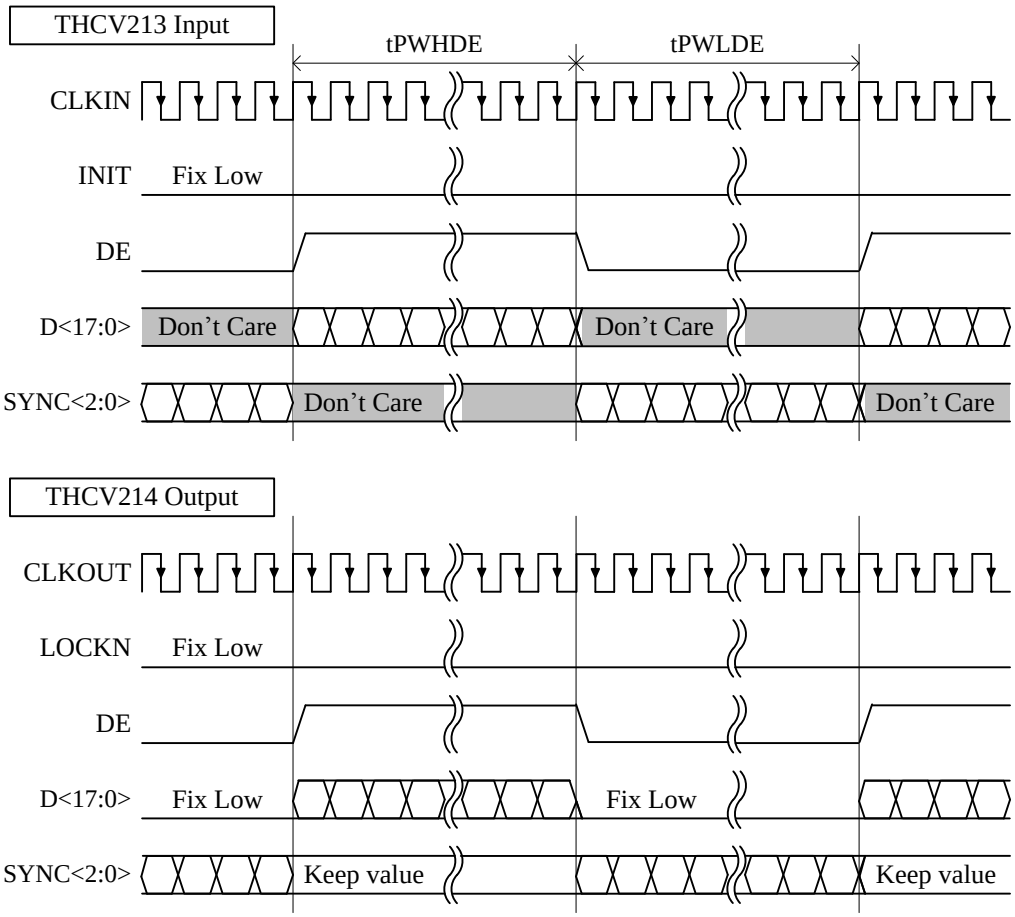
DE signal must meet the following requirements:

1) Min.of DE=H pulse width is 2clocks
2) Min.of DE=L pulse width is 2clocks

*1: Connect each PCB GND

3) Timing Chart

Following timing chart is common for all link mode.
THCV213: Falling edge (EDGE=Low)
THCV214: Falling edge (EDGE=Low)



Requirements for DE pulse width

THCV214 Mode	tPWHDE	tPWLDE	Remarks
Normal	Min. 2Clock Max. 80us	Min. 50Clock	-
Shake Hand	Min. 2Clock	Min. 2Clock	-

4) THCV214 Receiver Eye Mask Diagram.

Differential voltage/timing (EYE) diagram

Eye diagram measurement is performed with an oscilloscope capable of recovering clock from the incoming data stream. The clock recovery algorithm is set as specified in Table 1. Differential eye measurement is performed at either the termination resistor located close to the receiver chip or the chip package pins. Waveforms equivalent to 100,000 UI's are captured for the eye mask test.

Refer to Figure 1 and Table2 for receiver eye mask specifications.

Table1 Clock Recovery Algorithm for Eye Mask Test

Item	Value	Unit
Clock Recovery Method	2nd order PLL	-
Nominal Data Rate	Pixel clock *21	bps
PLL's Loop Bandwidth	0.3	MHz
Damping Factor	0.6	-

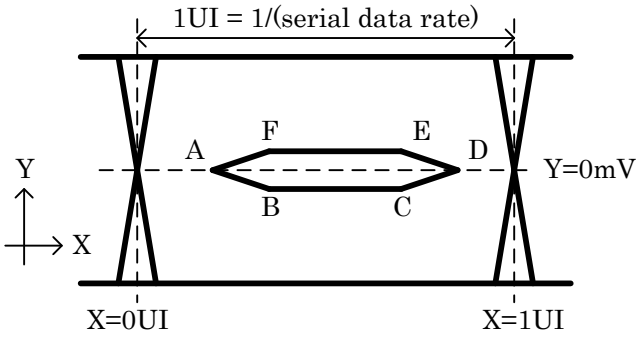


Figure 1 Receive EYE Mask

Table 2 Receiver Mask Vertices Table

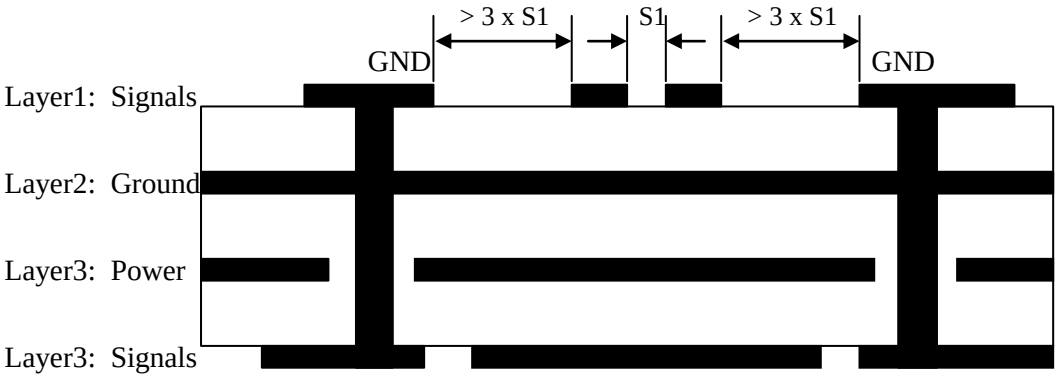
	X[UI]	Y[mV]
A	0.2	0
B	0.35	-50
C	0.65	-50
D	0.8	0
E	0.65	50
F	0.35	50

Note1: UI=Unit Interval.

5) PCB Design Guide Line for LVDS.

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended micro-strip lines or coupled micro-strip lines whose differential characteristic impedance is 100Ω.
- Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low._

PCB Cross-sectional View
for Microstrip Lines



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