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| Application Note | THAN0201_Rev.2.00_E |

THC63LVDM83D/THC63LVDF(R)84C Application Note

System Diagram and PCB Design Guideline

Date	Revision
2015/08/04	Rev.1.00_E
2015/10/21	Rev.1.10_E
2015/11/04	Rev.2.00_E

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1. TTL Data Timing Diagram

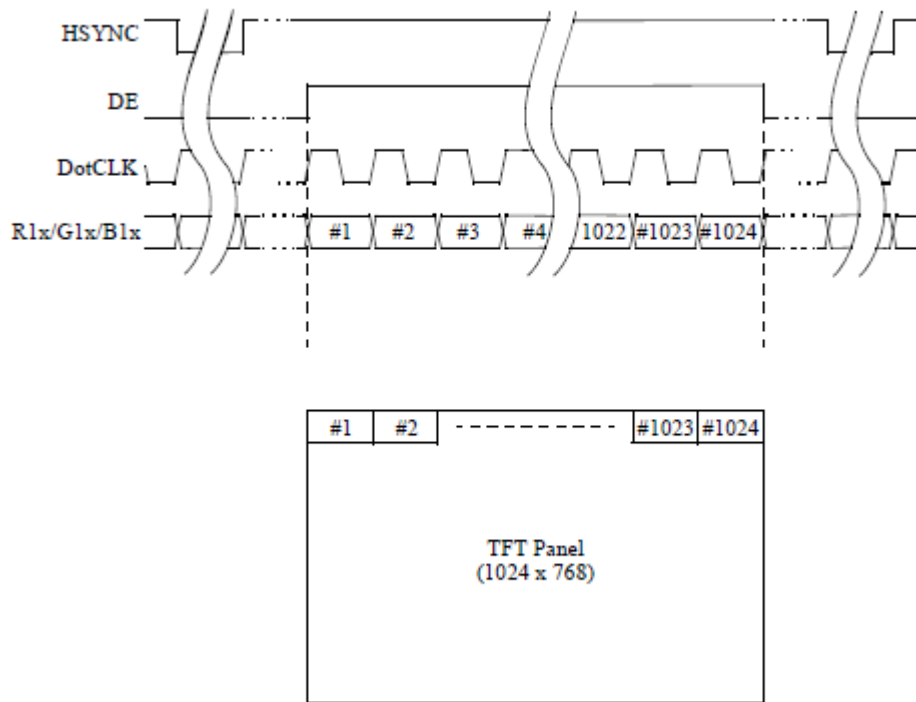Figure 1 and Table 1 shows the THC63LVDM83D TTL data input example for XGA(1024x768).

Figure 1. THC63LVDM83D TTL data timing diagram example (XGA, 1024x768)

Table 1. RGB ordering

	Red	Green	Blue
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
6bit LSB	R2	G2	B2
	R1	G1	B1
8bit LSB	R0	G0	B0

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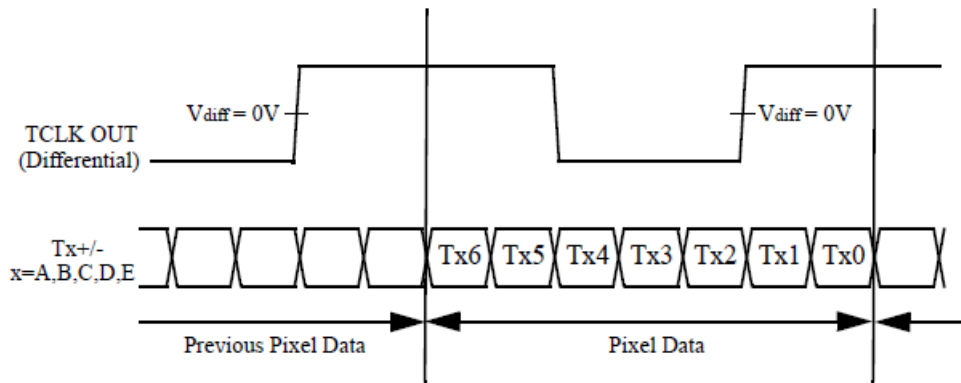
2. LVDS Data Timing Diagram

Figure 2. THC63LVDF(R)84C LVDS data input timing diagram

Table 2. THC63LVDM83D/THC63LVDF(R)84C Pixel Data Assignment (6bit, 8bit Application)

	6bit	8bit
TA0	R2	R2
TA1	R3	R3
TA2	R4	R4
TA3	R5	R5
TA4	R6	R6
TA5	R7	R7
TA6	G2	G2
TB0	G3	G3
TB1	G4	G4
TB2	G5	G5
TB3	G6	G6
TB4	G7	G7
TB5	B2	B2
TB6	B3	B3
TC0	B4	B4
TC1	B5	B5
TC2	B6	B6
TC3	B7	B7
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	–	R0
TD1	–	R1
TD2	–	G0
TD3	–	G1
TD4	–	B0
TD5	–	B1
TD6	–	N/A

Note: For 6bit application, use TA-TC channel and open TD+/- pin.
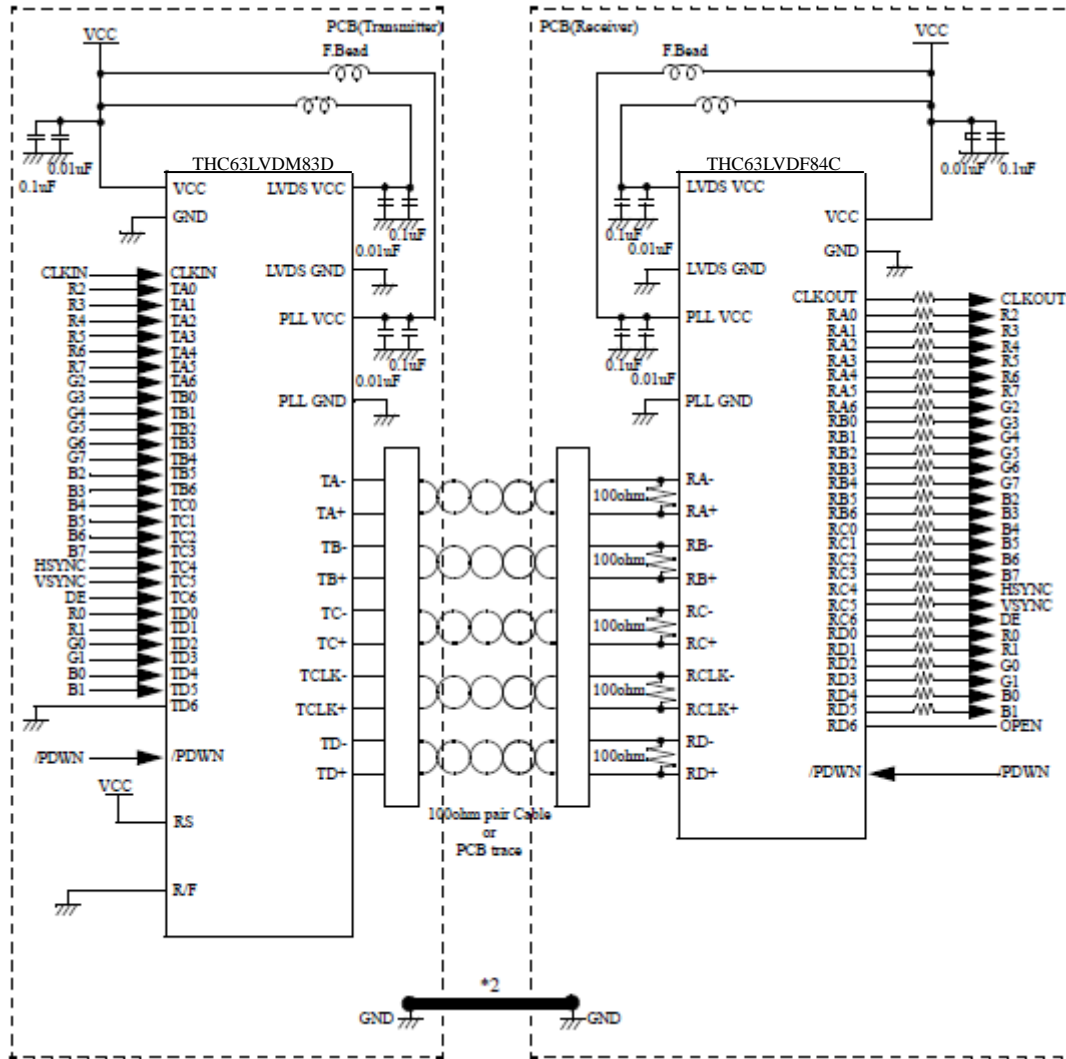
3. Examples of System Diagrams

1) 8bit TTL/CMOS Input(8 to 112MHz)

Example:
  THC63LVDM83D: Falling edge/Normal Swing
  THC63LVDF84C: Falling edge

   *1: If RS pin is tied to VCC, LVDS swing is 350mV.
      If RS pin is tied to GND, LVDS swing is 200mV.
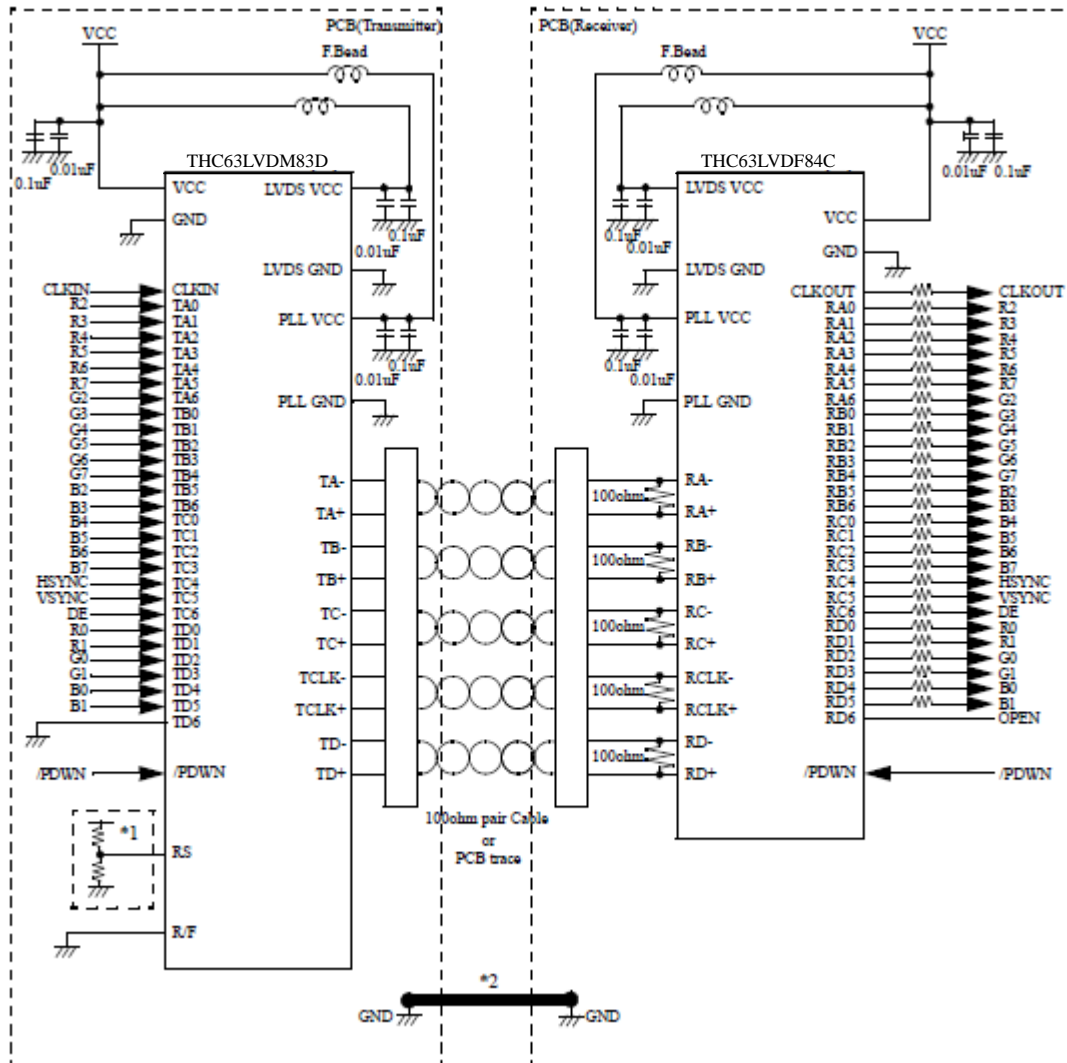
   *2: Connect each PCB GND

Figure 3. System Diagram Example (8bit TTL/CMOS Input)

2) 8bit Small Swing Input(8 to 112MHz)
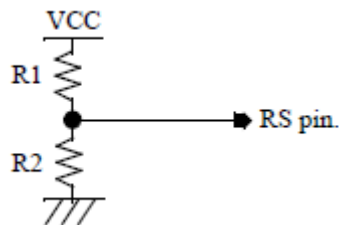
Example:

  THC63LVDM83D: Small Swing input/Falling edge

  THC63LVDF84C: Falling edge

∗1: RS pin acts as VREF input pin when input voltage is set to half of high level signal input.
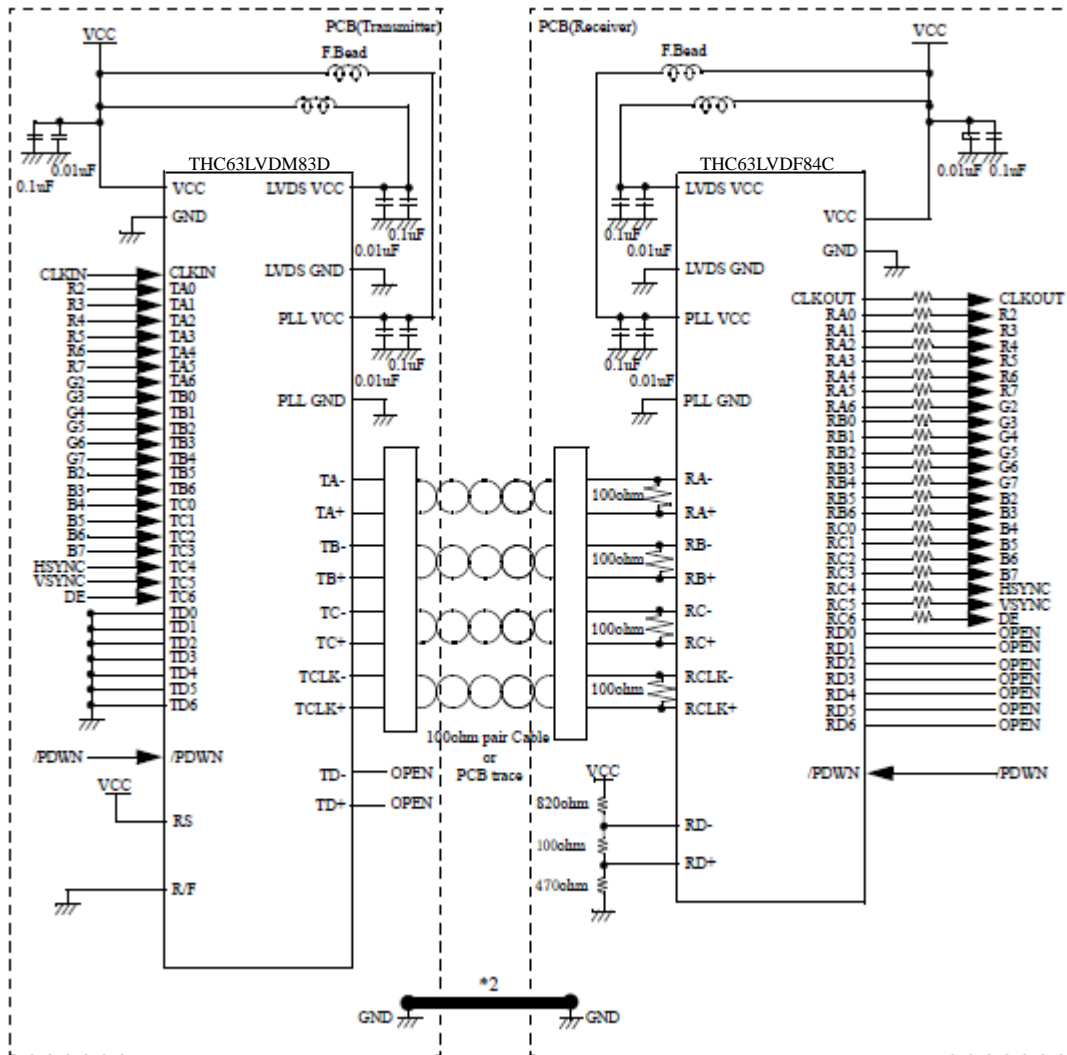

*2: Connect each PCB GND

Figure 4. System Diagram Example (8bit Small Swing Input)

3) 6bit TTL/CMOS Input(8 to 112MHz)

Example:

   THC63LVDM83D: Falling edge/Normal Swing

   THC63LVDF84C: Falling edge

*1: If RS pin is tied to VCC, LVDS swing is 350mV.

    If RS pin is tied to GND, LVDS swing is 200mV.

*2: Connect each PCB GND

Figure 5. System Diagram Example (6bit TTL/CMOS Input)

4. Note

1) Power On Sequence
   Power on THC63LVDM83D after THC63LVDF(R)84C is powered on.

2) Cable Connection and Disconnection
   Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

3) GND Connection
   Connect the each GND of the PCB which THC63LVDM83D and THC63LVDF(R)84C on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

4) Multi Drop Connection
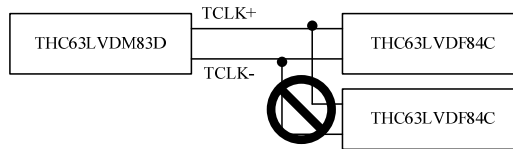   Multi drop connection is not recommended.

Figure 6. Multi Drop Connection Example (not recommended)

5) Asynchronous Use
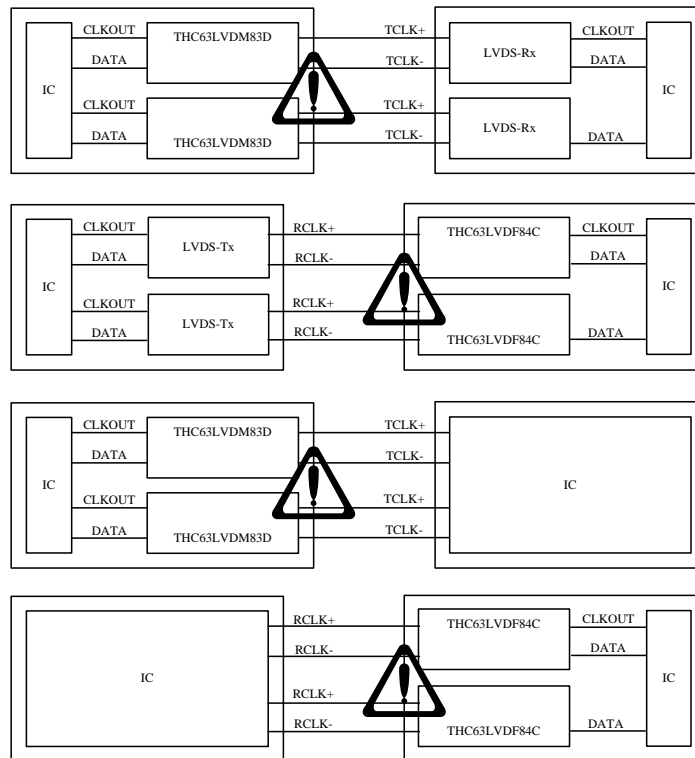   Asynchronous use such as following systems is not recommended.

Figure 7. Asynchronous Use Examples (not recommended)

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5. PCB Design Guideline

General Guideline

• Use 4 layer PCB (minimum).
• Locate by-pass capacitors adjacent to the device pins as close as possible.
• Make the loop minimum which is consist of Power line and Gnd line.

LVDS Traces

• Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
• Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
• Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as much as possible.
• Avoid 90 degree bends.
• Minimize the number of VIA on LVDS traces.
• Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
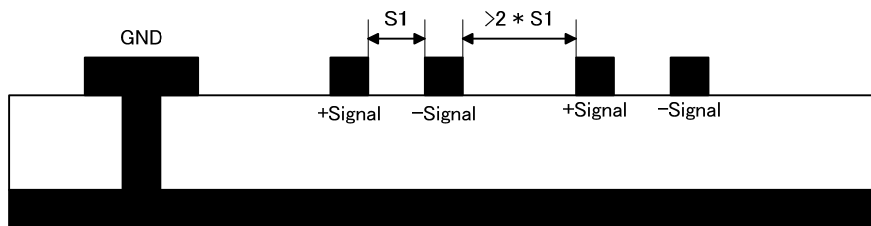• Place Terminal Resister adjacent to the Receiver.

Figure 8. PCB Design Guideline

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