Application Note	THAN0135 _Rev.1.01_E

THC63LVD827
Application Note
System Diagram and PCB Design Guide Line

Date	Revision
20120420	THAN0135_Rev.1.00_E
20160712	THAN0135_Rev.1.01_E

Contents

1. Mode Settings

Input / Output	Option	MODE	DDRN	O/E
		Input Mode	Double Data Rate	Output Enable
		H : Single	H : DDR Input off	H : Enable
		L : Dual	L : DDR Input on-	L : Disable
Single In / Single Out	Output Disable (Hi-Z)	H	-	L
	Output Enable	H	-	H
Single In / Dual Out	Output Disable (Hi-Z)	L	-	L
	Output Enable/DDR off	L	H	H
	Output Enable/DDR on	L	L	H

2. Signal Flow for Each Setting

Single In / Single Out

Single In / Dual Out
Double Data Rate off

Single In / Dual Out
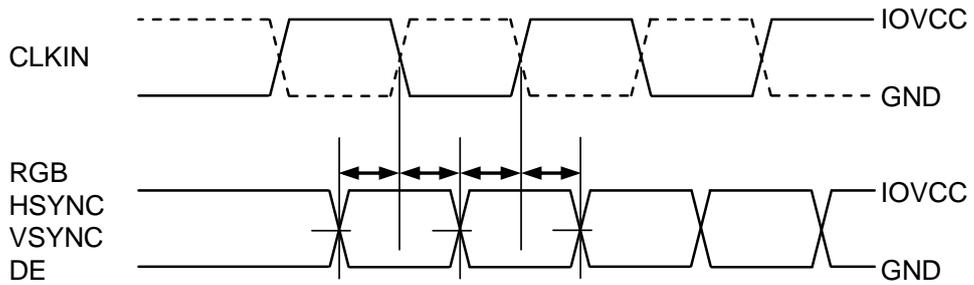Double Data Rate on
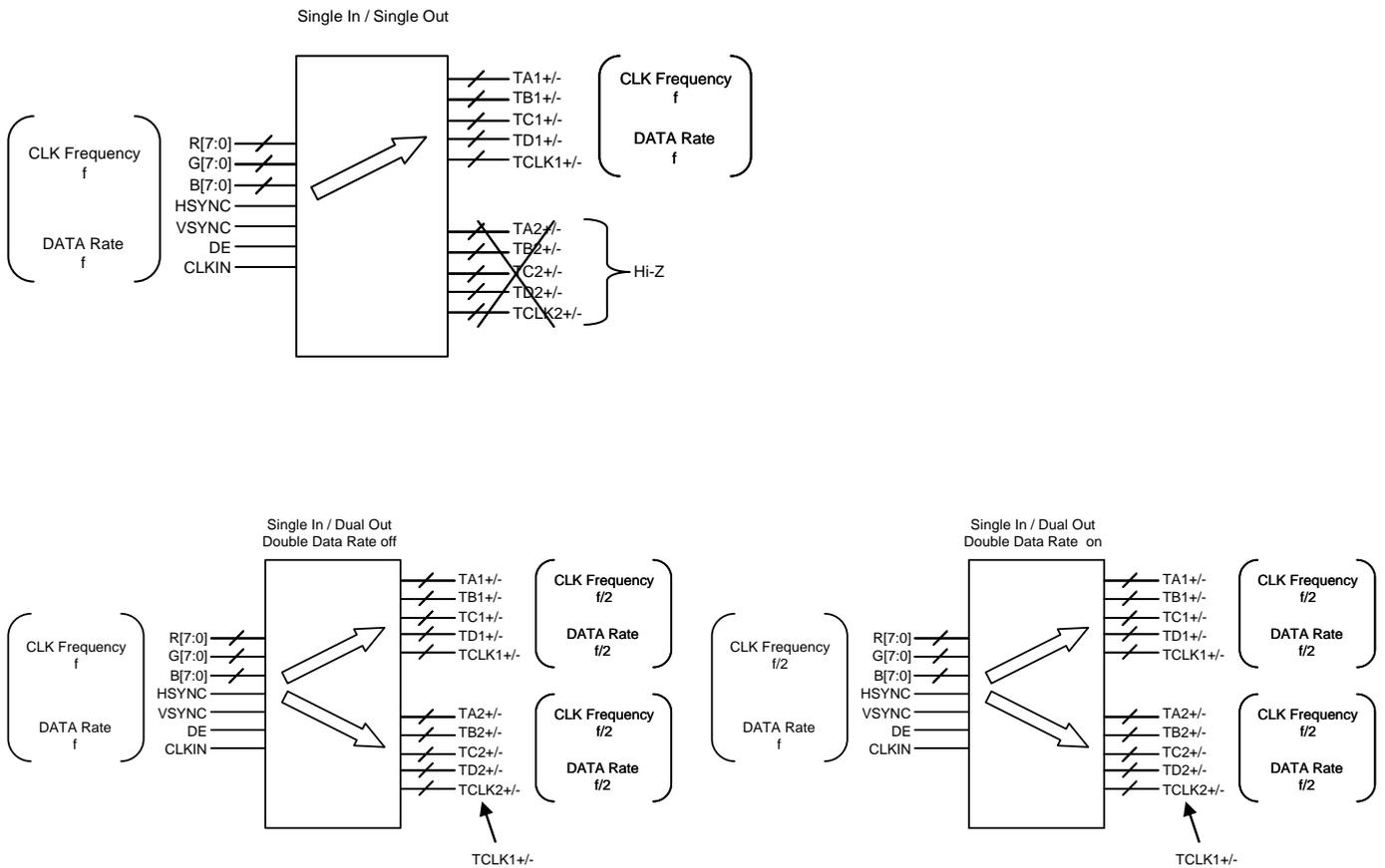
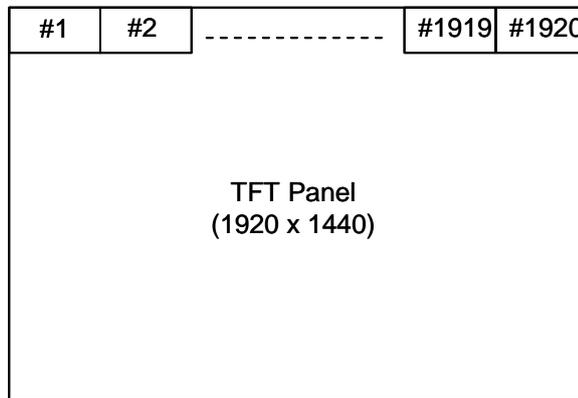## 3. COMS/TTL Data Timing Diagram

1) Single Edge Input Mode (MODE=H or MODE=L, DDR=H)
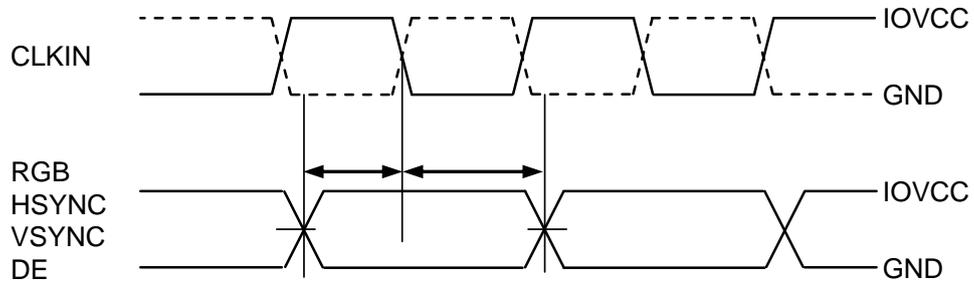
2) Double Edge Input Mode (MODE=L, DDR=L)

3) Data sorting example of TTL input versus LVDS output in Single-In Dual-Out mode with double edge Input mode for 1920 x 1440 panel.

Single CMOS/TTL Input

Dual LVDS Output
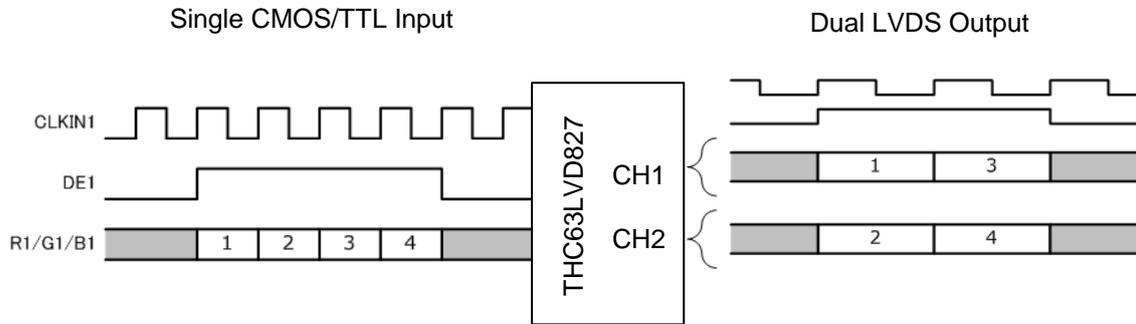
MSB	R17	G17	B17
	R16	G16	B16
	R15	G15	B15
	R14	G14	B14
	R13	G13	B13
	R12	G12	B12
	R11	G11	B11
LSB	R10	G10	B10

4. LVDS Data Timing Diagram
1) Single In- Dual Out Mode (MODE=L)

Security E
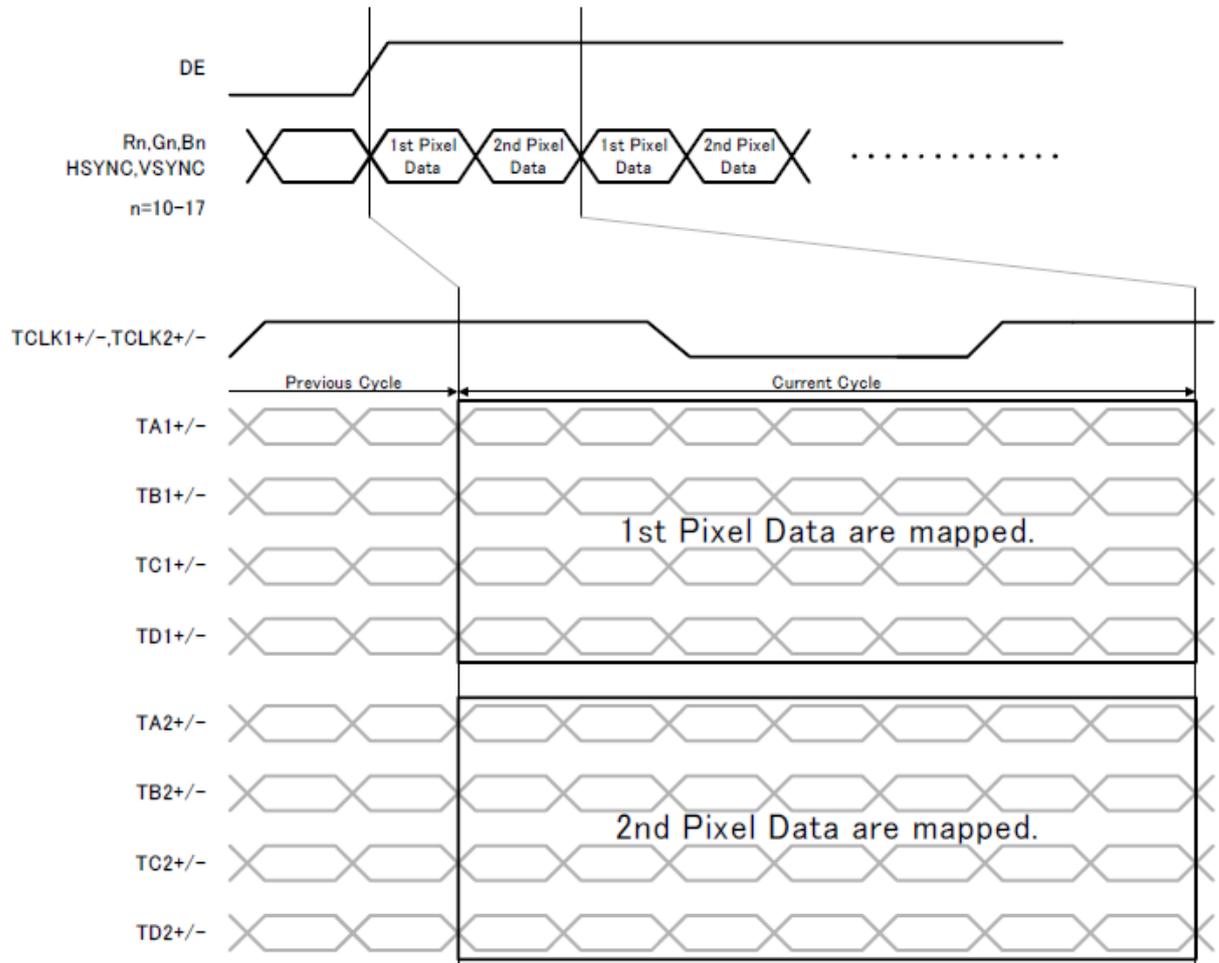
2) Single In- Single Out Mode (MODE=H)
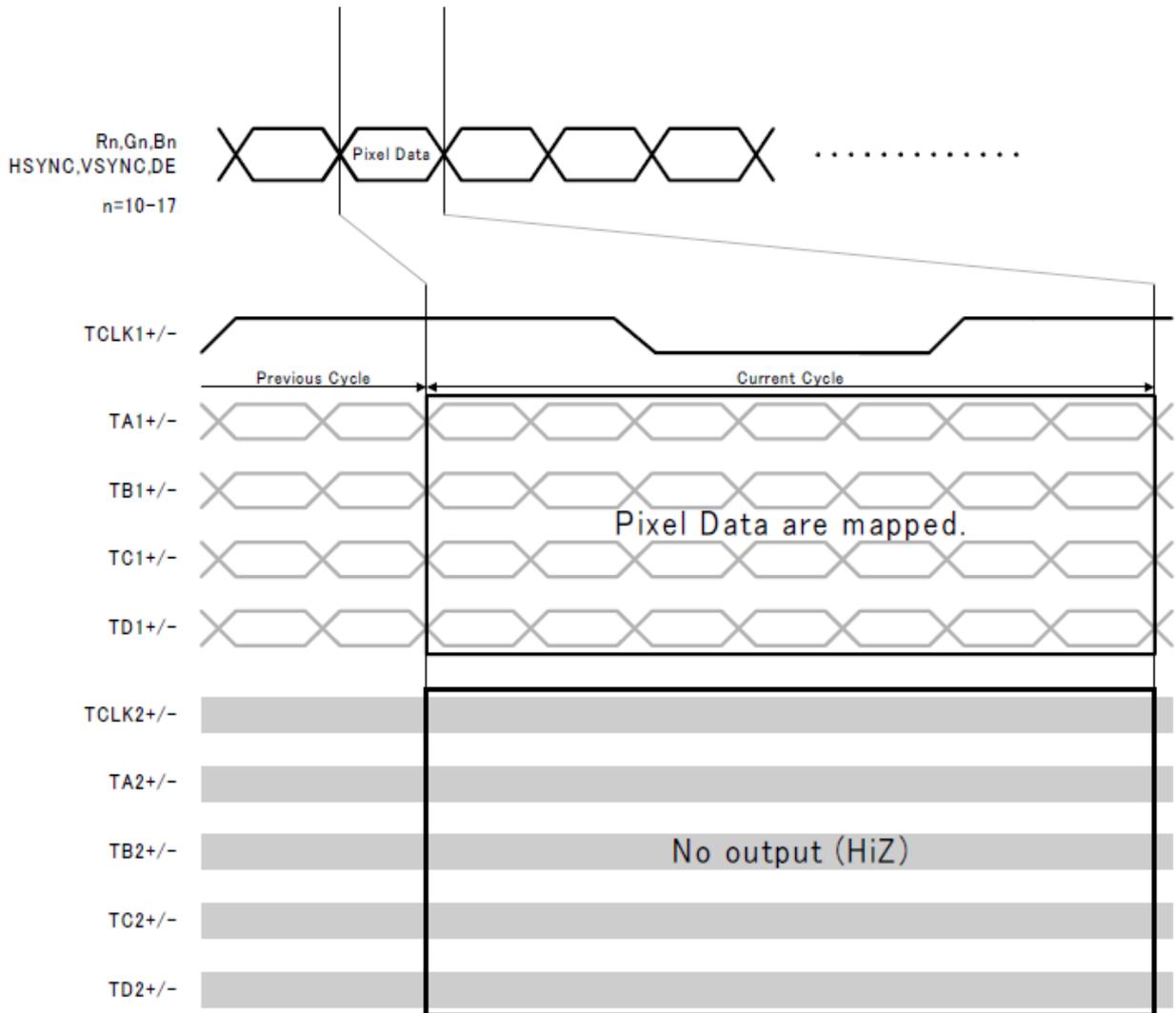
5. LVDS Data Mapping

1) for 8 bit mode (6B/8B=L)

(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)

(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

2) for 6 bit mode (6B/8B=H)

(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)
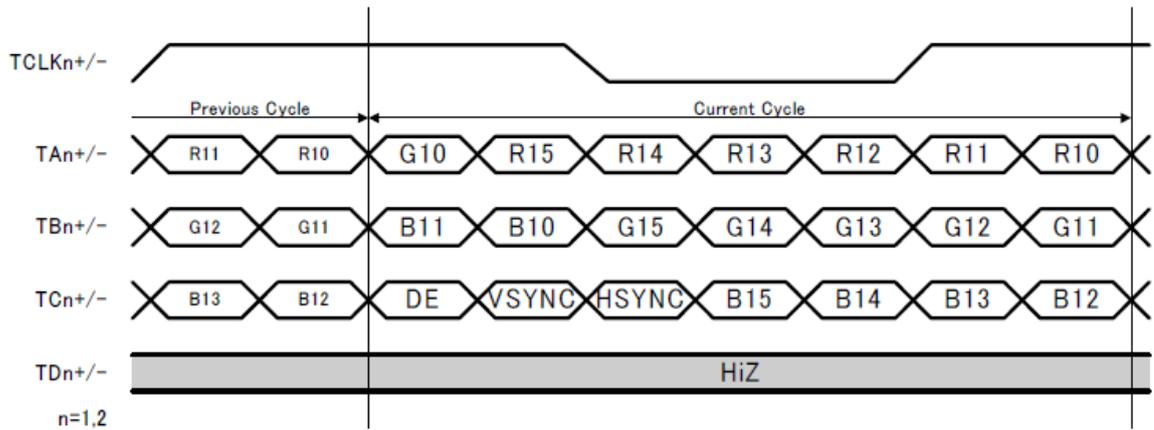
(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

6. Example of System Diagram

1) Single In–Single Out / 8bit 1.8V COMS/TTL Input
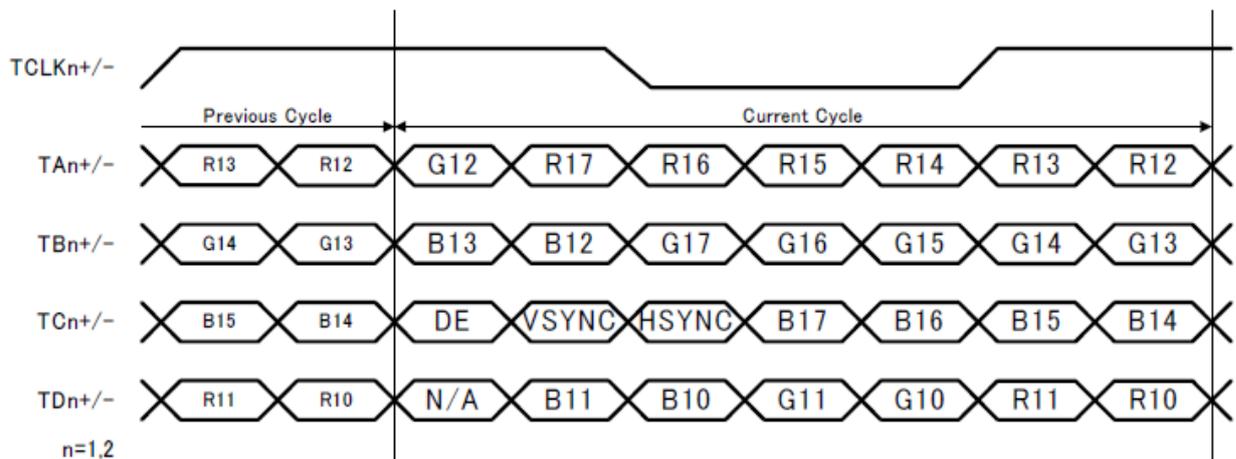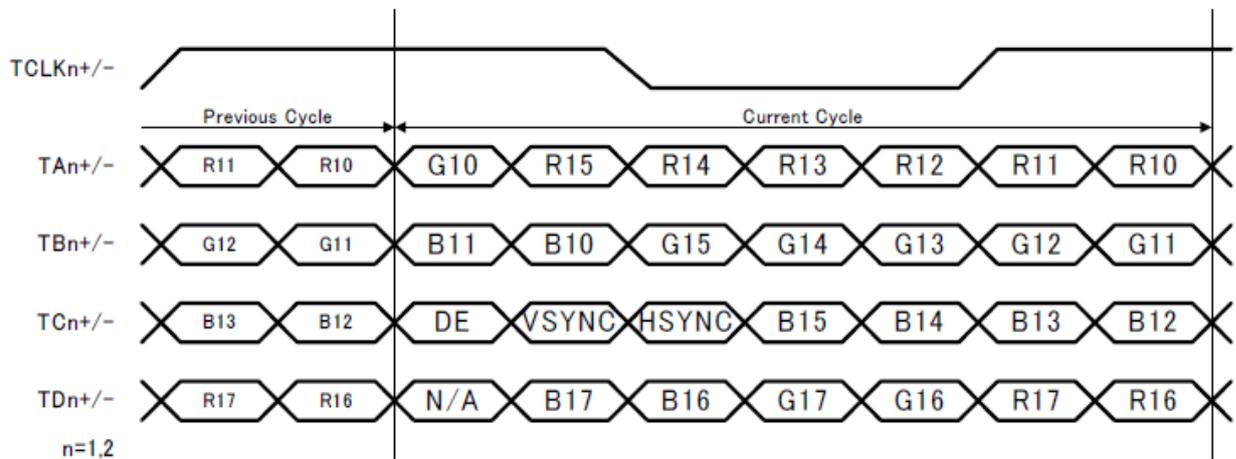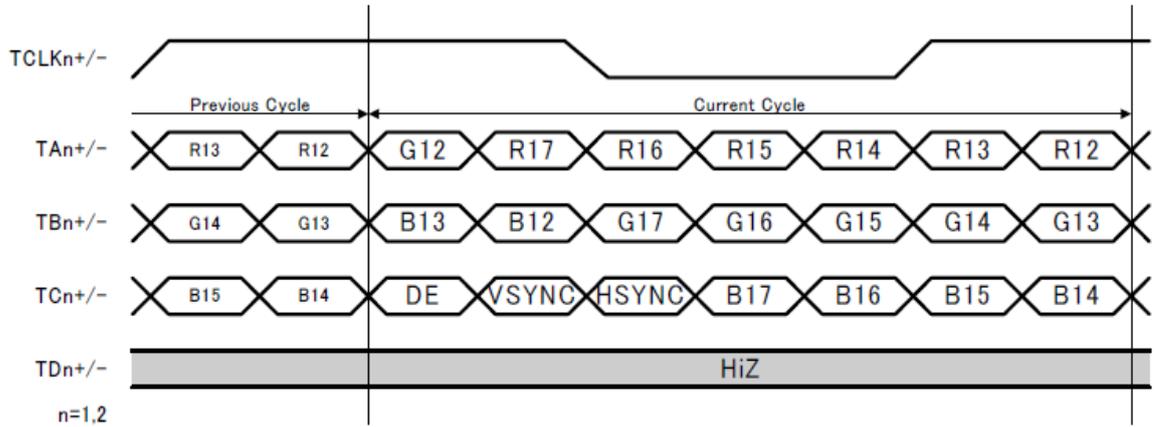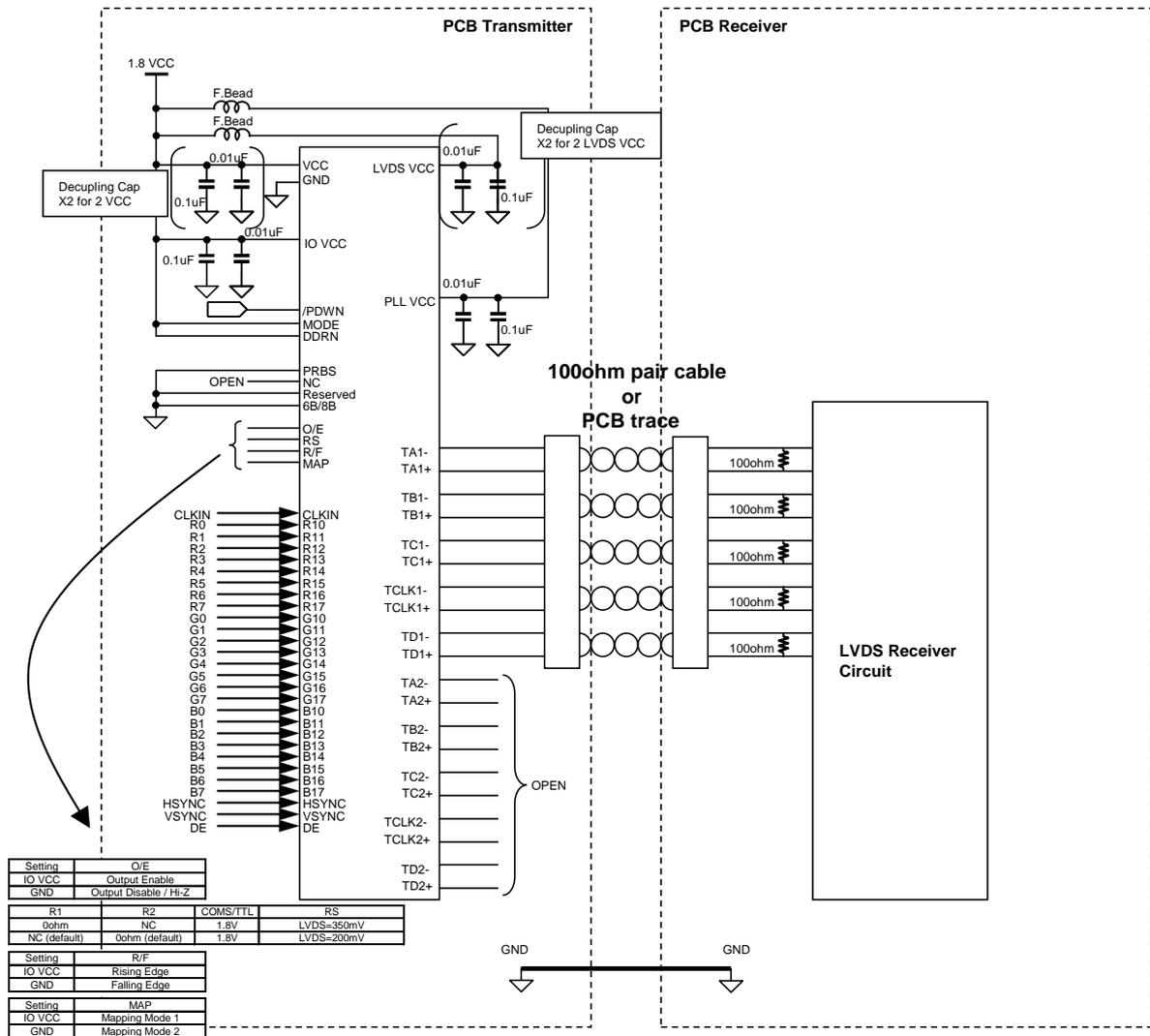

Setting	O/E
IO VCC	Output Enable
GND	Output Disable / Hi-Z

R1	R2	COMS/TTL	RS
0ohm	NC	1.8V	LVDS=350mV
NC (default)	0ohm (default)	1.8V	LVDS=200mV

Setting	R/F
IO VCC	Rising Edge
GND	Falling Edge

Setting	MAP
IO VCC	Mapping Mode 1
GND	Mapping Mode 2

Note :
- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.

THine Electronics, Inc.

Security E

2) Single In –Dual Out / 8bit 1.8V COMS/TTL Input
DDR(Double Edge input) function disable.
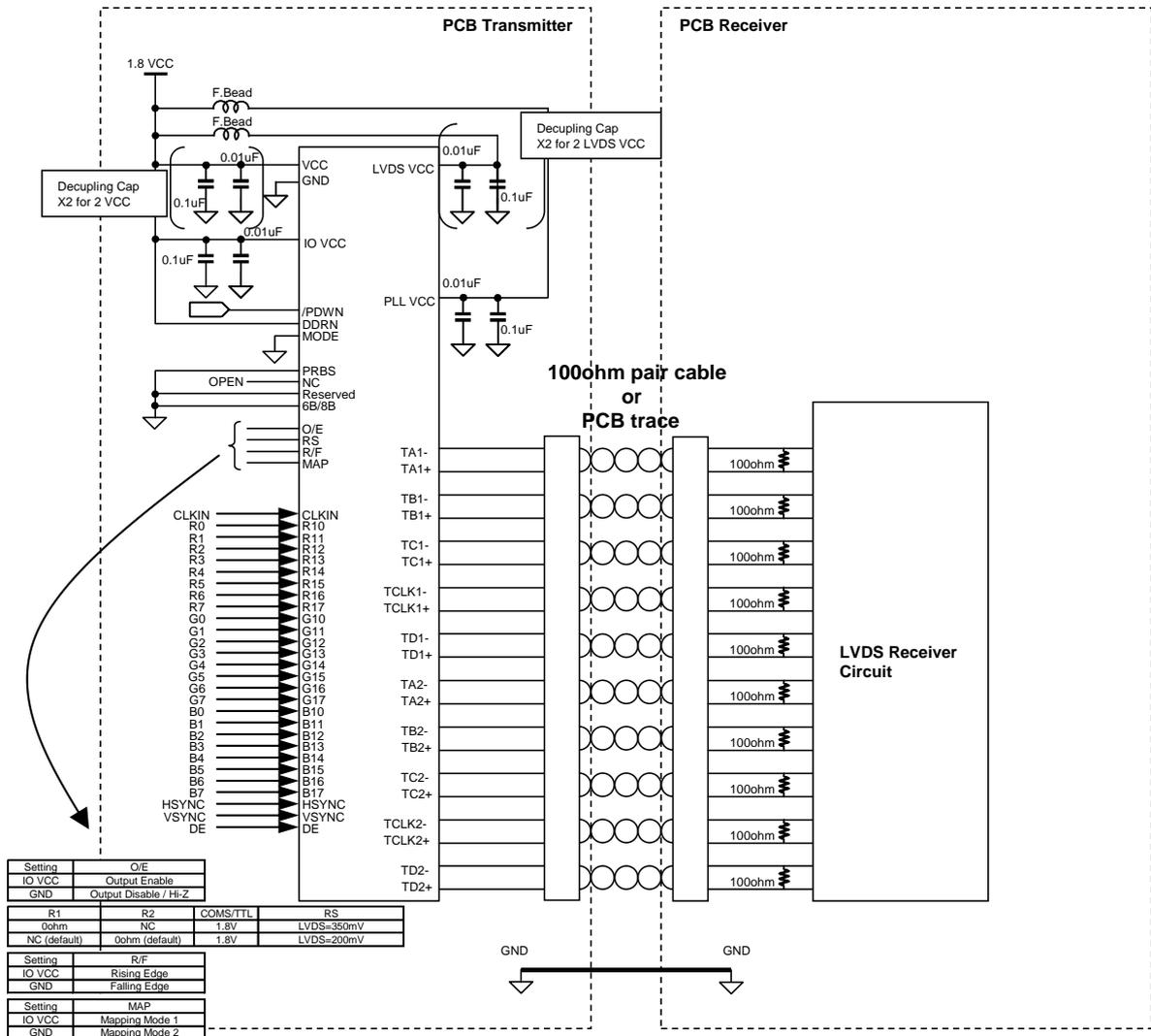
Setting	O/E
IO VCC	Output Enable
GND	Output Disable / Hi-Z

R1	R2	COMS/TTL	RS
0ohm	NC	1.8V	LVDS=350mV
NC (default)	0ohm (default)	1.8V	LVDS=200mV

Setting	R/F
IO VCC	Rising Edge
GND	Falling Edge

Setting	MAP
IO VCC	Mapping Mode 1
GND	Mapping Mode 2

Note :
- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.

3) Single In –Dual Out / 3.3V 6bit COMS/TTL Input
   DDR(Double Edge input) function enable

Note :
- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.
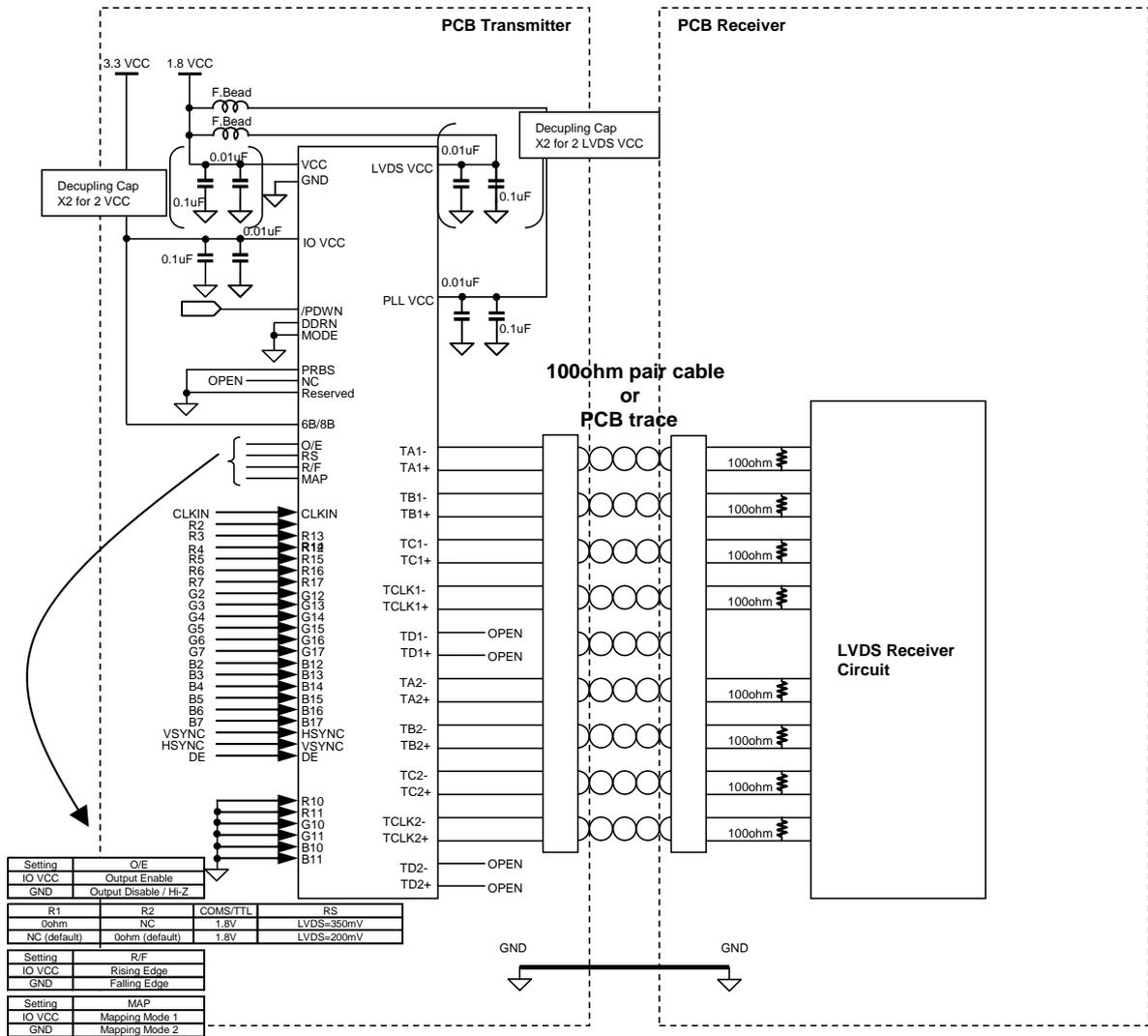
7. Note

7.1) Cable Connection and Disconnection
Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

7.2) GND Connection
Connect the each GND of the Board which THC63LVDM83E and Receiver on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

7.3) Multi Drop Connection
Multi drop connection is not recommended.
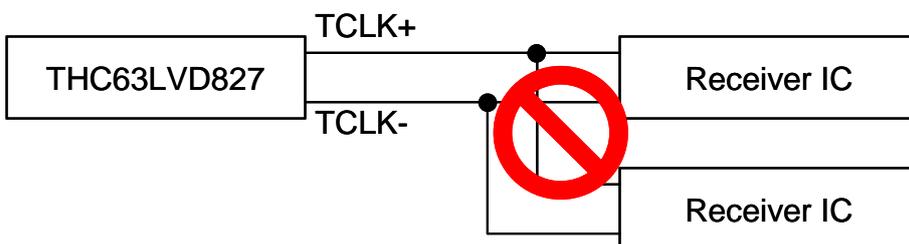
7.3) Asynchronous use
Asynchronous uses such as following systems are not recommended. If it's not avoidable, please contact to

       mspsupport@thine.co.jp   (for FAE mailing list)

8. Trace Example for BGA

TOP VIEW

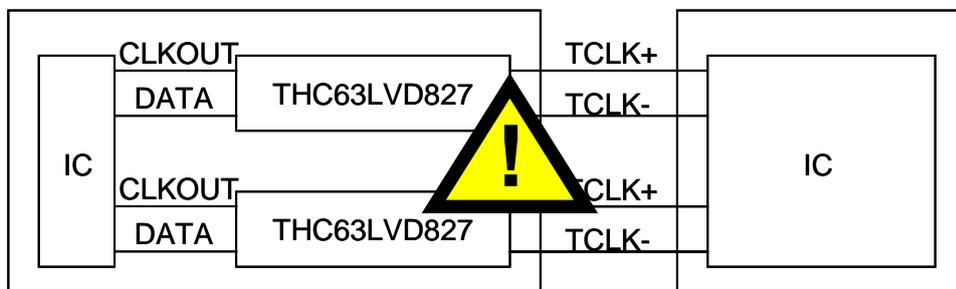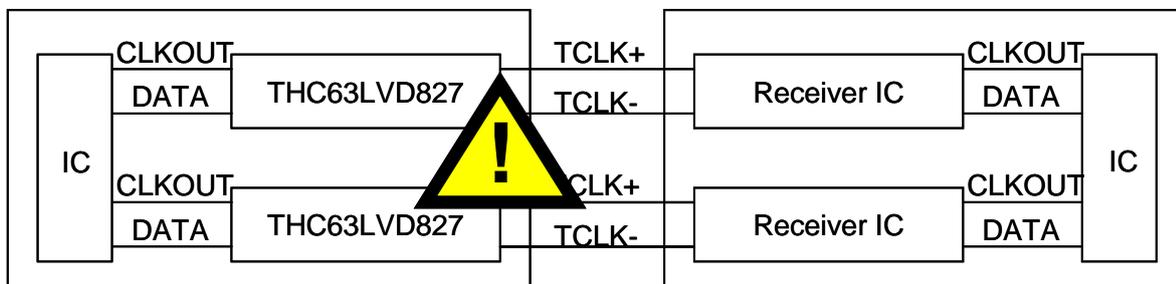|	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	PRBS	NC	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	C
D	R11	R10	LVDS VCC				GND	/PWDN	O/E	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B/8B	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	IO VCC	R/F	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	
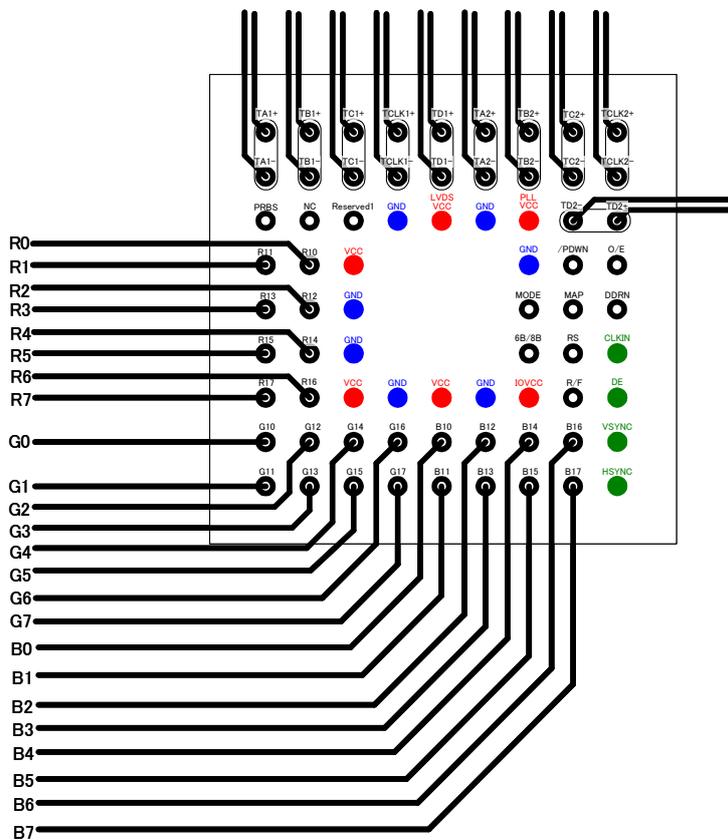
9. PCB Design Guide Line

General Guideline
- Use 4 layers PCB (minimum).
- Locate by-pass capacitors adjacent close to the device pins to a maximum extent.
- Make the loop minimum which is consist of Power line and GND line.
- Use large GND plane.
- Separate VDD power supply for each block via ferrite bead.

LVDS Trace
- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector and cable) should be well balanced. (Keep all these differential impedance and the length of media as same as possible)
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as possible.
- Avoid 90 degree bends and sharp angles.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, cable and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place terminal resistor close to the Receiver pins to a maximum extent.
- To place common mode choke coil is desired for EMI reduction.
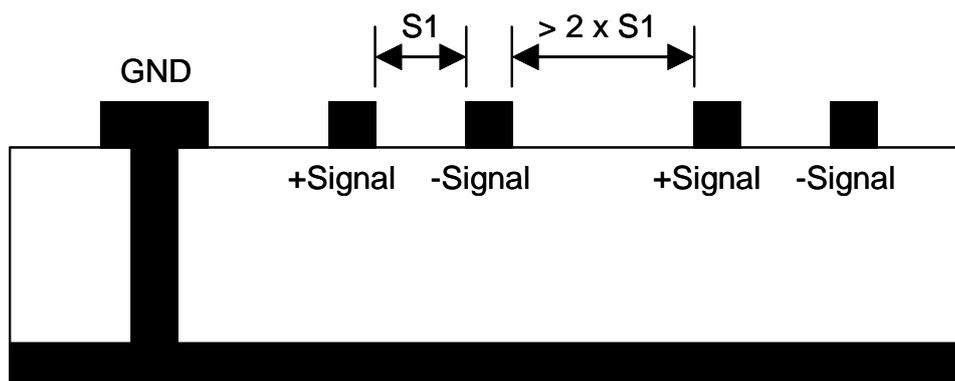
Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.

3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.

4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
   5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. ("THine") accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
   5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.

sales@thine.co.jp