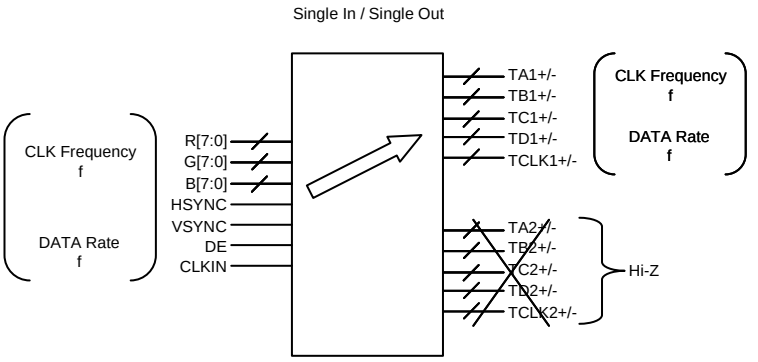
THC63LVD827
System Diagram and PCB Design Guide

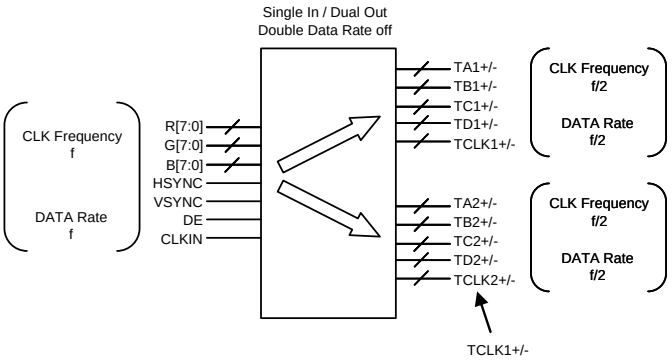
Contents

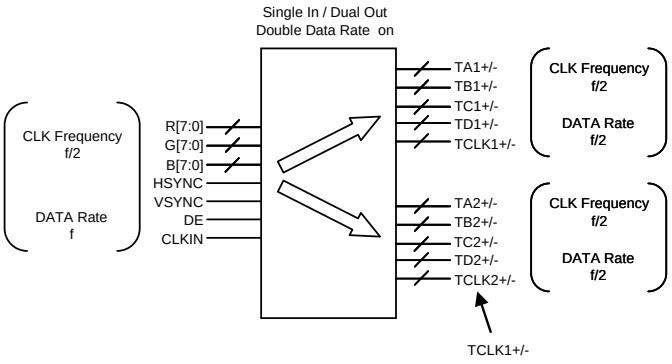
1. Mode Settings

Input / Output	Option	MODE Input Mode H : Single L : Dual	DDRN Double Data Rate H : DDR Input off L : DDR Input on-	O/E Output Enable H : Enable L : Disable
Single In / Single Out	Output Disable (Hi-Z)	H	-	L
	Output Enable	H	-	H
Single In / Dual Out	Output Disable (Hi-Z)	L	-	L
	Output Enable/DDR off	L	H	H
	Output Enable/DDR on	L	L	H

2. Signal Flow for Each Setting

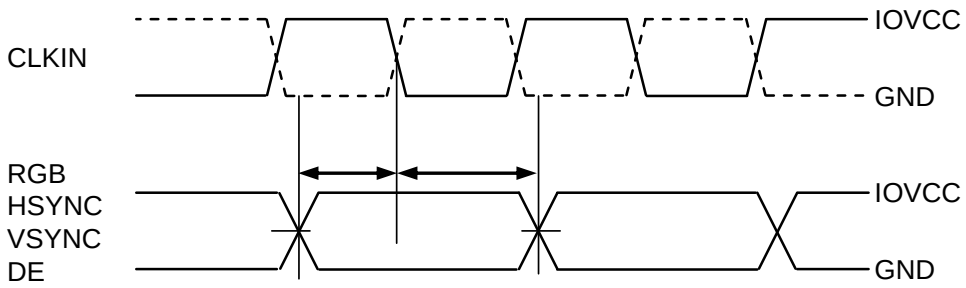




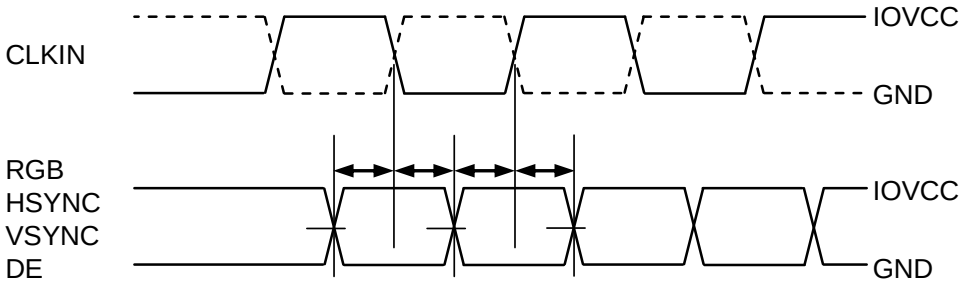


3. COMS/TTL Data Timing Diagram

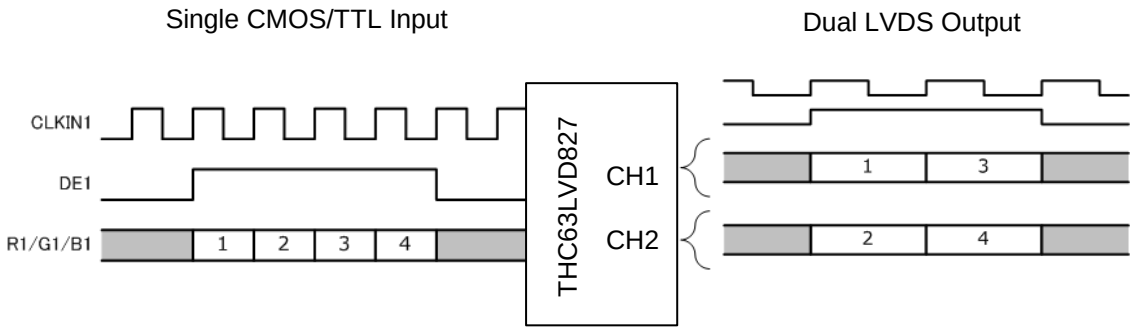
1) Single Edge Input Mode (MODE=H or MODE=L, DDR=H)

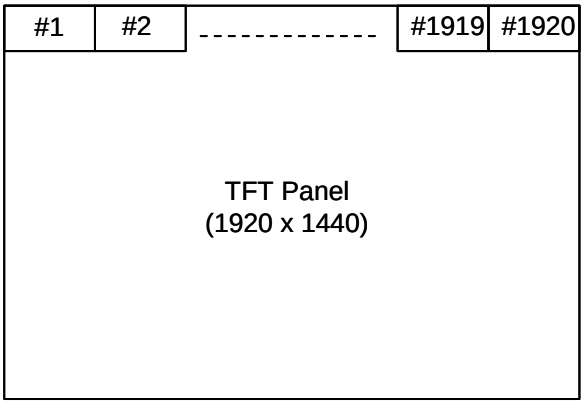


2) Double Edge Input Mode (MODE=L, DDR=L)



3) Data sorting example of TTL input versus LVDS output in Single-In Dual-Out mode with double edge Input mode for 1920 x 1440 panel.

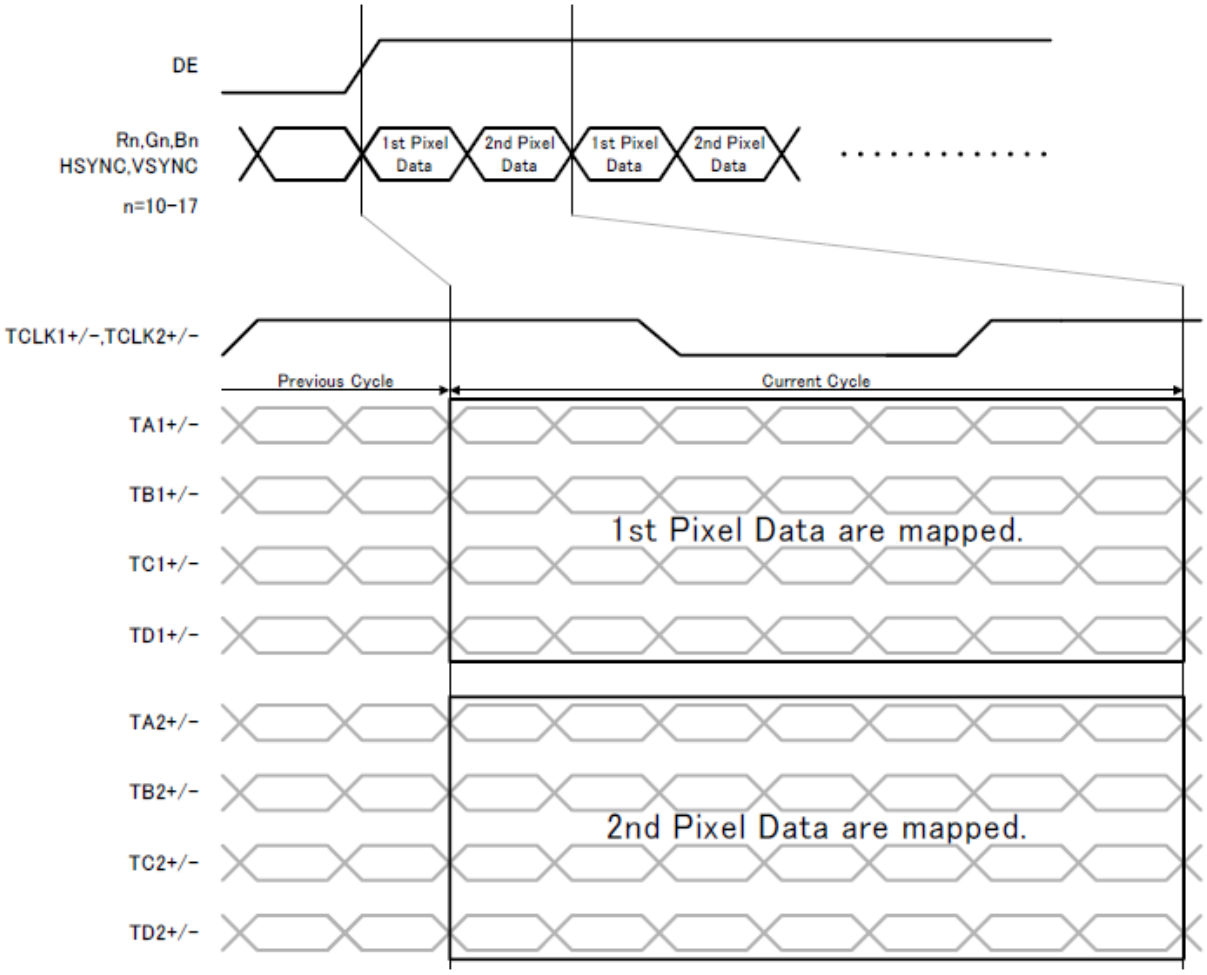




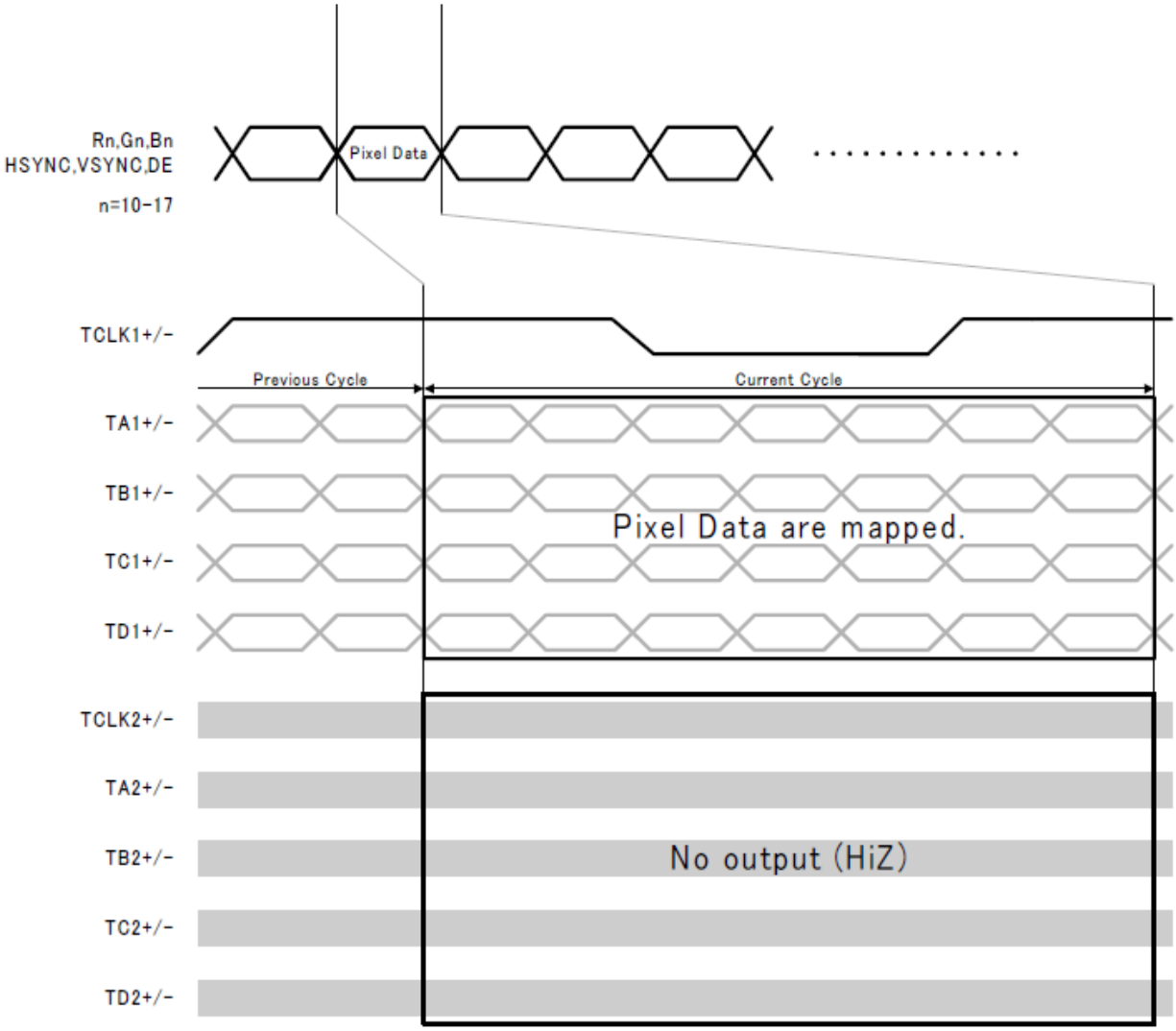
MSB	R17	G17	B17
	R16	G16	B16
	R15	G15	B15
	R14	G14	B14
	R13	G13	B13
	R12	G12	B12
	R11	G11	B11
LSB	R10	G10	B10

4. LVDS Data Timing Diagram

1) Single In- Dual Out Mode (MODE=L)

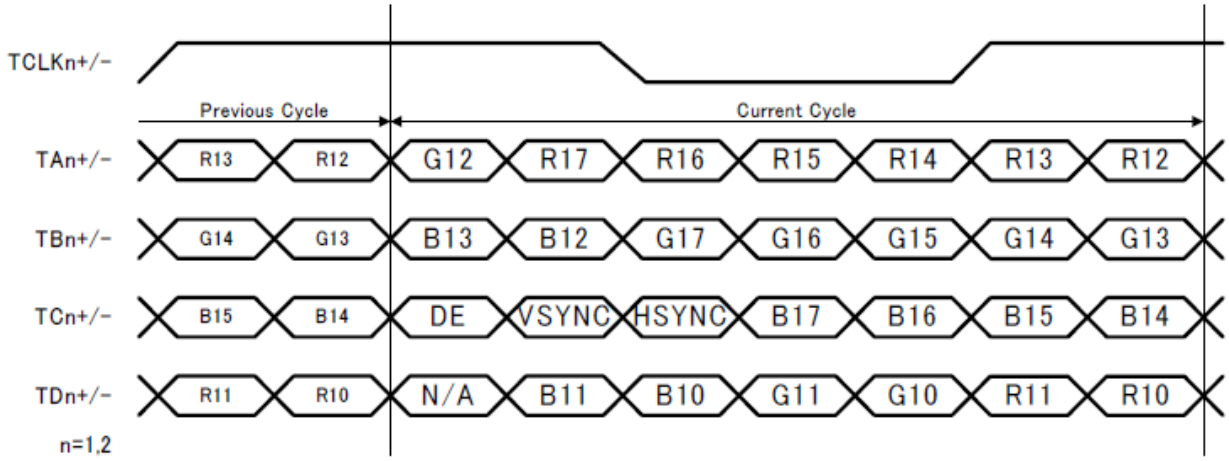


2) Single In- Single Out Mode (MODE=H)

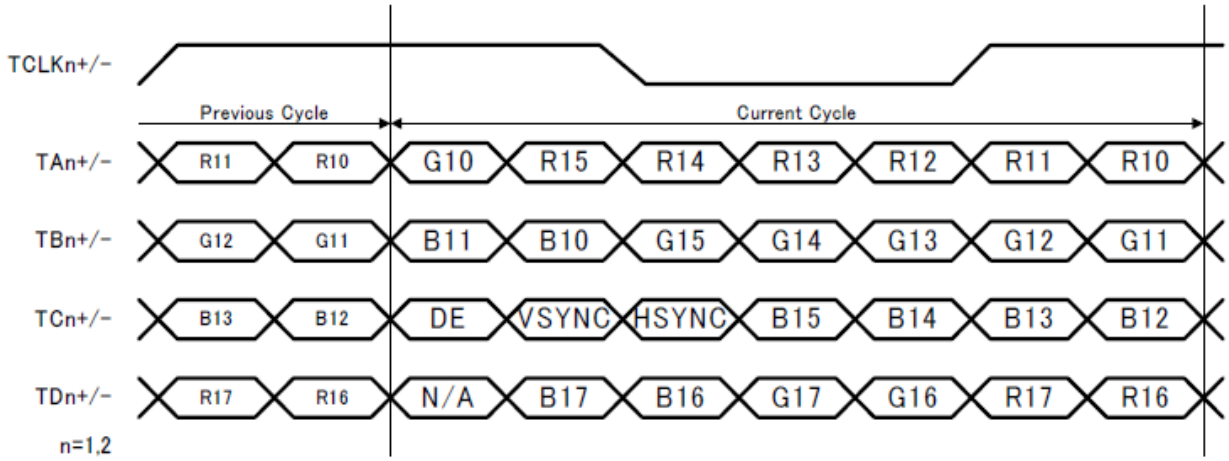


5. LVDS Data Mapping

1) for 8 bit mode (6B/8B=L)

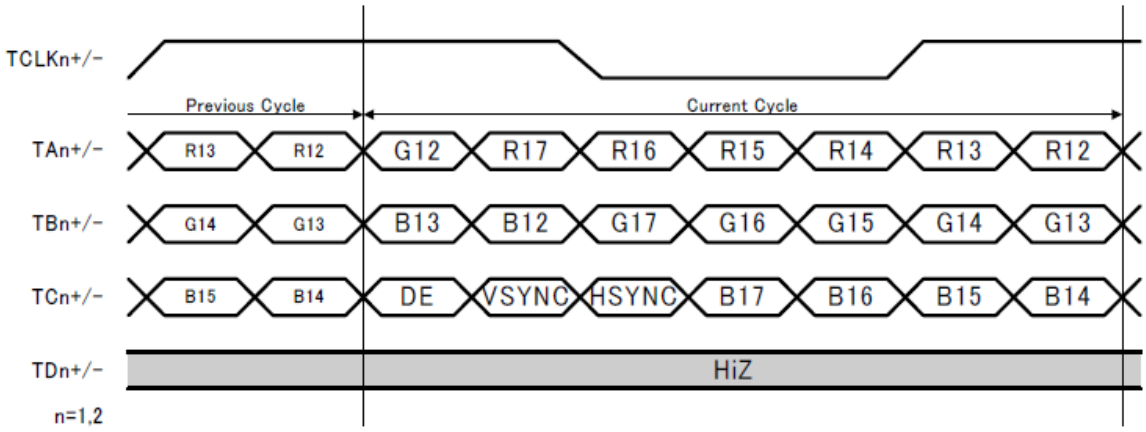


(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)

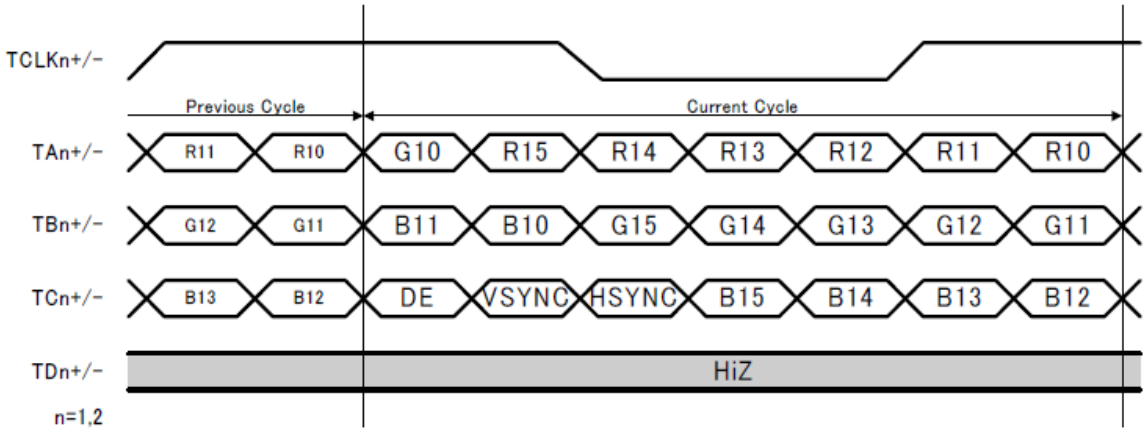


(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

2) for 6 bit mode (6B/8B=H)



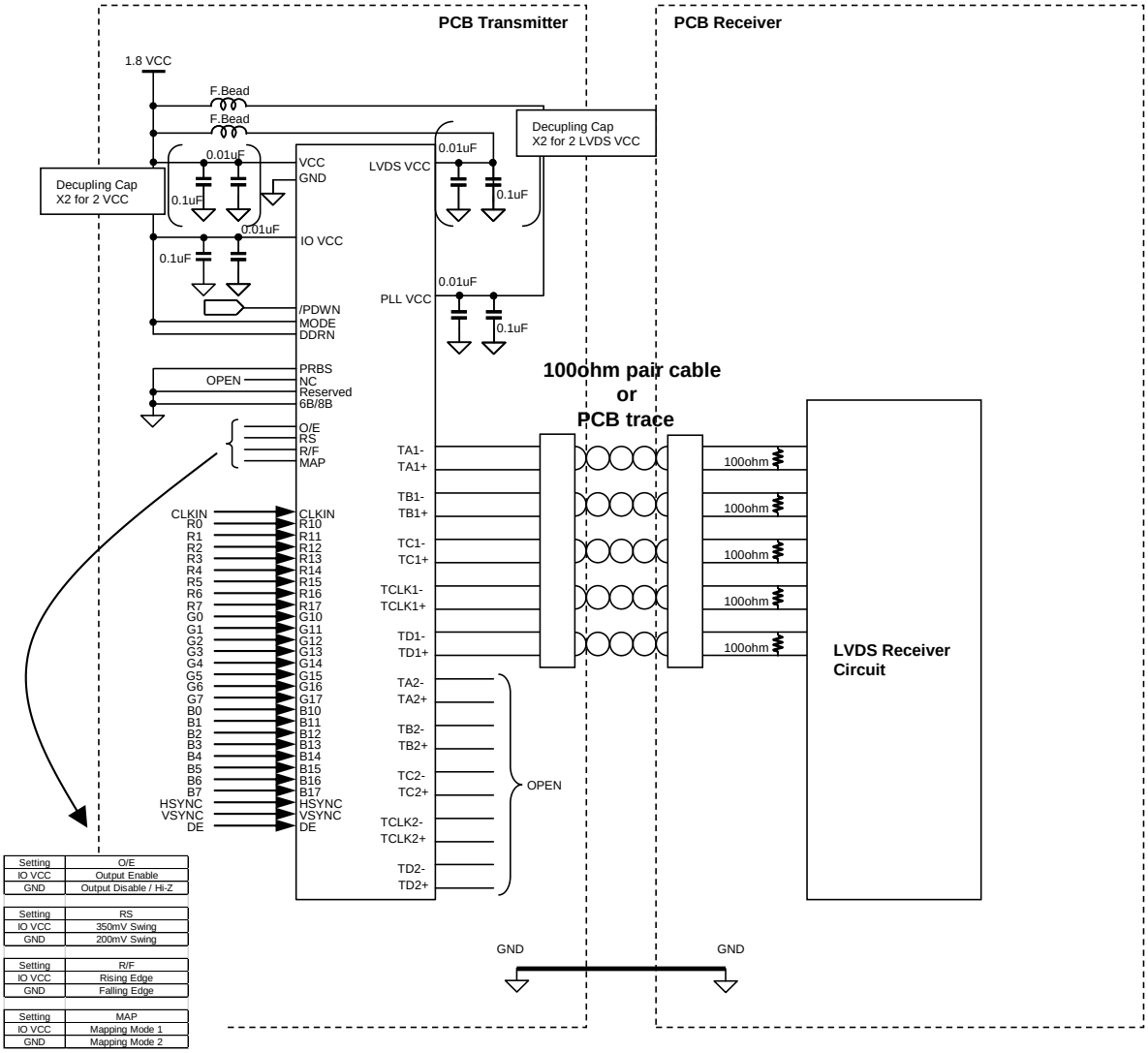
(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

6. Example of System Diagram

1) Single In–Single Out / 8bit 1.8V COMS/TTL Input



Setting	O/E
IO VCC	Output Enable
GND	Output Disable / Hi-Z

Setting	RS
IO VCC	350mV Swing
GND	200mV Swing

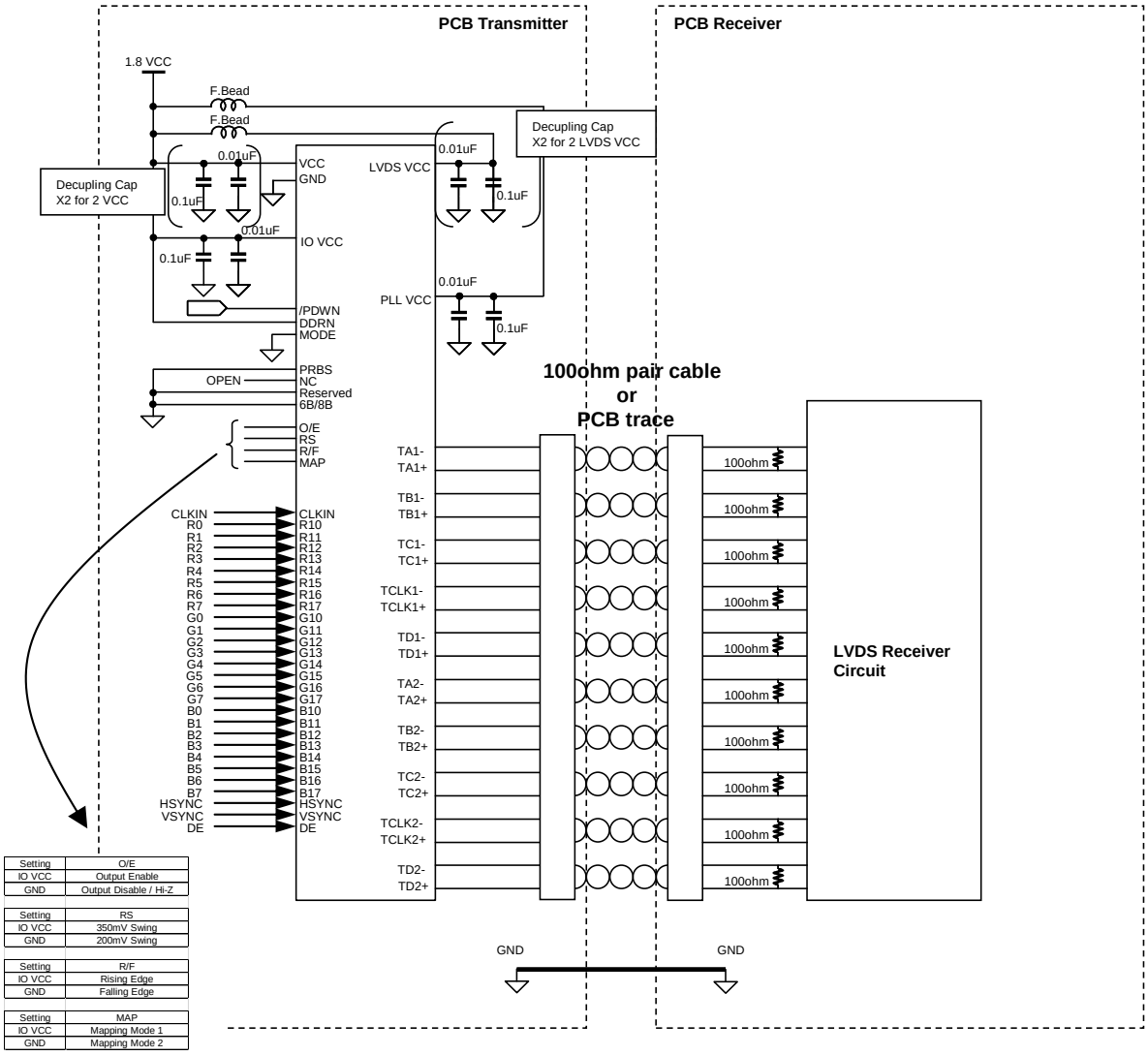
Setting	R/F
IO VCC	Rising Edge
GND	Falling Edge

Setting	MAP
IO VCC	Mapping Mode 1
GND	Mapping Mode 2

Note :

- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.

2) Single In –Dual Out / 8bit 1.8V COMS/TTL Input
DDR(Double Edge input) function disable.



Setting	O/E
IO VCC	Output Enable
GND	Output Disable / Hi-Z

Setting	RS
IO VCC	350mV Swing
GND	200mV Swing

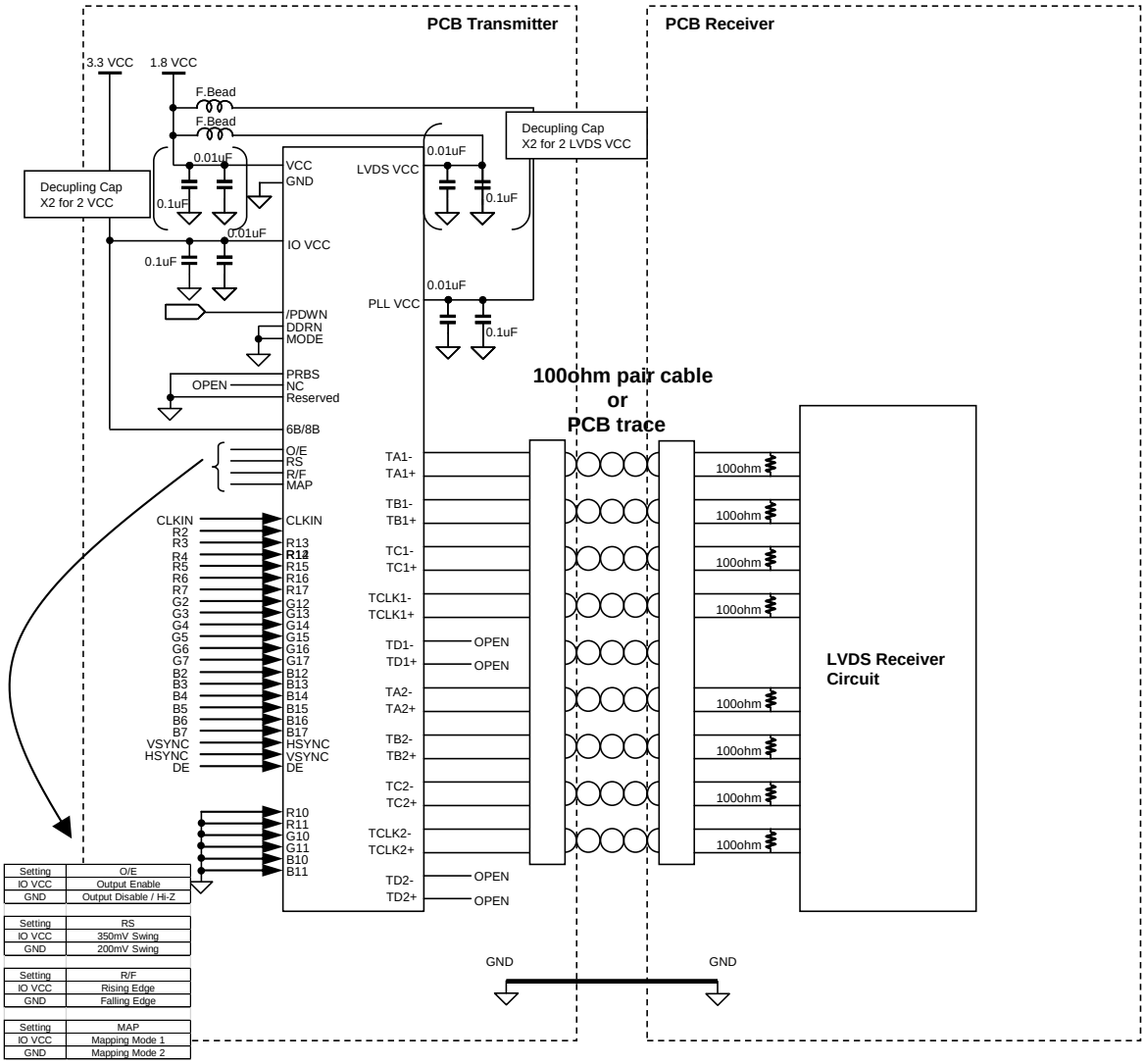
Setting	R/F
IO VCC	Rising Edge
GND	Falling Edge

Setting	MAP
IO VCC	Mapping Mode 1
GND	Mapping Mode 2

Note :

- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.

3) Single In –Dual Out / 3.3V 6bit COMS/TTL Input
DDR(Double Edge input) function enable



Note :

- O/E, RS, R/F, MAP : Please select IOVCC level or GND level, it depends on your operation.
- Connect each Board GND
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.

7. Note

7.1) Cable Connection and Disconnection

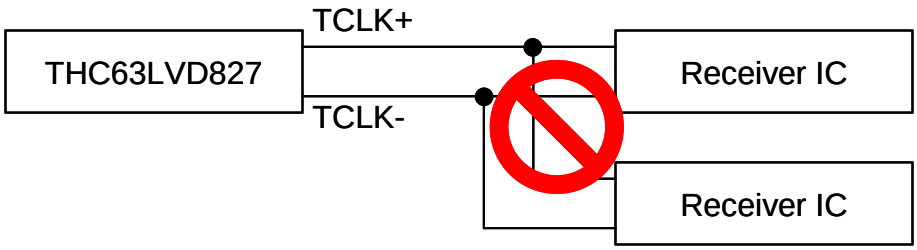
Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

7.2) GND Connection

Connect the each GND of the Board which THC63LVDM83E and Receiver on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

7.3) Multi Drop Connection

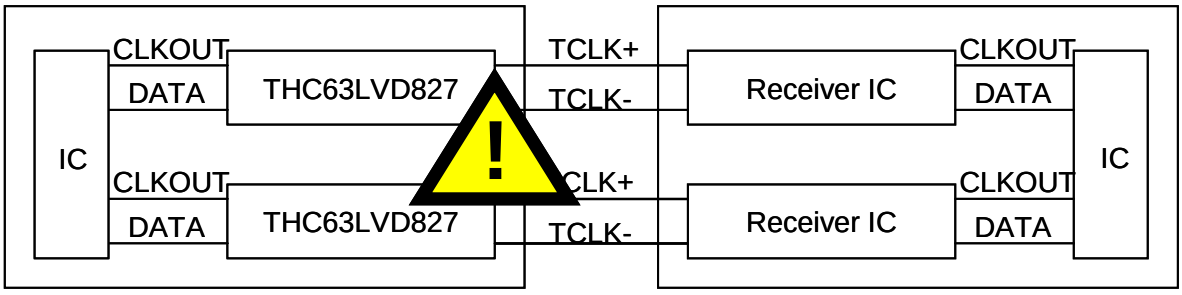
Multi drop connection is not recommended.

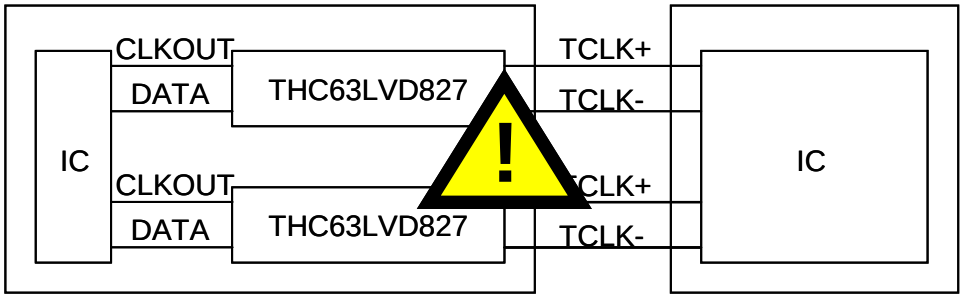


7.3) Asynchronous use

Asynchronous uses such as following systems are not recommended. If it's not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

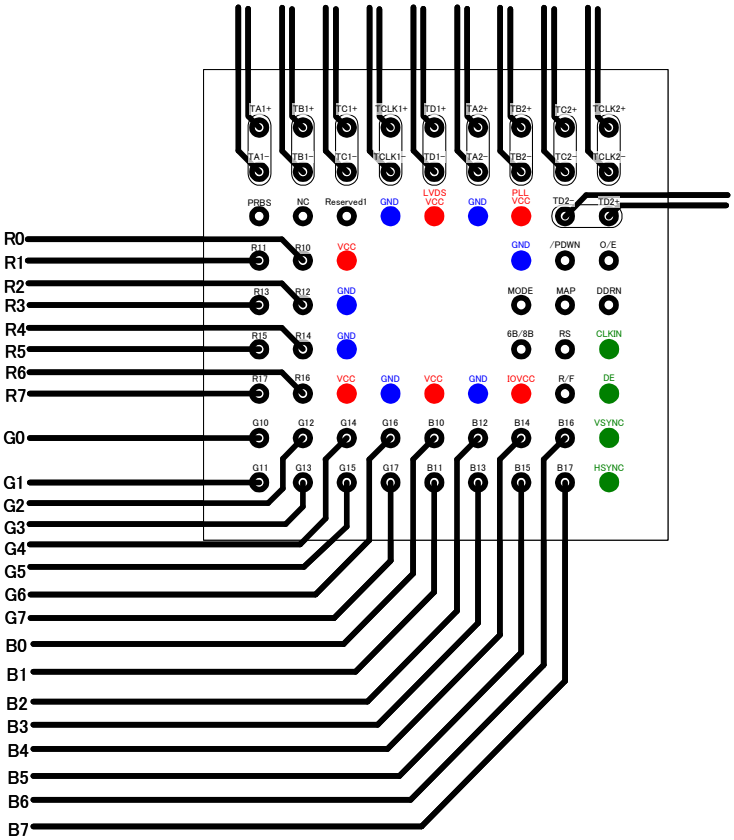




8. Trace Example for BGA

TOP VIEW

	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	PRBS	NC	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	C
D	R11	R10	LVDS VCC				GND	/PWDN	O/E	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B/8B	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	IO VCC	R/F	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	



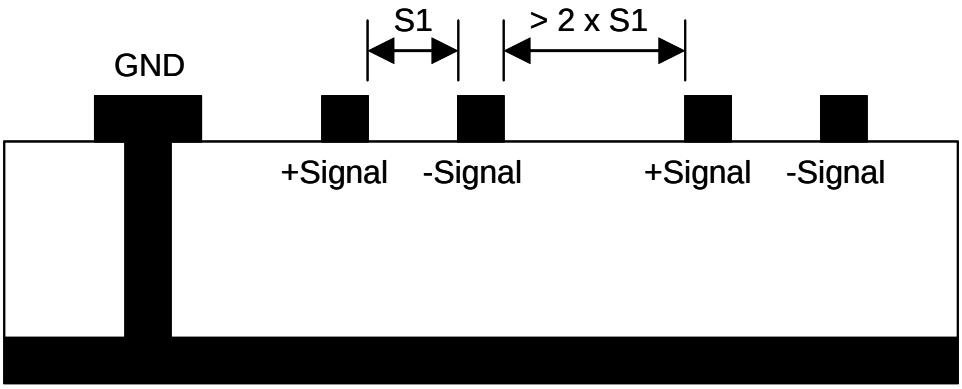
9. PCB Design Guide Line

General Guideline

- Use 4 layers PCB (minimum).
- Locate by-pass capacitors adjacent close to the device pins to a maximum extent.
- Make the loop minimum which is consist of Power line and GND line.
- Use large GND plane.
- Separate VDD power supply for each block via ferrite bead.

LVDS Trace

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector and cable) should be well balanced. (Keep all these differential impedance and the length of media as same as possible)
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as possible.
- Avoid 90 degree bends and sharp angles.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, cable and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place terminal resistor close to the Receiver pins to a maximum extent.
- To place common mode choke coil is desired for EMI reduction.



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