Application Note	*THCV242_RegisterMap_Rev.2.00_E*

THCV242 Register Map

Contents

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Register Map

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0000	[7:0]	reserved	8	-	-	-
0x0001	[7:1]	reserved	7	-	-	-
	[0]	R_SLINK_RST	1	W	Sub-Link Soft Reset 1: Reset 0x0001[0] Sub-Link reset does not includes 2-wire slave controller so that 0x0001[0] reset write access does not cause 2-wire slave abort and reaction to 2-wire master is normal ACK. Function is a little different from 0x1701[1].	-
0x0002	[7:0]	reserved	8	-	-	-
0x0003	[7:0]	reserved	8	-	-	-
0x0004	[7:3]	reserved	5	-	-	-
	[2:0]	R_SLINK_MODE	3	RW	Sub-Link basic protocol setting as Sub-Link Master 1: 2-wire Set&Trigger (Normal) mode1 3: 2-wire Pass Through mode1 0,2,4,5,6,7: Reserved	3'd1
0x0005	[7:0]	reserved	8	-	-	-
0x0006	[7:0]	reserved	8	-	-	-
0x0007	[7:0]	reserved	8	-	-	-
0x0008	[7:1]	reserved	7	-	-	-
	[0]	R_CKSUM_EN	1	RW	Internal Register AutoCheckSum Enable 0:Disable 1:Enable	1'b0
0x0009	[7:0]	R_CKSUM_TIM	8	RW	Internal Register AutoCheckSum check interval =1024×64×(R_CKSUM_TIM<7:0>+1) × tOSC	8'd19
0x000A	[7:0]	R_CKSUM_VAL	8	RW	Internal Register AutoCheckSum expected target value	8'd0
0x000B	[7:0]	R_CKSUM_RVAL	8	R	Internal Register AutoCheckSum read value	-
0x000C	[7:0]	reserved	8	-	-	-
0x000D	[7:0]	reserved	8	-	-	-
0x000E	[7:0]	reserved	8	-	-	-
0x000F	[7:0]	reserved	8	-	-	-
0x0010	[7:4]	R_SLINK_EN	4	RW	Sub-Link Enable [7] Reserved [6] Reserved [5] 0:Lane1 Disable, 1:Lane1 Enable [4] 0:Lane0 Disable, 1:Lane0 Enable	4'd0
	[3:0]	R_SLINK_POL_EN	4	RW	Sub-Link Polling Enable [3] Reserved [2] Reserved [1] 0:Lane1 Disable, 1:Lane1 Enable [0] 0:Lane0 Disable, 1:Lane0 Enable	4'hF
0x0011	[7:4]	R_SLINK_SSR_EN	4	RW	Sub-Link SSR Enable [7] Reserved [6] Reserved [5] 0:Lane1 Disable, 1:Lane1 Enable [4] 0:Lane0 Disable, 1:Lane0 Enable	4'hF
	[3:0]	R_SLINK_WD_EN	4	RW	Sub-Link WDT Enable [3] Reserved [2] Reserved [1] 0:Lane1 Disable, 1:Lane1 Enable [0] 0:Lane0 Disable, 1:Lane0 Enable	4'hF
0x0012	[7:0]	reserved	8	-	-	-
0x0013	[7:0]	reserved	8	-	-	-
0x0014	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0015	[7:5]	reserved	3	-	-	-
	[4]	R_SLINK_PHASE_EN	1	RW	Sub-Link Phase Shift Enable 0:Disable 1:Enable, Sub-Link phase of each lanes are shifted as below lane1 offset from lane0: 4×CLK_I	1'b0
	[3:1]	reserved	3	-	-	-
	[0]	R_SLINK_POL_CPY_EN	1	RW	Sub-Link Polling Copy Distribution at 2-wire mode1 (R_SLINK_MODE[1:0]=2'd1) 0:Disable, GPI[1:0] is sent to lane0. GPI[3:2] is sent to Lane1. 1:Enable, GPI[1:0] is copied to all Sub-Link Lanes	1'b0
0x0016	[7:6]	reserved	2	-	-	-
	[5:4]	R_POL_TIM_CLR_EN	2	RW	Polling Timer Clear/Mask Enable 0:Disable 1:Polling Timer Clear by GPI mode Enable 2:Polling Timer Mask by GPI mode Enable 3:Disable	2'd0
	[3]	reserved	1	-	-	-
	[2:0]	R_GPI_TRG_SEL	3	RW	Polling Timer Clear/Mask GPI select 0:GPI0、1:GPI1、2:GPI2、3:GPI3、4:GPI4、5:GPI5、6:GPI6、7:GPI7 *Only 0and1 are available at 2-wire mode1 (R_SLINK_MODE[1:0]=2'd1)	3'd0
0x0017	[7:6]	R_RES_GP7_LN_SEL	2	RW	GPIO7 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[5:4]	R_RES_GP6_LN_SEL	2	RW	GPIO6 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[3:2]	R_RES_GP5_LN_SEL	2	RW	GPIO5 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[1:0]	R_RES_GP4_LN_SEL	2	RW	GPIO4 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
0x0018	[7:6]	R_RES_GP3_LN_SEL	2	RW	GPIO3 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[5:4]	R_RES_GP2_LN_SEL	2	RW	GPIO2 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[3:2]	R_RES_GP1_LN_SEL	2	RW	GPIO1 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
	[1:0]	R_RES_GP0_LN_SEL	2	RW	GPIO0 Through GPO Mode counterpart GPI over Sub-Link lane assignment select 0:Lane 0, 1:Lane1, 2:Reserved, 3:Reserved	2'd0
0x0019	[7:4]	ReservedL	4	RW	Must be set 0	4'd0
	[3:2]	R_LOCKN_LN1_SEL	2	RW	Sub-Link Lane1 LOCKN/HTPDN scheme of releted Main-Link select 0:LOCKN1 1:LOCKN0 | LOCKN1 2:Reserved 3:1'b0 (Forced LOCKN/HTPDN=Low) *LOCKN1=LOCKN signal of V-by-One(R) HS Lane1=RX1P/RX1N *HTPDN of the same lane as above set LOCKN lane is used	2'd0
	[1:0]	R_LOCKN_LN0_SEL	2	RW	Sub-Link Lane0 LOCKN/HTPDN scheme of releted Main-Link select 0:LOCKN0 1:LOCKN0 | LOCKN1 2:Reserved 3:1'b0 (Forced LOCKN/HTPDN=Low) *LOCKN0=LOCKN signal of V-by-One(R) HS Lane0=RX0P/RX0N *HTPDN of the same lane as above set LOCKN lane is used	2'd0
0x001A	[7:5]	reserved	3	-	-	-
	[4]	R_SLINK_POL_OFSET_EN	1	RW	Sub-Link Polling Offset Enable 0:Disable 1:Enable, Polling time phase of each lanes are shifted as below lane1 offset from lane0: Sub-Link Poling interval x 1/4	1'b0
	[3:2]	reserved	2	-	-	-
	[1:0]	R_SLINK_POL_TIM_UP	2	RW	Sub-Link Polling interval setting (min. 0x018, about 20us)	2'd0
0x001B	[7:0]	R_SLINK_POL_TIM_DN	8	RW	Sub-Link Polling interval time=64×(256×R_SLINK_POL_TIM_UP<1:0> +R_SLINK_POL_TIM_DN<7:0>+1)×tOSC *No Polling when R_SLINK_POL_TIM_UP=0 and R_SLINK_POL_TIM_DN=0	8'd124
0x001C	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_SSR_TIM_UP	2	RW	Sub-Link SSR interval setting	2'd0
0x001D	[7:0]	R_SLINK_SSR_TIM_DN	8	RW	Sub-Link SSR interval time=64×(256×R_SLINK_SSR_TIM_UP<1:0> +R_SLINK_SSR_TIM_DN<7:0>+1)×tOSC *No SSR when R_SLINK_SSR_TIM_UP=0 and R_SLINK_SSR_TIM_DN=0	8'd249
0x001E	[7:2]	reserved	6	-	-	-
	[1:0]	R_SLINK_WD_TIM_UP	2	RW	Sub-Link WDT time parameter	2'd0
0x001F	[7:0]	R_SLINK_WD_TIM_DN	8	RW	Sub-Link WDT time =64×(256×R_SLINK_WD_TIM_UP<1:0> +R_SLINK_WD_TIM_DN<7:0>+1)×CLK_I	8'd187

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0020	[7:5]	reserved	3	-	-	-
	[4]	R_VS_PHASE_EN	1	RW	Internal VSYNC supply Phase Shift Enable (R_VS_MODE=2'd2) 0:Disable 1:Enable, Sub-Link phase of each lanes are shifted as below lane1 offset from lane0: R_VS_PHASE_WIDTH	1'b0
	[3:2]	reserved	2	-	-	-
	[1:0]	R_VS_MODE	2	RW	multiple camera synchronization Frame VSYNC supply mode setting 0: Disable 1: External VSYNC from EXTSYNC to remote camera supply 2: Internal VSYNC to remote camera supply and EXTSYNC pin output supply 3: Disable	2'd0
0x0021	[7:5]	reserved	3	-	-	-
	[4]	ReservedL	1	RW	Must be set 0	1'b0
	[3:1]	reserved	3	-	-	-
	[0]	R_VS_POL	1	RW	Internal VSYNC supply polarity (R_VS_MODE=2'd2) 0: Active Low negative polarity at Vertical blanking pulse 1: Active High positive polarity at Vertical blanking pulse	1'b0
0x0022	[7]	reserved	1	-	-	-
	[6:4]	R_VS_GPI_SEL	3	RW	Frame VSYNC supply mode Sub-Link GPI assignment bit on applied Sub-Link port 0:GPI0、1:GPI1、2:GPI2、3:GPI3、4:GPI4、5:GPI5、6:GPI6、7:GPI7 *only GPI0 or GPI1 are available for 2-wire Set&Trigger mode1 and 2-wire Pass Through mode1	3'd0
	[3:2]	ReservedL	2	RW	Must be set 0	2'd0
	[1:0]	R_VS_LANE_SEL	2	RW	Frame VSYNC supply target Sub-Link port [0]:Sub-Link port0; 0:no supply, 1:Frame VSYNC supply [1]:Sub-Link port1; 0:no supply, 1:Frame VSYNC supply	2'd0
0x0023	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_LINE_UP	4	RW	Internal VSYNC clock number / line by oscillator setting	4'd0
0x0024	[7:0]	R_VSOSC_LINE_DN	8	RW	Internal VSYNC clock number / line by oscillator = (256×R_VSOSC_LINE_UP<3:0> +R_VSOSC_LINE_DN<7:0>+1)×tOSC *Clock / line is 1 when R_VSOSC_LINE_UP=0 and R_VSOSC_LINE_DN=0	8'd15
0x0025	[7:0]	R_VSOSC_WIDTH	8	RW	Internal VSYNC pulse width line number by oscillator setting Line Number = R_VSOSC_WIDTH + 1 (e.g. 0x0 for 1line)	8'd4
0x0026	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSOSC_TIM_UP	4	RW	Internal VSYNC pulse interval line number by oscillator setting	4'd0
0x0027	[7:0]	R_VSOSC_TIM_DN	8	RW	Internal VSYNC pulse interval line number by oscillator = (256×R_VSOSC_TIM_UP<3:0> +R_VSOSC_TIM_DN<7:0>+1)×tOSC *Interval line is 2 when R_VSOSC_TIM_UP=0 and R_VSOSC_TIM_DN=0	8'd15
0x0028	[7:2]	reserved	6	-	-	-
	[1:0]	R_VS_PCLK_SEL	2	RW	Internal VSYNC generation base pixel clock domain select 0: CLK_I from Main-Link Lane0 1: CLK_I from Main-Link Lane1 2: Reserved 3: Reserved	2'd0
0x0029	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_LINE_UP	4	RW	Internal VSYNC clock number / line by base pixel clock setting	4'd0
0x002A	[7:0]	R_VSP_LINE_DN	8	RW	Internal VSYNC clock number / line by base pixel clock = (256×R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)×CLK_I *Clock / line is 1 when R_VSP_LINE_UP=0 and R_VSP_LINE_DN=0 *For setting or reset of this register, R_VS_MODE is supposed to be Disable	8'd15
0x002B	[7:0]	R_VSP_WIDTH	8	RW	Internal VSYNC pulse width line number by base pixel clock setting Line Number = R_VSP_WIDTH + 1 (e.g. 0x0 for 1line) *For setting or reset of this register, R_VS_MODE is supposed to be Disable	8'd4
0x002C	[7:4]	reserved	4	-	-	-
	[3:0]	R_VSP_TIM_UP	4	RW	Internal VSYNC pulse interval line number setting	4'd0
0x002D	[7:0]	R_VSP_TIM_DN	8	RW	Internal VSYNC pulse interval line number = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) Internal VSYNC pulse interval frame period by base pixel clock = (256×R_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) x (256×R_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)×CLK_I *Interval line is 2 when R_VSP_TIM_UP=0 and R_VSP_TIM_DN=0 *For setting or reset of this register, R_VS_MODE is supposed to be Disable	8'd15
0x002E	[7:0]	R_VS_PHASE_WIDTH	8	RW	VSYNC Phase shift difference = =16×R_VS_PHASE_WIDTH<7:0>×CLK_I *Phase shift difference is 16 xCLK_I as exception when R_VS_PHASE_WIDTH=0 *For setting or reset of this register, R_VS_PHASE_EN is supposed to be Disable	8'd1
0x002F	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0030	[7:0]	R_2WIRE_SADR	8	RW	2WIRE slave device address setting [7]2WIRE slave device address control 0: 2WIRE slv device addr. is set by AIN<1:0> pin 1: 2WIRE slv device addr. is set by following register [6:0] [6:0]2WIRE slave device address value for register control	8'd0
0x0031	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIREPT_MODE	2	RW	2WIRE Pass Through mode setting [1]Pass Through processing protocol on Sub-Link Slave 0:Reserved 1:Divided write & Divided read** (available with 2-wire Pass Through mode1) **:Transaction address and data Byte number is set as R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE. [0]Pass Through 2WIRE device addrress processing 0:Address rename (rule as R_2WIREPT1_PASS_ADRxy0/1. x is Lane0or1, y=<3:0>) 1:All Through (exception definition of address to ignore as R_2WIREPT2_NOPASS_ADRxz. x is Lane0or1, z=<7:0>)	2'd0
0x0032	[7]	reserved	1	-	-	-
	[6:4]	R_2WIREPT_WA_BYTE	3	RW	2WIRE Pass Through Divided write/read Sub-Address (Word Address) Byte number setting, being active at R_2WIREPT_MODE[1]=1 Byte Number = R_2WIREPT_WA_BYTE + 1 (e.g. 0x1 for 2Byte Sub-Address) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < 14 is required.	3'd0
	[3:0]	R_2WIREPT_DATA_BYTE	4	RW	2WIRE Pass Through Divided write/read data Byte number per one transaction setting, being active at R_2WIREPT_MODE[1]=1 Byte Number = R_2WIREPT_DATA_BYTE + 1 (e.g. 0x2 for 3Byte per transaction) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < 14 is required.	4'd0
0x0033	[7:0]	reserved	8	-	-	-
0x0034	[7:0]	reserved	8	-	-	-
0x0035	[7:0]	reserved	8	-	-	-
0x0036	[7:0]	reserved	8	-	-	-
0x0037	[7:0]	reserved	8	-	-	-
0x0038	[7:0]	reserved	8	-	-	-
0x0039	[7:0]	reserved	8	-	-	-
0x003A	[7:0]	reserved	8	-	-	-
0x003B	[7:5]	reserved	3	-	-	-
	[4]	R_2WIRE_WD_EN	1	RW	2WIRE WDT Enable 0:Disable 1:Enable	1'b1
	[3:1]	reserved	3	-	-	-
	[0]	R_2WIRE_WD_OFFSET	1	RW	2WIRE_WDT_OffsetTime 1:11'd2047 0:11'd1023	1'd1
0x003C	[7:0]	R_2WIRE_WD_TIM	8	RW	2WIRE WDT_time=64×{R_2WIRE_WD_TIM<7:0>+1}×{2WIRE_WDT_OffsetTime}×tOSC	8'd255
0x003D	[7:0]	reserved	8	-	-	-
0x003E	[7:0]	reserved	8	-	-	-
0x003F	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0040	[7:0]	R_2WIREPT1_PASS_ADR000	8	RW	2WIRE Pass Through received "before rename" address for Lane0 #0, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0041	[7:0]	R_2WIREPT1_PASS_ADR001	8	RW	2WIRE Pass Through "after renamed" address to send for Lane0 #0, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0042	[7:0]	R_2WIREPT1_PASS_ADR010	8	RW	2WIRE Pass Through received "before rename" address for Lane0 #1, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0043	[7:0]	R_2WIREPT1_PASS_ADR011	8	RW	2WIRE Pass Through "after renamed" address to send for Lane0 #1, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0044	[7:0]	R_2WIREPT1_PASS_ADR020	8	RW	2WIRE Pass Through received "before rename" address for Lane0 #2, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0045	[7:0]	R_2WIREPT1_PASS_ADR021	8	RW	2WIRE Pass Through "after renamed" address to send for Lane0 #2, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0046	[7:0]	R_2WIREPT1_PASS_ADR030	8	RW	2WIRE Pass Through received "before rename" address for Lane0 #3, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0047	[7:0]	R_2WIREPT1_PASS_ADR031	8	RW	2WIRE Pass Through "after renamed" address to send for Lane0 #3, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0048	[7:0]	R_2WIREPT2_NOPASS_ADR00	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #0, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x0049	[7:0]	R_2WIREPT2_NOPASS_ADR01	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #1, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004A	[7:0]	R_2WIREPT2_NOPASS_ADR02	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #2, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004B	[7:0]	R_2WIREPT2_NOPASS_ADR03	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #3, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004C	[7:0]	R_2WIREPT2_NOPASS_ADR04	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #4, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004D	[7:0]	R_2WIREPT2_NOPASS_ADR05	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #5, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004E	[7:0]	R_2WIREPT2_NOPASS_ADR06	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #6, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x004F	[7:0]	R_2WIREPT2_NOPASS_ADR07	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane0 #7, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x0050	[7:0]	R_2WIREPT1_PASS_ADRIN0	8	RW	2WIRE Pass Through counterpart Sub-Link Slave internal access dedicated address for Lane0, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0051	[7:0]	reserved	8	-	-	-
0x0052	[7:0]	reserved	8	-	-	-
0x0053	[7:0]	reserved	8	-	-	-
0x0054	[7:0]	reserved	8	-	-	-
0x0055	[7:0]	reserved	8	-	-	-
0x0056	[7:0]	reserved	8	-	-	-
0x0057	[7:0]	reserved	8	-	-	-
0x0058	[7:0]	reserved	8	-	-	-
0x0059	[7:0]	reserved	8	-	-	-
0x005A	[7:0]	reserved	8	-	-	-
0x005B	[7:0]	reserved	8	-	-	-
0x005C	[7:0]	reserved	8	-	-	-
0x005D	[7:0]	reserved	8	-	-	-
0x005E	[7:0]	reserved	8	-	-	-
0x005F	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0060	[7:0]	R_2WIREPT1_PASS_ADR100	8	RW	2WIRE Pass Through received "before rename" address for Lane1 #0, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0061	[7:0]	R_2WIREPT1_PASS_ADR101	8	RW	2WIRE Pass Through "after renamed" address to send for Lane1 #0, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0062	[7:0]	R_2WIREPT1_PASS_ADR110	8	RW	2WIRE Pass Through received "before rename" address for Lane1 #1, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0063	[7:0]	R_2WIREPT1_PASS_ADR111	8	RW	2WIRE Pass Through "after renamed" address to send for Lane1 #1, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0064	[7:0]	R_2WIREPT1_PASS_ADR120	8	RW	2WIRE Pass Through received "before rename" address for Lane1 #2, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0065	[7:0]	R_2WIREPT1_PASS_ADR121	8	RW	2WIRE Pass Through "after renamed" address to send for Lane1 #2, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0066	[7:0]	R_2WIREPT1_PASS_ADR130	8	RW	2WIRE Pass Through received "before rename" address for Lane1 #3, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0067	[7:0]	R_2WIREPT1_PASS_ADR131	8	RW	2WIRE Pass Through "after renamed" address to send for Lane1 #3, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0068	[7:0]	R_2WIREPT2_NOPASS_ADR10	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #0, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x0069	[7:0]	R_2WIREPT2_NOPASS_ADR11	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #1, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006A	[7:0]	R_2WIREPT2_NOPASS_ADR12	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #2, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006B	[7:0]	R_2WIREPT2_NOPASS_ADR13	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #3, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006C	[7:0]	R_2WIREPT2_NOPASS_ADR14	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #4, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006D	[7:0]	R_2WIREPT2_NOPASS_ADR15	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #5, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006E	[7:0]	R_2WIREPT2_NOPASS_ADR16	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #6, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x006F	[7:0]	R_2WIREPT2_NOPASS_ADR17	8	RW	2WIRE Pass Through ignore address /otherwise All Through fror Lane1 #7, being active only at R_2WIREPT_MODE[0]=1.	8'd0
0x0070	[7:0]	R_2WIREPT1_PASS_ADRIN1	8	RW	2WIRE Pass Through counterpart Sub-Link Slave internal access dedicated address for Lane1, being active only at R_2WIREPT_MODE[0]=0.	8'd0
0x0071	[7:0]	reserved	8	-	-	-
0x0072	[7:0]	reserved	8	-	-	-
0x0073	[7:0]	reserved	8	-	-	-
0x0074	[7:0]	reserved	8	-	-	-
0x0075	[7:0]	reserved	8	-	-	-
0x0076	[7:0]	reserved	8	-	-	-
0x0077	[7:0]	reserved	8	-	-	-
0x0078	[7:0]	reserved	8	-	-	-
0x0079	[7:0]	reserved	8	-	-	-
0x007A	[7:0]	reserved	8	-	-	-
0x007B	[7:0]	reserved	8	-	-	-
0x007C	[7:0]	reserved	8	-	-	-
0x007D	[7:0]	reserved	8	-	-	-
0x007E	[7:0]	reserved	8	-	-	-
0x007F	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0080	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0081	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0082	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0083	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0084	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0085	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0086	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0087	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0088	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0089	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008A	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008B	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008C	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008D	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008E	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x008F	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0090	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x0091	[7:0]	reserved	8	-	-	-
0x0092	[7:0]	reserved	8	-	-	-
0x0093	[7:0]	reserved	8	-	-	-
0x0094	[7:0]	reserved	8	-	-	-
0x0095	[7:0]	reserved	8	-	-	-
0x0096	[7:0]	reserved	8	-	-	-
0x0097	[7:0]	reserved	8	-	-	-
0x0098	[7:0]	reserved	8	-	-	-
0x0099	[7:0]	reserved	8	-	-	-
0x009A	[7:0]	reserved	8	-	-	-
0x009B	[7:0]	reserved	8	-	-	-
0x009C	[7:0]	reserved	8	-	-	-
0x009D	[7:0]	reserved	8	-	-	-
0x009E	[7:0]	reserved	8	-	-	-
0x009F	[7:0]	reserved	8	-	-	-
0x00A0	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A1	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A2	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A3	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A4	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A5	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A6	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A7	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A8	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00A9	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AA	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AB	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AC	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AD	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AE	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00AF	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00B0	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x00B1	[7:0]	reserved	8	-	-	-
0x00B2	[7:0]	reserved	8	-	-	-
0x00B3	[7:0]	reserved	8	-	-	-
0x00B4	[7:0]	reserved	8	-	-	-
0x00B5	[7:0]	reserved	8	-	-	-
0x00B6	[7:0]	reserved	8	-	-	-
0x00B7	[7:0]	reserved	8	-	-	-
0x00B8	[7:0]	reserved	8	-	-	-
0x00B9	[7:0]	reserved	8	-	-	-
0x00BA	[7:0]	reserved	8	-	-	-
0x00BB	[7:0]	reserved	8	-	-	-
0x00BC	[7:0]	reserved	8	-	-	-
0x00BD	[7:0]	reserved	8	-	-	-
0x00BE	[7:0]	reserved	8	-	-	-
0x00BF	[7:0]	reserved	8	-	-	-
0x00C0	[7:0]	reserved	8	-	-	-
0x00C1	[7:0]	reserved	8	-	-	-
0x00C2	[7:0]	reserved	8	-	-	-
0x00C3	[7:0]	reserved	8	-	-	-
0x00C4	[7:0]	reserved	8	-	-	-
0x00C5	[7:0]	reserved	8	-	-	-
0x00C6	[7:0]	reserved	8	-	-	-
0x00C7	[7:0]	reserved	8	-	-	-
0x00C8	[7:0]	reserved	8	-	-	-
0x00C9	[7:0]	reserved	8	-	-	-
0x00CA	[7:0]	reserved	8	-	-	-
0x00CB	[7:0]	reserved	8	-	-	-
0x00CC	[7:0]	reserved	8	-	-	-
0x00CD	[7:0]	reserved	8	-	-	-
0x00CE	[7:0]	reserved	8	-	-	-
0x00CF	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x00D0	[7:0]	R_2WIRE_DATA0	8	RW	2-wire serial I/F remote write/read data #0	8'd0
0x00D1	[7:0]	R_2WIRE_DATA1	8	RW	2-wire serial I/F remote write/read data #1	8'd0
0x00D2	[7:0]	R_2WIRE_DATA2	8	RW	2-wire serial I/F remote write/read data #2	8'd0
0x00D3	[7:0]	R_2WIRE_DATA3	8	RW	2-wire serial I/F remote write/read data #3	8'd0
0x00D4	[7:0]	R_2WIRE_DATA4	8	RW	2-wire serial I/F remote write/read data #4	8'd0
0x00D5	[7:0]	R_2WIRE_DATA5	8	RW	2-wire serial I/F remote write/read data #5	8'd0
0x00D6	[7:0]	R_2WIRE_DATA6	8	RW	2-wire serial I/F remote write/read data #6	8'd0
0x00D7	[7:0]	R_2WIRE_DATA7	8	RW	2-wire serial I/F remote write/read data #7	8'd0
0x00D8	[7:0]	R_2WIRE_DATA8	8	RW	2-wire serial I/F remote write/read data #8	8'd0
0x00D9	[7:0]	R_2WIRE_DATA9	8	RW	2-wire serial I/F remote write/read data #9	8'd0
0x00DA	[7:0]	R_2WIRE_DATA10	8	RW	2-wire serial I/F remote write/read data #10	8'd0
0x00DB	[7:0]	R_2WIRE_DATA11	8	RW	2-wire serial I/F remote write/read data #11	8'd0
0x00DC	[7:0]	R_2WIRE_DATA12	8	RW	2-wire serial I/F remote write/read data #12	8'd0
0x00DD	[7:0]	R_2WIRE_DATA13	8	RW	2-wire serial I/F remote write/read data #13	8'd0
0x00DE	[7:0]	R_2WIRE_DATA14	8	RW	2-wire serial I/F remote write/read data #14	8'd0
0x00DF	[7:0]	R_2WIRE_DATA15	8	RW	2-wire serial I/F remote write/read data #15	8'd0
0x00E0	[7:1]	R_2WIRE_DEVADR	7	RW	2-wire serial I/F remote access target device address. if target=self addr.; access to Sub-Link Slave inside register, else; access to remote side 2-wire serial Slave devices externally connected to Sub-Link slave	7'h00
	[0]	R_2WIRE_WR	1	RW	2-wire serial I/F remote access write or read select 0:Write 1:Read	1'b0
0x00E1	[7]	reserved	1	-	-	-
	[6:4]	R_2WIRE_WADR_BYTE	3	RW	2-wire serial I/F remote device's Sub Address (Word Address, register address) Byte width select. address Byte width=R_2WIRE_WADR_BYTE<2:0>+1 0 : 1Byte= 8bit Sub addr.(register addr.) 1 : 2Byte=16bit Sub addr.(register addr.) 4 : 5Byte=40bit Sub addr.(register addr.), etc.	3'd0
	[3:0]	R_2WIRE_DATA_BYTE	4	RW	2-wire serial I/F remote access data Byte number Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3byte burst) [write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd16 [read rule] R_2WIRE_DATA_BYTE<'d16	4'd0
0x00E2	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_CLKSEN	1	RW	2-wire serial I/F local response clock stretching Enable 0: Sub-Link Master (2-wire slave) No clock stretching 1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode forces clock stretching Enable	1'b0
0x00E3	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIRE_RD_LANE_SEL	2	RW	Sub-Link transaction read lane select 0: Lane0 Sub-Link read 1: Lane1 Sub-Link read 2,3: Reserved	2'd0
0x00E4	[7:2]	reserved	4	-	-	-
	[1:0]	R_2WIRE_WR_LANE_SEL	4	RW	Sub-Link transaction write lane select [1] 0: Lane1 Disable, 1:Lane1 Enable [0] 0: Lane0 Disable, 1:Lane0 Enable *Only active when R_SLINK_MODE=4'd0 or 4'd1	4'hF
0x00E5	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_START	1	W	2-wire serial I/F remote access start trigger	-
0x00E6	[7:0]	reserved	8	-	-	-
0x00E7	[7:0]	reserved	8	-	-	-
0x00E8	[7:0]	reserved	8	-	-	-
0x00E9	[7:0]	reserved	8	-	-	-
0x00EA	[7:0]	reserved	8	-	-	-
0x00EB	[7:0]	reserved	8	-	-	-
0x00EC	[7:0]	reserved	8	-	-	-
0x00ED	[7:0]	reserved	8	-	-	-
0x00EE	[7:0]	reserved	8	-	-	-
0x00EF	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x00F0	[7:0]	reserved	6	-	-	-
	[1:0]	R_SLINK_FBET_LANE_SEL	2	RW	Sub-Link FieldBET Lane select 0: Sub-Link Lane0 Sub-Link FieldBET 1: Sub-Link Lane1 Sub-Link FieldBET 2: Reserved 3: Reserved	2'd0
0x00F1	[7:1]	reserved	7	-	-	-
	[0]	R_SLINK_FBETERR_CLR	1	W	Sub-Link FieldBET error count clear 1: Clear	-
0x00F2	[7:0]	R_SLINK_FBETERR_NUM_UP	8	R	Sub-Link FieldBET error count parameter	-
0x00F3	[7:0]	R_SLINK_FBETERR_NUM_DN	8	R	Sub-Link FieldBET error count =256×R_SLINK_FBETERR_NUM_UP<7:0> ＋R_SLINK_FBETERR_NUM_DN<7:0>	-
0x00F4	[7:0]	reserved	8	-	-	-
0x00F5	[7:0]	reserved	8	-	-	-
0x00F6	[7:0]	reserved	8	-	-	-
0x00F7	[7:0]	reserved	8	-	-	-
0x00F8	[7:0]	reserved	8	-	-	-
0x00F9	[7:0]	reserved	8	-	-	-
0x00FA	[7:0]	reserved	8	-	-	-
0x00FB	[7:0]	reserved	8	-	-	-
0x00FC	[7:0]	reserved	8	-	-	-
0x00FD	[7:0]	reserved	8	-	-	-
0x00FE	[7:0]	reserved	8	-	-	-
0x00FF	[7:0]	reserved	8	-	-	-

Addr(h)	bit	Register Name	width	R/W	Description	Default
0x0100	[7:0]	R_TUNING_ENABLE1	8	RW	Tuning register access Enable (1/2) 0x03: Enable others:Disable	8'd0
0x0101	[7]	ReservedL	1	RW	Must be set 0	1'b0
	[6]	ReservedL	1	RW	Must be set 0	1'b0
	[5]	R_BDCZ_HYS1	1	RW	Sub-Link Lane1 Hysterisis level select / 0:50mV, 1:175mV	1'b0
	[4]	R_BDCZ_HYS0	1	RW	Sub-Link Lane0 Hysterisis level select / 0:50mV, 1:175mV	1'b0
	[3]	ReservedH	1	RW	Must be set 1	1'b1
	[2]	ReservedH	1	RW	Must be set 1	1'b1
	[1]	R_BDCZ_TERMEN1	1	RW	Sub-Link Lane1 Termination Enable / 0:Disable, 1:Enable	1'b1
	[0]	R_BDCZ_TERMEN0	1	RW	Sub-Link Lane0 Termination Enable / 0:Disable, 1:Enable	1'b1
0x0102	[7:6]	ReservedL	2	RW	Must be set 0	2'b00
	[5:4]	ReservedL	2	RW	Must be set 0	2'b00
	[3:2]	R_BDCZ_TERM_TX1	2	RW	Sub-Link Lane1 Tx Termination select (10=50ohm is typical) 11=Reserved, 10=50ohm, 01=100ohm, 00=200ohm	2'b00
	[1:0]	R_BDCZ_TERM_TX0	2	RW	Sub-Link Lane0 Tx Termination select (10=50ohm is typical) 11=Reserved, 10=50ohm, 01=100ohm, 00=200ohm	2'b00
0x0103	[7:6]	ReservedL	2	RW	Must be set 0	2'b00
	[5:4]	ReservedL	2	RW	Must be set 0	2'b00
	[3:2]	R_BDCZ_DRIVE_TX1	2	RW	Sub-Link Lane1 Tx Drive current select (10=12mA is typical) 11=Reserved, 10=12mA, 01=6mA, 00=3mA	2'b00
	[1:0]	R_BDCZ_DRIVE_TX0	2	RW	Sub-Link Lane0 Tx Drive current select (10=12mA is typical) 11=Reserved, 10=12mA, 01=6mA, 00=3mA	2'b00
0x0104	[7:6]	ReservedL	2	RW	Must be set 0	2'b00
	[5:4]	ReservedL	2	RW	Must be set 0	2'b00
	[3:2]	R_BDCZ_TERM_RX1	2	RW	Sub-Link Lane1 Rx Termination select (10=50ohm is typical) 11=Reserved, 10=50ohm, 01=100ohm, 00=200ohm	2'b00
	[1:0]	R_BDCZ_TERM_RX0	2	RW	Sub-Link Lane0 Rx Termination select (10=50ohm is typical) 11=Reserved, 10=50ohm, 01=100ohm, 00=200ohm	2'b00
0x0105	[7:6]	ReservedL	2	RW	Must be set 0	2'b00
	[5:4]	ReservedL	2	RW	Must be set 0	2'b00
	[3:2]	R_BDCZ_DRIVE_RX1	2	RW	Sub-Link Lane1 Rx Drive current select (10=12mA is typical) 11=Reserved, 10=12mA, 01=6mA, 00=3mA	2'b00
	[1:0]	R_BDCZ_DRIVE_RX0	2	RW	Sub-Link Lane0 Rx Drive current select (10=12mA is typical) 11=Reserved, 10=12mA, 01=6mA, 00=3mA	2'b00
0x0106	[7:0]	reserved	8	-	-	-
0x0107	[7:0]	reserved	8	-	-	-
0x0108	[7:0]	reserved	8	-	-	-
0x0109	[7:0]	ReservedX	8	RW	[Tuning register] must be left as default 0x09	8'd9
0x010A	[7:0]	R_SLINK_DATA_WIDTH	8	RW	[Tuning register] Sub-Link clock pattern unit period = R_SLINK_DATA_WIDTH<7:0>+1 must be set to 0x15 (default 0x0F is supposed to be changed)	8'h0F
0x010B	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x010C	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x010D	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x010E	[7:0]	ReservedL	8	RW	Must be set 0	8'd0
0x010F	[7:0]	R_TUNING_ENABLE2	8	RW	Tuning register access Enable (2/2) 0x25: Enable others:Disable	8'd0

Adr	bit	Register Name	width	R/W	init	Description
0x10 00	[7:1]	reserved	7	-	-	-
0x10 00	[0]	R_2WIRE_DS	1	R/W	1'b1	CMOS I/O Driveility for 2WIRE Pin (SCL/SDA and GPIO on Second 2WIRE Mode) 0:Normal Drive 1:Strong Drive
0x10 01	[7:4]	R_GPIO7_MODE	4	R/W	4'h0	GPIO7 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 01	[3:0]	R_GPIO6_MODE	4	R/W	4'h0	GPIO6 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 02	[7:4]	R_GPIO5_MODE	4	R/W	4'h0	GPIO5 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 02	[3:0]	R_GPIO4_MODE	4	R/W	4'h0	GPIO4 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 03	[7:4]	R_GPIO3_MODE	4	R/W	4'h0	GPIO3 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 03	[3:0]	R_GPIO2_MODE	4	R/W	4'h0	GPIO2 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved

Adr	bit	Register Name	width	R/W	init	Description
0x10 04	[7:4]	R_GPIO1_MODE	4	R/W	4'h0	GPIO1 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 04	[3:0]	R_GPIO0_MODE	4	R/W	4'h0	GPIO0 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7~F:Reserved
0x10 05	[7:4]	R_ERR1_MODE	4	R/W	4'h0	ERRR1 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3~F:Reserved
0x10 05	[3:0]	R_ERR0_MODE	4	R/W	4'h0	ERRR0 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3~F:Reserved
0x10 06	[7:4]	R_INT1_MODE	4	R/W	4'h0	INT1 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3~F:Reserved
0x10 06	[3:0]	R_INT0_MODE	4	R/W	4'h0	INT0 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3~F:Reserved
0x10 07	[7:4]	reserved	4	-	-	-
0x10 07	[3:0]	R_EXTSYNC_MODE	4	R/W	4'h0	EXTSYNC I/O Mode 0:Disable 1:Normal Mode (Controlled by Sub-Link Register) 2~F: Reserved

Adr	bit	Register Name	width	R/W	init	Description
0x10 08	[7:4]	R_FLT_GPIO7	4	R/W	4'h7	GPIO7 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 08	[3:0]	R_FLT_GPIO6	4	R/W	4'h7	GPIO6 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 09	[7:4]	R_FLT_GPIO5	4	R/W	4'h7	GPIO5 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 09	[3:0]	R_FLT_GPIO4	4	R/W	4'h7	GPIO4 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 0A	[7:4]	R_FLT_GPIO3	4	R/W	4'h7	GPIO3 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 0A	[3:0]	R_FLT_GPIO2	4	R/W	4'h7	GPIO2 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 0B	[7:4]	R_FLT_GPIO1	4	R/W	4'h7	GPIO1 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 0B	[3:0]	R_FLT_GPIO0	4	R/W	4'h7	GPIO0 I/O Filter Length 0: Filter Disable N: Filter Enable and Filter Length is N (unit is term of Oscillator Clock)
0x10 0C	[7:0]	R_ERR1_SEL	8	R/W	8'h0	ERR1 Pin Signal Select
0x10 0D	[7:0]	R_ERR0_SEL	8	R/W	8'h0	ERR0 Pin Signal Select
0x10 0E	[7:0]	reserved	8	-	-	-
0x10 0F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x10 10	[7:6]	R_MLNK_NHSEL0	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for LINK0) 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard mode 11 : Reserved
0x10 10	[5:4]	R_MLNK_COL0	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for LINK0) 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved
0x10 10	[3]	reserved	1	-	-	-
0x10 10	[2]	R_MLINK_AOCEN0	1	R/W	1'b0	V-by-One® AOC Enable (for LINK0) 0:Auto Offset Cancel Disable 1:Auto Offset Cancel Enable
0x10 10	[1]	ReservedL	1	R/W	1'b0	Must be set 0
0x10 10	[0]	R_MLINK_AEQEN0	1	R/W	1'b0	V-by-One® Adaptive Equalizer Setting (for LINK0) 0:Static Equalizer Mode (Register Control) 1:Adaptive Equalizer Mode
0x10 11	[7]	reserved	1	-	-	-
0x10 11	[6:4]	R_MLINK_LEQCTLC0	3	R/W	3'h0	V-by-One® Main-Link Equalizer strength Control setting (for LINK0) available when R_MLINK_AEQEN0=0 (static Equalizer Mode) 000: 8dB (informative) (the weakest) 001: 9dB (informative) 011: 10dB (informative) 010: 11dB (informative) 110: 12dB (informative) 111: 13dB (informative) 101: 14dB (informative) 100: 15dB (informative) (the strongest)
0x10 11	[3]	reserved	1	-	-	-
0x10 11	[2:0]	R_MLINK_LEQCTLR0	3	R/W	3'h0	V-by-One® Main-Link Equalizer baseline Raise setting (for LINK0) 000: 0dB (informative) (the lowest) 001: 1dB (informative) 011: 2dB (informative) 010: 3dB (informative) 110: 4dB (informative) 111: 5dB (informative) 101: 6dB (informative) 100: 7dB (informative) (the highest)
0x10 12	[7:5]	reserved	3	-	-	-
0x10 12	[4]	R_RGB565_ON_L0	1	R/W	1'b0	Main-Link Input Data Format Setting2 (This register could use only when R_VX1_LANE_FMT0=0x1) 0: RGB888 1: RGB565
0x10 12	[3:0]	R_VX1_LANE_FMT0	4	R/W	4'h0	Main-Link Input Data Format Setting 0: MPRF 1: RGBxxx 2,3,4,5,6: YUV422 (NormalYU1,NormalYU2,NormalYU3,DemuxYU1,DemuxYU2) 7,8,9: RAW8 (NormalR081,NormalR082,DemuxR081) 10,11,12: RAW10 (NormalR101,DemuxR101,DemuxR102) 13,14,15: RAW12 (NormalR121,DemuxR121,DemuxR122)
0x10 13	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0

Adr	bit	Register Name	width	R/W	init	Description
0x10 14	[7:6]	R_MLINK_NHSEL1	2	R/W	2'h2	V-by-One® Main-Link Mode Select (for LINK1) 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard mode 11 : Reserved
0x10 14	[5:4]	R_MLINK_COL1	2	R/W	2'h1	V-by-One® Main-Link Byte Mode Select (for LINK1) 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved
0x10 14	[3]	reserved	1	-	-	-
0x10 14	[2]	R_MLINK_AOCEN1	1	R/W	1'b0	V-by-One® AOC Enable (for LINK1) 0:Auto Offset Cancel Disable 1:Auto Offset Cancel Enable
0x10 14	[1]	ReservedL	1	R/W	1'b0	Must be set 0
0x10 14	[0]	R_MLINK_AEQEN1	1	R/W	1'b0	V-by-One® Adaptive Equalizer Setting (for LINK1) 0:Static Equalizer Mode (Register Control) 1:Adaptive Equalizer Mode
0x10 15	[7]	reserved	1	-	-	-
0x10 15	[6:4]	R_MLINK_LEQCTLC1	3	R/W	3'h0	V-by-One® Main-Link Equalizer strength Control setting (for LINK1) available when R_MLINK_AEQEN1=0 (static Equalizer Mode) 000: 8dB (informative) (the weakest) 001: 9dB (informative) 011: 10dB (informative) 010: 11dB (informative) 110: 12dB (informative) 111: 13dB (informative) 101: 14dB (informative) 100: 15dB (informative) (the strongest)
0x10 15	[3]	reserved	1	-	-	-
0x10 15	[2:0]	R_MLINK_LEQCTLR1	3	R/W	3'h0	V-by-One® Main-Link Equalizer baseline Raise setting (for LINK1) 000: 0dB (informative) (the lowest) 001: 1dB (informative) 011: 2dB (informative) 010: 3dB (informative) 110: 4dB (informative) 111: 5dB (informative) 101: 6dB (informative) 100: 7dB (informative) (the highest)
0x10 16	[7:0]	reserved	8	-	-	-
0x10 17	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x10 18	[7:0]	ReservedX	8	R/W	8'h90	Must be left as default 0x90
0x10 19	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x10 1A	[7:0]	reserved	8	-	-	-
0x10 1B	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x10 1C	[7:0]	ReservedX	8	R/W	8'h90	Must be left as default 0x90
0x10 1D	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x10 1E	[7:0]	reserved	8	-	-	-
0x10 1F	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0

Adr	bit	Register Name	width	R/W	init	Description
0x10 20	[7:5]	reserved	3	-	-	-
0x10 20	[4:0]	ReservedL	4	R/W	4'h0	Must be set 0
0x10 21	[7:0]	R_PLL_SETTING[47:40]	8	R/W	8'h0	PLL setting value, Feedback Divider value (integer part)
0x10 22	[7:3]	R_PLL_SETTING[39:35]	5	-	5'h0	PLL setting value (Must be set 0)
0x10 22	[2:0]	R_PLL_SETTING[34:32]	3	R/W	3'h0	PLL setting value, Reference Divider value
0x10 23	[7]	R_PLL_SETTING[31]	1	-	1'h0	PLL setting value (Must be set 0)
0x10 23	[6:4]	R_PLL_SETTING[30:28]	3	R/W	3'h0	PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2)
0x10 23	[3]	R_PLL_SETTING[27]	1	-	1'h0	PLL setting value (Must be set 0)
0x10 23	[2:0]	R_PLL_SETTING[26:24]	3	R/W	3'h0	PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2)
0x10 24	[7:0]	R_PLL_SETTING[23:16]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part MSB)
0x10 25	[7:0]	R_PLL_SETTING[15:8]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part)
0x10 26	[7:0]	R_PLL_SETTING[7:0]	8	R/W	8'h0	PLL setting value, Feedback Divider value (decimal part LSB)
0x10 27	[7:4]	reserved	4	-	-	-
0x10 27	[3]	ReservedL	1	R/W	1'b0	Must be set 0
0x10 27	[2]	ReservedH	1	R/W	1'b0	Must be set 1
0x10 27	[1]	ReservedH	1	R/W	1'b0	Must be set 1
0x10 27	[0]	ReservedH	1	R/W	1'b0	Must be set 1
0x10 28	[7:2]	reserved	6	-	-	-
0x10 28	[1:0]	R_CSILANENUM_SEL	2	R/W	2'h0	MIPI CSI total active Lane number Setting 0:CSI 4 lane mode 1:Reserved 2:CSI 2 lane mode 3:CSI 1 lane mode For exmple, MIPI 2PORT2LANE output configuration, total 4 lane (2'h0) setting is required to be set.
0x10 29	[7:0]	reserved	8	-	-	-
0x10 2A	[7:0]	reserved	8	-	-	-
0x10 2B	[7:0]	reserved	8	-	-	-
0x10 2C	[7:0]	reserved	8	-	-	-
0x10 2D	[7:0]	reserved	8	-	-	-
0x10 2E	[7:0]	reserved	8	-	-	-
0x10 2F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x10 30	[7:5]	reserved	3	-	-	-
0x10 30	[4]	R_VX1_CLK_DETEN	1	R/W	1'h0	Main-Link Clock Stop Detection Enable 0:Disable 1:Enable
0x10 30	[3:0]	R_VX1_CLK_SEL	4	R/W	4'h0	Main-Link Master Clock Select [3]Main Mode 0:Fixed Mode 1:Auto Detection Mode [2] All Main-Link Clock Lost Status Mask 0:Mask 1:Not Mask [1:0]Main-Link Master Clock Select 0:LINK0 Main-Link Clock is Master Clock 1:LINK1 Main-Link Clock is Master Clock 2,3:Reserved
0x10 31	[7:1]	reserved	7	-	-	-
0x10 31	[0]	R_VDSKCHK_EN	1	R/W	1'b0	Input Vsync Deskew Check Enable 0:Disable 1:Enable
0x10 32	[7:0]	R_VDSKCHK_LINEPIX[15:8]	8	R/W	8'h0	Limit Pixel-number for Input Vsync Deskew MSB
0x10 33	[7:0]	R_VDSKCHK_LINEPIX[7:0]	8	R/W	8'h0	Limit Pixel-number for Input Vsync Deskew LSB
0x10 34	[7:0]	R_VDSKCHK_LINENUM	8	R/W	8'h0	Limit Line-number for Input Vsync Deskew Limit Number = R_VDSKCHK_LINEPIX*R_VDSKCHK_LINEUM
0x10 35	[7:6]	reserved	2	-	-	-
0x10 35	[5:4]	R_SBET_MODE	2	R/W	2'h0	Sub-Link Field BET Mode Select [4]Enable / 0:Disable, 1:Enable [5]BETOUT select / 0:Raw BETOUT, 1:Latched BETOUT
0x10 35	[3]	ReservedL	1	R/W	1'b0	Must be set 0
0x10 35	[2]	ReservedL	1	R/W	1'b0	Must be set 0
0x10 35	[1]	R_MBET_MODE1	1	R/W	1'b0	Main-Link Field BET Mode Select (for LINK1) 0:Disable, 1:Enable
0x10 35	[0]	R_MBET_MODE0	1	R/W	1'b0	Main-Link Field BET Mode Select (for LINK0) 0:Disable, 1:Enable
0x10 36	[7:0]	reserved	8	-	-	-
0x10 37	[7:0]	reserved	8	-	-	-
0x10 38	[7:0]	reserved	8	-	-	-
0x10 39	[7:0]	reserved	8	-	-	-
0x10 3A	[7:0]	reserved	8	-	-	-
0x10 3B	[7:0]	reserved	8	-	-	-
0x10 3C	[7:0]	reserved	8	-	-	-
0x10 3D	[7:0]	reserved	8	-	-	-
0x10 3E	[7:0]	reserved	8	-	-	-
0x10 3F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x17 00	[7:3]	reserved	5	-	-	-
0x17 00	[2]	R_INTC_ALL2	1	W	-	All Interrption Clear for the Device connected via Sub-Link Target THCV231/5 or THCV241 is automatically selected depending on R_SLINK_MODE setting 1:Clear
	[1]	R_INTC_ALL1	1	W	-	All Interrption Clear for INT1 pin 1:Clear
0x17 00	[0]	R_INTC_ALL0	1	W	-	All Interrption Clear for INT0 pin 1:Clear
0x17 01	[7:6]	ReservedL	2	W	-	Must be set 0
0x17 01	[5:4]	R_PPRCSSR_RST	2	W	-	Software Reset for Pre-processor [5]:Main-Link Lane1 / 1:Software Reset [4]:Main-Link Lane0 / 1:Software Reset
0x17 01	[3]	R_DSHNDLR_RST	1	W	-	Software Reset for Data stream handler 1:Software Reset
0x17 01	[2]	R_CSI_RST	1	W	-	Software Reset for MIPI-CSI2 TX 1:Software Reset
0x17 01	[1]	R_BDC_RST	1	W	-	Software Reset for Sub-Link 1:Software Reset 0x1701[1] Sub-Link reset includes 2-wire slave controller so that 0x1701[1] reset write access cause immediate 2-wire slave abort and reaction to 2-wire master become NACK. In order to avoid NACK, for most cases, 0x0001 Sub-Link reset without 2-wire slave controller is fair enough.
0x17 01	[0]	R_BASE_RST	1	W	-	Software Reset for BASE logic 1:Software Reset
0x17 02	[7:1]	reserved	7	-	-	-
0x17 02	[0]	R_REG_RST	1	W	-	Software Reset for Register 1:Software Reset
0x17 03	[7:2]	reserved	6	-	-	-
0x17 03	[1]	reserved	1	-	-	-
0x17 03	[0]	R_PLL_PDN	1	R/W	1'b0	PLL Power Down 0:PowerDown 1:PowerOn
0x17 04	[7:6]	ReservedL	4	R/W	2'h0	Must be set 0
0x17 04	[5:4]	R_MLINKRX_PDN	4	R/W	2'h0	Main-Link Reciver Power Down [5]:Main-Link Lane1 / 0:PowerDown, 1:PowerOn [4]:Main-Link Lane0 / 0:PowerDown, 1:PowerOn
0x17 04	[3:2]	ReservedL	4	R/W	2'h0	Must be set 0
0x17 04	[1:0]	R_SLINK_PDN	4	R/W	2'h0	Sub-Link Power Down [1]:Sub-Link Lane1 / 0:PowerDown, 1:PowerOn [0]:Sub-Link Lane0 / 0:PowerDown, 1:PowerOn
0x17 05	[7:0]	reserved	8	-	-	-
0x17 06	[7:0]	reserved	8	-	-	-
0x17 07	[7:0]	reserved	8	-	-	-
0x17 08	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x17 09	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x17 0A	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x17 0B	[7:0]	ReservedL	8	R/W	8'h0	Must be set 0
0x17 0C	[7:0]	reserved	8	-	-	-
0x17 0D	[7:0]	reserved	8	-	-	-
0x17 0E	[7:0]	reserved	8	-	-	-
0x17 0F	[7:2]	reserved	6	-	-	-
0x17 0F	[1:0]	R_DSHNDLR_INTSEL	2	R/W	2'd3	Data stream Handler Interrpution Detection condition teaching 0:Main-Link side input upstream is faster 1:MIPI side output downstream is faster 2,3:Both stream is the same speed

Adr	bit	Register Name	width	R/W	init	Description
0x17 10	[7:0]	R_INTR_MLRX0	8	R	-	Interrupt to INT0
0x17 11	[7:6]	R_INTR_MODE0	2	R	-	Interrupt to INT0
0x17 11	[5:4]	R_INTR_DSHNDLR0	2	R	-	Interrupt to INT0
0x17 11	[3:0]	R_INTR_FMT0	4	R	-	Interrupt to INT0
0x17 12	[7:2]	reserved	6	-	-	-
0x17 12	[1:0]	R_INTR_CSI0[8:7]	2	R	-	Interrupt to INT0
0x17 13	[7]	reserved	1	-	-	-
0x17 13	[6:0]	R_INTR_CSI0[6:0]	7	R	-	Interrupt to INT0
0x17 14	[7:2]	reserved	6	-	-	-
0x17 14	[1:0]	R_INTR_BDC2Q0[17:16]	2	R	-	Interrupt to INT0
0x17 15	[7:0]	R_INTR_BDC2Q0[15:8]	8	R	-	[5]R_INTC_EXT2WIRE_ACSEND Lane1 to INT0 [4]R_INTC_EXT2WIRE_ACSEND Lane0 to INT0
0x17 16	[7:0]	R_INTR_BDC2Q0[7:0]	8	R	-	Interrupt to INT0
0x17 17	[7:0]	reserved	8	-	-	-
0x17 18	[7:0]	R_INTR_MLRX1	8	R	-	Interrupt to INT1
0x17 19	[7:6]	R_INTR_MODE1	2	R	-	Interrupt to INT1
0x17 19	[5:4]	R_INTR_DSHNDLR1	2	R	-	Interrupt to INT1
0x17 19	[3:0]	R_INTR_FMT1	4	R	-	Interrupt to INT1
0x17 1A	[7:2]	reserved	6	-	-	-
0x17 1A	[1:0]	R_INTR_CSI1[8:7]	2	R	-	Interrupt to INT1
0x17 1B	[7]	reserved	1	-	-	-
0x17 1B	[6:0]	R_INTR_CSI1[6:0]	7	R	-	Interrupt to INT1
0x17 1C	[7:2]	reserved	6	-	-	-
0x17 1C	[1:0]	R_INTR_BDC2Q1[17:16]	2	R	-	Interrupt to INT1
0x17 1D	[7:0]	R_INTR_BDC2Q1[15:8]	8	R	-	[5]R_INTC_EXT2WIRE_ACSEND Lane1 to INT1 [4]R_INTC_EXT2WIRE_ACSEND Lane0 to INT1
0x17 1E	[7:0]	R_INTR_BDC2Q1[7:0]	8	R	-	Interrupt to INT1
0x17 1F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x17 20	[7:0]	R_INTC_MLRX0	8	W	-	Interrption Clear 1:Clear
0x17 21	[7:6]	R_INTC_MODE0	2	W	-	Interrption Clear 1:Clear
0x17 21	[5:4]	R_INTC_DSHNDLR0	2	W	-	Interrption Clear 1:Clear
0x17 21	[3:0]	R_INTC_FMT0	4	W	-	Interrption Clear 1:Clear
0x17 22	[7:2]	reserved	6	-	-	-
0x17 22	[1:0]	R_INTC_CSI0[8:7]	2	W	-	Interrption Clear 1:Clear
0x17 23	[7]	reserved	1	-	-	-
0x17 23	[6:0]	R_INTC_CSI0[6:0]	7	W	-	Interrption Clear 1:Clear
0x17 24	[7:2]	reserved	6	-	-	-
0x17 24	[1:0]	R_INTC_BDC2Q0[17:16]	2	W	-	Interrption Clear 1:Clear
0x17 25	[7:0]	R_INTC_BDC2Q0[15:8]	8	W	-	Interrption Clear 1:Clear [5]R_INTC_EXT2WIRE_ACSEND Lane1 to INT0 Clear [4]R_INTC_EXT2WIRE_ACSEND Lane0 to INT0 Clear
0x17 26	[7:0]	R_INTC_BDC2Q0[7:0]	8	W	-	Interrption Clear 1:Clear
0x17 27	[7:0]	reserved	8	-	-	-
0x17 28	[7:0]	R_INTC_MLRX1	8	W	-	Interrption Clear 1:Clear
0x17 29	[7:6]	R_INTC_MODE1	2	W	-	Interrption Clear 1:Clear
0x17 29	[5:4]	R_INTC_DSHNDLR1	2	W	-	Interrption Clear 1:Clear
0x17 29	[3:0]	R_INTC_FMT1	4	W	-	Interrption Clear 1:Clear
0x17 2A	[7:2]	reserved	6	-	-	-
0x17 2A	[1:0]	R_INTC_CSI1[8:7]	2	W	-	Interrption Clear 1:Clear
0x17 2B	[7]	reserved	1	-	-	-
0x17 2B	[6:0]	R_INTC_CSI1[6:0]	7	W	-	Interrption Clear 1:Clear
0x17 2C	[7:2]	reserved	6	-	-	-
0x17 2C	[1:0]	R_INTC_BDC2Q1[17:16]	2	W	-	Interrption Clear 1:Clear
0x17 2D	[7:0]	R_INTC_BDC2Q1[15:8]	8	W	-	Interrption Clear 1:Clear [5]R_INTC_EXT2WIRE_ACSEND Lane1 to INT1 Clear [4]R_INTC_EXT2WIRE_ACSEND Lane0 to INT1 Clear
0x17 2E	[7:0]	R_INTC_BDC2Q1[7:0]	8	W	-	Interrption Clear 1:Clear
0x17 2F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x17 30	[7:0]	R_INTM_MLRX0	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 31	[7:6]	R_INTM_MODE0	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 31	[5:4]	R_INTM_DSHNDLR0	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 31	[3:0]	R_INTM_FMT0	4	R/W	4'h0	Interrption Mask 0:Mask
0x17 32	[7:2]	reserved	6	-	-	-
0x17 32	[1:0]	R_INTM_CSI0[8:7]	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 33	[7]	reserved	1	-	-	-
0x17 33	[6:0]	R_INTM_CSI0[6:0]	7	R/W	7'h0	Interrption Mask 0:Mask
0x17 34	[7:2]	reserved	6	-	-	-
0x17 34	[1:0]	R_INTM_BDC2Q0[17:16]	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 35	[7:0]	R_INTM_BDC2Q0[15:8]	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 36	[7:0]	R_INTM_BDC2Q0[7:0]	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 37	[7:0]	reserved	8	-	-	-
0x17 38	[7:0]	R_INTM_MLRX1	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 39	[7:6]	R_INTM_MODE1	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 39	[5:4]	R_INTM_DSHNDLR1	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 39	[3:0]	R_INTM_FMT1	4	R/W	4'h0	Interrption Mask 0:Mask
0x17 3A	[7:2]	reserved	6	-	-	-
0x17 3A	[1:0]	R_INTM_CSI1[8:7]	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 3B	[7]	reserved	1	-	-	-
0x17 3B	[6:0]	R_INTM_CSI1[6:0]	7	R/W	7'h0	Interrption Mask 0:Mask
0x17 3C	[7:2]	reserved	6	-	-	-
0x17 3C	[1:0]	R_INTM_BDC2Q1[17:16]	2	R/W	2'h0	Interrption Mask 0:Mask
0x17 3D	[7:0]	R_INTM_BDC2Q1[15:8]	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 3E	[7:0]	R_INTM_BDC2Q1[7:0]	8	R/W	8'h0	Interrption Mask 0:Mask
0x17 3F	[7:0]	reserved	8	-	-	-

Adr	bit	Register Name	width	R/W	init	Description
0x17 40	[7:2]	reserved	6	-	-	-
0x17 40	[1:0]	VX1_BETOUT	2	R	-	V-by-One Fleld-Bet Result [0]:Vx1 Lane0 Fleld-Bet Result (Latched) [1]:Vx1 Lane1 Fleld-Bet Result (Latched)
0x17 41	[7:2]	reserved	6	-	-	-
0x17 41	[1:0]	VX1_CLK_SEL	2	R	-	Current selected V-by-One Master Clock Lane for PLL Source Clock 0:0Lane Clock is Master for PLL Source Clock 1:1Lane Clock is Master for PLL Source Clock others: Reserved
0x17 42	[7]	reserved	1	-	-	-
0x17 42	[6:4]	LEQOC0	3	R	-	V-by-One® Main-Link Equalizer strength Control Observation (for LINK0) available w ith R_MLINK_AEQEN0=1 (Adaptive Equalizer Mode) 000: 8dB (informative) (the w eakest) 001: 9dB (informative) 011: 10dB (informative) 010: 11dB (informative) 110: 12dB (informative) 111: 13dB (informative) 101: 14dB (informative) 100: 15dB (informative) (the strongest)
0x17 42	[3:0]	reserved	4	-	-	-
0x17 43	[7]	reserved	1	-	-	-
0x17 43	[6:4]	LEQOC1	3	R	-	V-by-One® Main-Link Equalizer strength Control Observation (for LINK1) available w ith R_MLINK_AEQEN1=1 (Adaptive Equalizer Mode) 000: 8dB (informative) (the w eakest) 001: 9dB (informative) 011: 10dB (informative) 010: 11dB (informative) 110: 12dB (informative) 111: 13dB (informative) 101: 14dB (informative) 100: 15dB (informative) (the strongest)
0x17 43	[3:0]	reserved	4	-	-	-
0x17 44	[7:0]	reserved	8	-	-	-
0x17 45	[7:0]	reserved	8	-	-	-
0x17 46	[7:0]	reserved	8	-	-	-
0x17 47	[7:0]	reserved	8	-	-	-
0x17 48	[7:0]	reserved	8	-	-	-
0x17 49	[7:0]	reserved	8	-	-	-
0x17 4A	[7:0]	reserved	8	-	-	-
0x17 4B	[7:0]	reserved	8	-	-	-
0x17 4C	[7:0]	reserved	8	-	-	-
0x17 4D	[7:0]	reserved	8	-	-	-
0x17 4E	[7:0]	reserved	8	-	-	-
0x17 4F	[7:4]	R_MLINK_CRC_ERRCLR	4	W	-	Main-Link CRC Error Counter Clear 1:Clear
	[3:0]	R_MLINK_BET_ERRCLR	4	W	-	Main-Link BET Error Counter Clear 1:Clear
0x17 50	[7:0]	MLINK0_CRC_ERRNUM[15:8]	8	R	-	Main-Link(Lane0) CRC Error Number (Upper Byte)
0x17 51	[7:0]	MLINK0_CRC_ERRNUM[7:0]	8	R	-	Main-Link(Lane0) CRC Error Number (Low er Byte)
0x17 52	[7:0]	MLINK1_CRC_ERRNUM[15:8]	8	R	-	Main-Link(Lane1) CRC Error Number (Upper Byte)
0x17 53	[7:0]	MLINK1_CRC_ERRNUM[7:0]	8	R	-	Main-Link(Lane1) CRC Error Number (Low er Byte)
0x17 54	[7:0]	reserved	8	-	-	-
0x17 55	[7:0]	reserved	8	-	-	-
0x17 56	[7:0]	reserved	8	-	-	-
0x17 57	[7:0]	reserved	8	-	-	-
0x17 58	[7:0]	MLINK0_BET_ERRNUM[15:8]	8	R	-	Main-Link(Lane0) BET Error Number (Upper Byte)
0x17 59	[7:0]	MLINK0_BET_ERRNUM[7:0]	8	R	-	Main-Link(Lane0) BET Error Number (Low er Byte)
0x17 5A	[7:0]	MLINK1_BET_ERRNUM[15:8]	8	R	-	Main-Link(Lane1) BET Error Number (Upper Byte)
0x17 5B	[7:0]	MLINK1_BET_ERRNUM[7:0]	8	R	-	Main-Link(Lane1) BET Error Number (Low er Byte)
0x17 5C	[7:0]	reserved	8	-	-	-
0x17 5D	[7:0]	reserved	8	-	-	-
0x17 5E	[7:0]	reserved	8	-	-	-
0x17 5F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	R/W	Initial	Description
0x1100	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_PH_EN0	R/W	1'b0	Main-Link Lane0 Input MIPI Packet Header intake 1'b0: Packet Header from Main-Link Lane0 not used 1'b1: Packet Header from Main-Link Lane0 input
0x1101	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_CRC_EN0	R/W	1'b0	Main-Link Lane0 Input CRC intake 1'b0: CRC from Main-Link Lane0 not used 1'b1: CRC from Main-Link Lane0 input
0x1102	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_SP_EN0	R/W	1'b0	Main-Link Lane0 Input MIPI Short Packet intake 1'b0: Short Packet from Main-Link Lane0 not used 1'b1: Short Packet from Main-Link Lane0 input
0x1103	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_VVALID_MODE0	R/W	1'b0	Main-Link Lane0 to MIPI VVALID generation mode 1'b0: mode1 (available with THCV241) 1'b1: mode2 (FS/FE generation from VSYNC)
0x1104	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_VSYNC_POL0	R/W	1'b0	Main-Link Lane0 VSYNC intake polarity 1'b0: Low active / VSYNC=Low pulse 1'b1: High active / VSYNC=High pulse
0x1105	[7:0]	R_VX1_WC_LOW0	R/W	8'h00	Main-Link Lane0 to MIPI Word Count (LSB 8bit) manual setting (Only active when R_VX1_PH_EN=0)
0x1106	[7:0]	R_VX1_WC_UP0	R/W	8'h00	Main-Link Lane0 to MIPI Word Count (MSB 8bit) manual setting (Only active when R_VX1_PH_EN=0)
0x1107	[7:0]	R_VX1_DATAID0	R/W	8'h00	Main-Link Lane0 to MIPI Data ID manual setting (Only active when R_VX1_PH_EN=0)

Address	bit	Register Name	R/W	Initial	Description
0x1200	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_PH_EN1	R/W	1'b0	Main-Link Lane1 Input MIPI Packet Header intake 1'b0: Packet Header from Main-Link Lane1 not used 1'b1: Packet Header from Main-Link Lane1 input
0x1201	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_CRC_EN1	R/W	1'b0	Main-Link Lane1 Input CRC intake 1'b0: CRC from Main-Link Lane1 not used 1'b1: CRC from Main-Link Lane1 input
0x1202	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_SP_EN1	R/W	1'b0	Main-Link Lane1 Input MIPI Short Packet intake 1'b0: Short Packet from Main-Link Lane1 not used 1'b1: Short Packet from Main-Link Lane1 input
0x1203	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_VVALID_MODE1	R/W	1'b0	Main-Link Lane1 to MIPI VVALID generation mode 1'b0: mode1 (available with THCV241) 1'b1: mode2 (FS/FE generation from VSYNC)
0x1204	[7:1]	-	-	7'h00	Reserved
	[0]	R_VX1_VSYNC_POL1	R/W	1'b0	Main-Link Lane1 VSYNC intake polarity 1'b0: Low active / VSYNC=Low pulse 1'b1: High active / VSYNC=High pulse
0x1205	[7:0]	R_VX1_WC_LOW1	R/W	8'h00	Main-Link Lane1 to MIPI Word Count (LSB 8bit) manual setting (Only active when R_VX1_PH_EN=0)
0x1206	[7:0]	R_VX1_WC_UP1	R/W	8'h00	Main-Link Lane1 to MIPI Word Count (MSB 8bit) manual setting (Only active when R_VX1_PH_EN=0)
0x1207	[7:0]	R_VX1_DATAID1	R/W	8'h00	Main-Link Lane1 to MIPI Data ID manual setting (Only active when R_VX1_PH_EN=0)

Address	bit	Register Name	R/W	Initial	Description
0x1501	[7:5]	-	-	3'b000	Reserved
	[4:0]	R_MODE_NO	R/W	5'b0000_0	Main-Link input data stream handling mode number 5'd0,1,2,3,8,10,11 are available. Others: reserved

Address	bit	Register Name	R/W	Initial	Description
0x1600	[7:5]	-	-	3'b000	Reserved
	[4:0]	R_ANALOG	R/W	5'h00	[4] MIPI Power Down 0: Power Down 1: Normal operation [3] MIPI Soft Reset 0: Reset 1: Normal operation [2] ReservedL: Must be set 0 [1] ReservedH: Must be set 1 [0] ReservedL: Must be set 0
0x1601	[7:0]	ReservedX	R/W	8'h1B	must be left as default 0x1B
0x1602	[7:0]	R_TX_LANE_SEL0	R/W	8'b1110_0100	MIPI Tx Lane assignment select (SWAP) [7:6]Lane3, [5:4]Lane2, [3:2]Lane1, [1:0]Lane0 2'b00:1st Byte output 2'b01:2nd Byte output 2'b10:3rd Byte output 2'b11:4th Byte output *On 2port output configuration, 3rd and 4th Byte are 2nd PORT1 *On 2port 1lane output configuration, 1st and 3rd Byte are used
0x1603	[7:1]	-	-	7'h00	Reserved
	[1:0]	R_TX_LANE_SEL1	R/W	2'b00	MIPI 2port output 2nd PORT1 select (Select 3rd Byte assigned 2nd PORT1 TX lane)
0x1604	[7:0]	ReservedX	R/W	8'h3F	must be left as default 0x3F

Address	bit	Register Name	R/W	Initial	Description
0x1605	[7]	-	-	1'b0	Reserved
	[6:0]	R_LANE_EN	R/W	7'b0101_011	[6:5] MIPI Data lane Enable [6] Data PORT1 / 0:OFF, 1:ON [5] Data PORT0 / 0:OFF, 1:ON [4:3] MIPI CLK lane Enable [4] CLK lane1 / 0:OFF, 1:ON [3] CLK lane0 / 0:OFF, 1:ON [2:0] MIPI Configuration 3'b000:1PORT1LANE 3'b001:1PORT2LANE 3'b010:Reserved 3'b011:1PORT4LANE 3'b100:2PORT1LANE 3'b101:2PORT2LANE 3'b110:Reserved 3'b111:Reserved
0x1606	[7]	-	-	1'b0	Reserved
	[6:0]	R_MODE_SET	R/W	7'b100_0000	[6] ReservedH: Must be set 1 [5:4] ReservedL: Must be set 0 [3:2] HBLANK CLK OFF [3] HBLANK CLK OFF PORT1 0:OFF (HS clock off and go into LP at HBlank) 1:ON (HS clock continuously on at HBlank) [2] HBLANK CLK OFF PORT0 0:OFF (HS clock off and go into LP at HBlank) 1:ON (HS clock continuously on at HBlank) [1:0] CLK_NOT_STOP [1] CLK_NOT_STOP PORT1 0:OFF (HS clock off at VBlank) 1:ON (HS clock permanently on) [0] CLK_NOT_STOP PORT0 0:OFF (HS clock off at VBlank) 1:ON (HS clock permanently on) "7'b100_1100" is typical usage
0x1607	[7:0]	R_DINSEL_P0	R/W	8'b1110_0100	MIPI Data Byte SWAP PORT0 defalut setting is for MIPI standard order 2'b00:Byte0([7:0]) 2'b01:Byte1([15:8]) 2'b10:Byte2([23:16]) 2'b11:Byte3([31:24])
0x1608	[7:4]	-	-	4'b0000	Reserved
	[3:0]]	R_DINSEL_P1	R/W	4'b1110	MIPI Data Byte SWAP PORT1 defalut setting is for MIPI standard order 2'b10:Byte2([23:16]) 2'b11:Byte3([31:24])

Address	bit	Register Name	R/W	Initial	Description
0x1609	[7:0]	R_TX_CLK_PREPARE0	R/W	8'd4	CLK lane PrePare period setting PORT0 arrangement with counterpart MIPI Rx is required. (informative)tclk_prepare.ref={(R_TX_CLK_PREPARE0)+1}*[{1/F(OUT)}*8] +53 (ns) (informative)setting reference with data-rate (informative)0x05 from 1.2Gbps to 1.1Gbps (informative)0x04 from 1.1Gbps to 1Gbps (informative)0x03 from 1Gbps to 750Mbps (informative)0x02 from 750Mbps to 500Mbps (informative)0x01 from 500Mbps to 250Mbps (informative)0x00 from 250Mbps to 80Mbps
0x160a	[7:0]	R_TX_CLK_ZERO0	R/W	8'h1d	CLK lane ZERO period setting PORT0 (informative)tclk_zero.ref={(R_TX_CLK_ZERO0)+1}*[{1/F(OUT)}*8] -56 (ns) (informative)setting reference (informative)(R_TX_CLK_PREPARE0+R_TX_CLK_ZERO0)*[{1/F(OUT)}*8] is supposed to be more than 360ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x160b	[7:0]	R_TX_CLK_TRAIL0	R/W	8'h07	CLK lane TRAIL period setting PORT0 (informative)tclk_trail.ref=(R_TX_CLK_TRAIL0)*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative)(R_TX_CLK_TRAIL0)*[{1/F(OUT)}*8] is supposed to be more than 100ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x160c	[7:0]	R_TX_CLK_PRE0	R/W	8'h02	CLK lane PRE period setting PORT0 (informative)tclk_pre.ref=(R_TX_CLK_PRE0)*[{1/F(OUT)}*8] +7 (ns) (informative)setting reference (informative)(R_TX_CLK_PRE0) is supposed to be equal or more than 2 (0x02) (informative)To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x160d	[7:0]	R_TX_CLK_POST0	R/W	8'h0c	CLK lane POST period setting PORT0 (informative)tclk_post.ref={(R_TX_CLK_POST0)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_CLK_POST0)-6}*[{1/F(OUT)}*8] is supposed to be more than 60ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x160e	[7:0]	R_TX_THS_EXIT0	R/W	8'h0b	CLK and Data lane EXIT period setting PORT0 This register determines minumum time of HS_EXIT, Low Power state. If blanking period of data stream is more than this register setting, HS_EXIT becomes blanking period of data stream itself for most cases. Too long value setting over blanking period of data stream is also not recommended. (informative)ths_exit.ref={(R_TX_THS_EXIT0)+7}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_THS_EXIT0)+7}*[{1/F(OUT)}*8] is supposed to be more than 100ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x160f	[7:0]	R_TX_TLPX0	R/W	8'h05	Data lane TLPX period setting PORT0 (informative)tlpx.ref={(R_TX_TLPX0)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_TLPX0)+1}*[{1/F(OUT)}*8] is supposed to be more than 50ns (informative)margin value setting is highly recommended. To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x1610	[7:0]	R_TX_THS_PREPARE0	R/W	8'h04	Data lane Prepare period setting PORT0 arrangement with counterpart MIPI Rx is required. (informative)ths_prepare.ref={(R_TX_THS_PREPARE0)+1}*[{1/F(OUT)}*8] +53 (ns) (informative)setting reference with data-rate (informative)0x04 from 1.2Gbps to 1Gbps (informative)0x03 from 1Gbps to 700Mbps (informative)0x02 from 700Mbps to 450Mbps (informative)0x01 from 450Mbps to 80Mbps
0x1611	[7:0]	R_TX_THS_ZERO0	R/W	8'h10	Data lane ZERO period setting PORT0 (informative)ths_zero.ref={(R_TX_THS_ZERO0)+4}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative)(R_TX_THS_PREPARE0+R_TX_THS_ZERO0+3)*[{1/F(OUT)}*8] is supposed to be more than 150ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x1612	[7:0]	R_TX_THS_TRAIL0	R/W	8'h07	Data lane TRAIL period setting PORT0 (informative)ths_trail.ref={(R_TX_THS_TRAIL0)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_THS_TRAIL0)-2}*[{1/F(OUT)}*8] is supposed to be more than 90ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x1613	[7:0]	R_TX_MARK0	R/W	8'h40	ULPS exit TWAKEUP setting PORT0 (informative)twakeup.ref=(R_TX_MARK0)*[{1/F(OUT)}*8]*(2^11) at least. (informative)setting reference (informative)(R_TX_MARK0)*[{1/F(OUT)}*8]*(2^11) is supposed to be more than 1ms (informative)margin value setting is highly recommended. To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x1614	[7:0]	R_TX_CLK_PREPARE1	R/W	8'h04	CLK lane PrePare period setting PORT1 arrangement with counterpart MIPI Rx is required. (informative)tclk_prepare.ref={(R_TX_CLK_PREPARE1)+1}*[{1/F(OUT)}*8] +53 (ns) (informative)setting reference with data-rate (informative)0x05 from 1.2Gbps to 1.1Gbps (informative)0x04 from 1.1Gbps to 1Gbps (informative)0x03 from 1Gbps to 750Mbps (informative)0x02 from 750Mbps to 500Mbps (informative)0x01 from 500Mbps to 250Mbps (informative)0x00 from 250Mbps to 80Mbps
0x1615	[7:0]	R_TX_CLK_ZERO1	R/W	8'h1d	CLK lane ZERO period setting PORT1 (informative)tclk_zero.ref={(R_TX_CLK_ZERO1)+1}*[{1/F(OUT)}*8] -56 (ns) (informative)setting reference (informative)(R_TX_CLK_PREPARE1+R_TX_CLK_ZERO1)*[{1/F(OUT)}*8] is supposed to be more than 360ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x1616	[7:0]	R_TX_CLK_TRAIL1	R/W	8'h07	CLK lane TRAIL period setting PORT1 (informative)tclk_trail.ref=(R_TX_CLK_TRAIL1)*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative)(R_TX_CLK_TRAIL1)*[{1/F(OUT)}*8] is supposed to be more than 100ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x1617	[7:0]	R_TX_CLK_PRE1	R/W	8'h02	CLK lane PRE period setting PORT1 (informative)tclk_pre.ref=(R_TX_CLK_PRE1)*[{1/F(OUT)}*8] +7 (ns) (informative)setting reference (informative)(R_TX_CLK_PRE1) is supposed to be equal or more than 2 (0x02) (informative)To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x1618	[7:0]	R_TX_CLK_POST1	R/W	8'h0c	CLK lane POST period setting PORT1 (informative)tclk_post.ref={(R_TX_CLK_POST1)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_CLK_POST1)-6}*[{1/F(OUT)}*8] is supposed to be more than 60ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x1619	[7:0]	R_TX_THS_EXIT1	R/W	8'h0b	CLK and Data lane EXIT period setting PORT1 This register determines minumum time of HS_EXIT, Low Power state. If blanking period of data stream is more than this register setting, HS_EXIT becomes blanking period of data stream itself for most cases. Too long value setting over blanking period of data stream is also not recommended. (informative)ths_exit.ref={(R_TX_THS_EXIT1)+7}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_THS_EXIT1)+7}*[{1/F(OUT)}*8] is supposed to be more than 100ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x161a	[7:0]	R_TX_TLPX1	R/W	8'h05	Data lane TLPX period setting PORT1 (informative)tlpx.ref={(R_TX_TLPX1)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_TLPX1)+1}*[{1/F(OUT)}*8] is supposed to be more than 50ns (informative)margin value setting is highly recommended. To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x161b	[7:0]	R_TX_THS_PREPARE1	R/W	8'h04	Data lane Prepare period setting PORT1 arrangement with counterpart MIPI Rx is required. (informative)ths_prepare.ref={(R_TX_THS_PREPARE1)+1}*[{1/F(OUT)}*8] +53 (ns) (informative)setting reference with data-rate (informative)0x04 from 1.2Gbps to 1Gbps (informative)0x03 from 1Gbps to 700Mbps (informative)0x02 from 700Mbps to 450Mbps (informative)0x01 from 450Mbps to 80Mbps
0x161c	[7:0]	R_TX_THS_ZERO1	R/W	8'h10	Data lane ZERO period setting PORT1 (informative)ths_zero.ref={(R_TX_THS_ZERO1)+4}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative)(R_TX_THS_PREPARE1+R_TX_THS_ZERO1+3)*[{1/F(OUT)}*8] is supposed to be more than 150ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x161d	[7:0]	R_TX_THS_TRAIL1	R/W	8'h07	Data lane TRAIL period setting PORT1 (informative)ths_trail.ref={(R_TX_THS_TRAIL1)+1}*[{1/F(OUT)}*8] (ns) (informative)setting reference (informative){(R_TX_THS_TRAIL1)-2}*[{1/F(OUT)}*8] is supposed to be more than 90ns (informative)margin value setting is highly recommended. To use default value is better way as an example.
0x161e	[7:0]	R_TX_MARK1	R/W	8'h40	ULPS exit TWAKEUP setting PORT1 (informative)twakeup.ref=(R_TX_MARK1)*[{1/F(OUT)}*8]*(2^11) at least. (informative)setting reference (informative)(R_TX_MARK1)*[{1/F(OUT)}*8]*(2^11) is supposed to be more than 1ms (informative)margin value setting is highly recommended. To use default value is better way as an example.

Address	bit	Register Name	R/W	Initial	Description
0x161f	[7:4]	-	-	2'b00	Reserved
	[3:0]	R_REQ_SEL	R/W	4'h0	MIPI Tx Lane PORT assignment [3]Lane3, [2]Lane2, [1]Lane1, [0]Lane0 0:PORT0 1:PORT1

Notices and Requests

1.The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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4. Note that even if infringement of any third party's industrial ownership should occur by using this product, THine will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.
sales@thine.co.jp
https://www.thine.co.jp