
<i>Application Note</i>	<i>THCV241A_RegisterMap_Rev200_E</i>
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THCV241A Register Map



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Register Map

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master Addr(h)	Slave Addr(h)							
0x0000	0x0080	[7:1]	reserved	7	-	-	-	-
0x0000	0x0080	[0]	R_INT	1	R	Interrupt signal (Total-OR) 1: Interrupt	-	M
0x0001	-	[7:1]	reserved	7	-	-	-	-
0x0001	-	[0]	R_SLINK_RST	1	W	Sub-Link Soft Reset 1: Reset	-	M
0x0002	-	[7:0]	reserved	8	-	-	-	-
0x0003	-	[7:0]	reserved	8	-	-	-	-
0x0004	-	[7:2]	reserved	6	-	-	-	-
0x0004	-	[1:0]	R_SLINK_MODE	2	RW	Sub-Link basic protocol setting as Sub-Link Master 0: Reserved 1: 2-wire Set&Trigger (Normal) mode1 (compatible with THCV236) 2: Reserved 3: Reserved Note: When THCV241 is used as Sub-Link Slave, this register setting has no meaning. Counterpart Sub-Link Master setting controls Sub-Link protocol including THCV241 as slave device.	2'd1	M
0x0005	-	[7:0]	reserved	8	-	-	-	-
0x0006	-	[7:0]	reserved	8	-	-	-	-
0x0007	-	[7:0]	reserved	8	-	-	-	-
0x0008	0x0088	[7:1]	reserved	7	-	-	-	-
0x0008	0x0088	[0]	R_CKSUM_EN	1	RW	Internal Register AutoCheckSum Enable 0:Disable 1:Enable	1'b0	MS
0x0009	0x0089	[7:0]	R_CKSUM_TIM	8	RW	Internal Register AutoCheckSum check interval =1024x64x(R_CKSUM_TIM<7:0>+1) x tOSC	8'd19	MS
0x000A	0x008A	[7:0]	R_CKSUM_VAL	8	RW	Internal Register AutoCheckSum expected target value	8'd0	MS
0x000B	0x008B	[7:0]	R_CKSUM_RVAL	8	R	Internal Register AutoCheckSum read value	-	MS
0x000C	-	[7:0]	reserved	8	-	-	-	-
0x000D	-	[7:0]	reserved	8	-	-	-	-
0x000E	-	[7:0]	reserved	8	-	-	-	-
0x000F	-	[7:0]	reserved	8	-	-	-	-

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master Addr(h)	Slave Addr(h)							
0x0010	-	[7:1]	reserved	7	-	-	-	-
0x0010	-	[0]	R_SLINK_EN	1	RW	Sub-link Enable 0:Sub-Link Disable 1:Sub-Link Enable	1'b0	M
0x0011	-	[7:0]	reserved	8	-	-	-	-
0x0012	-	[7:0]	reserved	8	-	-	-	-
0x0013	-	[7:0]	reserved	8	-	-	-	-
0x0014	-	[7:5]	reserved	3	-	-	-	-
0x0014	-	[4]	R_SLINK_POL_EN	1	RW	Sub-Link Polling Enable 0:Disable 1:Enable	1'b1	M
0x0014	-	[3:2]	reserved	2	-	-	-	-
0x0014	-	[1:0]	R_SLINK_POL_TIM_UP	2	RW	Sub-Link Polling interval setting	2'd0	M
0x0015	-	[7:0]	R_SLINK_POL_TIM_DN	8	RW	Sub-Link Polling interval time=64x(256x R_SLINK_POL_TIM_UP<1:0> +R_SLINK_POL_TIM_DN<7:0>+1)x tOSC *No Polling when R_SLINK_POL_TIM_UP=0 and R_SLINK_POL_TIM_DN=0	8'd124	M
0x0016	-	[7:5]	reserved	3	-	-	-	-
0x0016	-	[4]	R_SLINK_SSR_EN	1	RW	Sub-Link SSR Enable 0:Disable 1:Enable	1'b1	M
0x0016	-	[3:2]	reserved	2	-	-	-	-
0x0016	-	[1:0]	R_SLINK_SSR_TIM_UP	2	RW	Sub-Link SSR interval setting	2'd0	M
0x0017	-	[7:0]	R_SLINK_SSR_TIM_DN	8	RW	Sub-Link SSR interval time=64x(256xR_SLINK_SSR_TIM_UP<1:0> +R_SLINK_SSR_TIM_DN<7:0>+1)x tOSC *No SSR when R_SLINK_SSR_TIM_UP=0 and R_SLINK_SSR_TIM_DN=0	8'd249	M
0x0018	0x0098	[7:5]	reserved	3	-	-	-	-
0x0018	0x0098	[4]	R_SLINK_WD_EN	1	RW	Sub-Link WDT Enable 0:Disable 1:Enable	1'b1	MS
0x0018	0x0098	[3:2]	reserved	2	-	-	-	-
0x0018	0x0098	[1:0]	R_SLINK_WD_TIM_UP	2	RW	Sub-Link WDT time parameter	2'd0	MS
0x0019	0x0099	[7:0]	R_SLINK_WD_TIM_DN	8	RW	Sub-Link WDT time =64x(256xR_SLINK_WD_TIM_UP<1:0> + R_SLINK_WD_TIM_DN<7:0>+1) x tOSC	8'd187	MS

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master	Slave							
Addr(h)	Addr(h)							
0x001A	-	[7:0]	reserved	8	-	-	-	-
0x001B	-	[7:0]	reserved	8	-	-	-	-
0x001C	-	[7:0]	reserved	8	-	-	-	-
0x001D	-	[7:0]	reserved	8	-	-	-	-
0x001E	-	[7:0]	reserved	8	-	-	-	-
0x001F	-	[7:0]	reserved	8	-	-	-	-
0x0020	0x00A0	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	MS
0x0021	0x00A1	[7:0]	reserved	8	-	-	-	MS
0x0022	0x00A2	[7:0]	reserved	8	-	-	-	MS
-	0x00A3	[7:1]	reserved	7	-	-	-	-
-	0x00A3	[0]	R_SLINK_FBETERR_CLR	1	W	Sub-Link FieldBET error count clear 1: Clear	-	S
-	0x00A4	[7:0]	R_SLINK_FBETERR_NUM_UP	8	R	Sub-Link FieldBET error count parameter	-	S
-	0x00A5	[7:0]	R_SLINK_FBETERR_NUM_DN	8	R	Sub-Link FieldBET error count = 256 × R_SLINK_FBETERR_NUM_UP<7:0> + R_SLINK_FBETERR_NUM_DN<7:0>	-	S
0x0026	-	[7:0]	reserved	8	-	-	-	-
0x0027	-	[7:0]	reserved	8	-	-	-	-
0x0028	-	[7:0]	reserved	8	-	-	-	-
0x0029	-	[7:0]	reserved	8	-	-	-	-
0x002A	-	[7:0]	reserved	8	-	-	-	-
0x002B	-	[7:0]	reserved	8	-	-	-	-
0x002C	-	[7:0]	reserved	8	-	-	-	-
0x002D	-	[7:0]	reserved	8	-	-	-	-
0x002E	-	[7:0]	reserved	8	-	-	-	-
0x002F	-	[7:0]	reserved	8	-	-	-	-

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master	Slave							
Addr(h)	Addr(h)							
0x0030	-	[7:0]	R_2WIRE_DATA0	8	RW	2-wire serial VF remote write/read data #0	8'd0	M
0x0031	-	[7:0]	R_2WIRE_DATA1	8	RW	2-wire serial VF remote write/read data #1	8'd0	M
0x0032	-	[7:0]	R_2WIRE_DATA2	8	RW	2-wire serial VF remote write/read data #2	8'd0	M
0x0033	-	[7:0]	R_2WIRE_DATA3	8	RW	2-wire serial VF remote write/read data #3	8'd0	M
0x0034	-	[7:0]	R_2WIRE_DATA4	8	RW	2-wire serial VF remote write/read data #4	8'd0	M
0x0035	-	[7:0]	R_2WIRE_DATA5	8	RW	2-wire serial VF remote write/read data #5	8'd0	M
0x0036	-	[7:0]	R_2WIRE_DATA6	8	RW	2-wire serial VF remote write/read data #6	8'd0	M
0x0037	-	[7:0]	R_2WIRE_DATA7	8	RW	2-wire serial VF remote write/read data #7	8'd0	M
0x0038	-	[7:0]	R_2WIRE_DATA8	8	RW	2-wire serial VF remote write/read data #8	8'd0	M
0x0039	-	[7:0]	R_2WIRE_DATA9	8	RW	2-wire serial VF remote write/read data #9	8'd0	M
0x003A	-	[7:0]	R_2WIRE_DATA10	8	RW	2-wire serial VF remote write/read data #10	8'd0	M
0x003B	-	[7:0]	R_2WIRE_DATA11	8	RW	2-wire serial VF remote write/read data #11	8'd0	M
0x003C	-	[7:0]	R_2WIRE_DATA12	8	RW	2-wire serial VF remote write/read data #12	8'd0	M
0x003D	-	[7:0]	R_2WIRE_DATA13	8	RW	2-wire serial VF remote write/read data #13	8'd0	M
0x003E	-	[7:0]	R_2WIRE_DATA14	8	RW	2-wire serial VF remote write/read data #14	8'd0	M
0x003F	-	[7:0]	R_2WIRE_DATA15	8	RW	2-wire serial VF remote write/read data #15	8'd0	M
0x0040	-	[7:1]	R_2WIRE_DEVADR	7	RW	2-wire serial VF remote access target device address. if target=self addr.; access to Sub-Link Slave inside register, else; access to remote side 2-wire serial Slave devices externally connected to Sub-Link slave	7'h00	M
0x0040	-	[0]	R_2WIRE_WR	1	RW	2-wire serial VF remote access write or read select 0:Write 1:Read	1'b0	M
0x0041	-	[7]	reserved	1	-	-	-	-
0x0041	-	[6:4]	R_2WIRE_WADR_BYTE	3	RW	2-wire serial VF remote device's Sub Address (Word Address, register address) Byte width select. address Byte width=R_2WIRE_WADR_BYTE<2:0>+1 0 : 1Byte= 8bit Sub addr.(register addr.) 1 : 2Byte=16bit Sub addr.(register addr.) 4 : 5Byte=40bit Sub addr.(register addr.), etc.	3'd0	M
0x0041	-	[3:0]	R_2WIRE_DATA_BYTE	4	RW	2-wire serial VF remote access data Byte number Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3byte burst) [write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE =< 'd16 [read rule] R_2WIRE_DATA_BYTE=<'d16	4'd0	M
0x0042	-	[7:1]	reserved	7	-	-	-	-
0x0042	-	[0]	R_2WIRE_CLKSEN	1	RW	2-wire serial VF local response clock stretching Enable 0: Sub-Link Master (2-wire slave) No clock stretching 1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode forces clock stretching Enable	1'b0	M
0x0043	-	[7:1]	reserved	7	-	-	-	-
0x0043	-	[0]	R_2WIRE_START	1	W	2-wire serial VF remote access start trigger	-	M
0x0044	-	[7:0]	reserved	8	-	-	-	-
0x0045	-	[7:0]	reserved	8	-	-	-	-
0x0046	-	[7:0]	reserved	8	-	-	-	-
0x0047	-	[7:0]	reserved	8	-	-	-	-
-	0x00C8	[7:1]	reserved	7	-	-	-	-
-	0x00C8	[0]	R_2WIRE_BUS_CLR	1	W	2-wire serial VF remote side bus clear Write 1: 2-wire bus clear action triggered from Sub-Link Slave (2-wire master) to 2-wire slave device connected to Sub-Link Slave. This bit is automatically cleared into 0 after reset action. 0 is always read.	-	S
-	0x00C9	[7:0]	R_2WIRE_SCL_HW	8	RW	SCL High width [tHIGH] setting on Sub-Link Slave side. Output SCL High width is defined as below. 16x(R_2WIRE_SCL_HW<7:0>+1) * tOSC	8'd31	S
-	0x00CA	[7:0]	R_2WIRE_SCL_LW	8	RW	SCL Low width [tLOW] setting on Sub-Link Slave side. Output SCL Low width is defined as below. 16x(R_2WIRE_SCL_LW<7:0>+1) * tOSC	8'd31	S

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master	Slave							
Addr(h)	Addr(h)							
0x004B	0x00CB	[7:5]	reserved	3	-	-	-	-
0x004B	0x00CB	[4]	R_2WIRE_WD_EN	1	RW	2-wire WDT Enable 0:Disable 1:Enable	1'b1	MS
0x004B	0x00CB	[3:1]	reserved	3	-	-	-	-
0x004B	0x00CB	[0]	R_2WIRE_WD_OFFSET	1	RW	2-wire WDT offset time 1:11'd2047 0:11'd1023	1'd1	MS
0x004C	0x00CC	[7:0]	R_2WIRE_WD_TIM	8	RW	2-wire WDT time = 64x{R_2WIRE_WD_TIM<7:0>+1}x("2WIRE WDT offset time") x tOSC	8'd255	MS
0x004D	-	[7:0]	reserved	8	-	-	-	-
0x004E	-	[7:0]	reserved	8	-	-	-	-
0x004F	-	[7:0]	reserved	8	-	-	-	-
0x0050	0x00D0	[7:0]	R_2WIRE_SADR	8	RW	2WIRE slave device address setting [7]2WIRE slave device address control 0: 2WIRE slv device addr. is set by AIN pin 1: 2WIRE slv device addr. is set by following register [6:0] [6:0]2WIRE slave device address value for register control	8'd0	MS
0x0051	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0052	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0053	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0054	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0055	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0056	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0057	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0058	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x0059	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x005A	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x005B	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x005C	-	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	M
0x005D	-	[7:0]	reserved	8	-	-	-	-
0x005E	-	[7:0]	reserved	8	-	-	-	-
0x005F	-	[7:0]	reserved	8	-	-	-	-

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master Addr(h)	Slave Addr(h)							
0x0060	0x00E0	[7:6]	reserved	2	-	-	-	-
0x0060	0x00E0	[5]	R_INT_EXTERNAL	1	R	Interrupt factor: IC Internal event except Sub-Link 1: Interrupt (event is detected)	-	MS
0x0060	0x00E0	[4]	R_INT_CKSUM_ERR	1	R	Interrupt factor: Internal register Checksum error 1: Interrupt (error is detected)	-	MS
0x0060	0x00E0	[3]	R_INT_I2C_TMOUT	1	R	Interrupt factor: 2-wire access time out error 1: Interrupt (error is detected)	-	MS
0x0060	0x00E0	[2]	reserved	1	-	-	-	MS
0x0060	0x00E0	[1]	R_INT_SLINK_PROTERR	1	R	Interrupt factor: Sub-Link protocol error 1: Interrupt (error is detected)	-	MS
0x0060	0x00E0	[0]	R_INT_SLINK_TMOUT	1	R	Interrupt factor: Sub-Link access time out error 1: Interrupt (error is detected)	-	MS
0x0061	0x00E1	[7:6]	reserved	2	-	-	-	-
0x0061	0x00E1	[5]	R_INTM_EXTERNAL	1	RW	Interrupt mask: IC Internal error except Sub-Link 0: Interrupt masked (related Interrupt Low fixed)	1'b0	MS
0x0061	0x00E1	[4]	R_INTM_CKSUM_ERR	1	RW	Interrupt mask: Internal register CheckSum error 0: Interrupt masked (related Interrupt Low fixed)	1'b0	MS
0x0061	0x00E1	[3]	R_INTM_I2C_TMOUT	1	RW	Interrupt mask: 2-wire access time out error 0: Interrupt masked (related Interrupt Low fixed)	1'b0	MS
0x0061	0x00E1	[2]	ReservedL	1	RW	Must be set 0	1'b0	MS
0x0061	0x00E1	[1]	R_INTM_SLINK_PROTERR	1	RW	Interrupt mask: Sub-Link protocol error 0: Interrupt masked (related Interrupt Low fixed)	1'b0	MS
0x0061	0x00E1	[0]	R_INTM_SLINK_TMOUT	1	RW	Interrupt mask: Sub-Link access time out error 0: Interrupt masked (related Interrupt Low fixed)	1'b0	MS
0x0062	0x00E2	[7:6]	reserved	2	-	-	-	-
0x0062	0x00E2	[5]	R_INTC_EXTERNAL	1	W	Interrupt clear: IC Internal error except Sub-Link 1: Interrupt clear	-	MS
0x0062	0x00E2	[4]	R_INTC_CKSUM_ERR	1	W	Interrupt clear: Internal register CheckSum error 1: Interrupt clear	-	MS
0x0062	0x00E2	[3]	R_INTC_I2C_TMOUT	1	W	Interrupt clear: 2-wire access time out error 1: Interrupt clear	-	MS
0x0062	0x00E2	[2]	reserved	1	-	-	-	MS
0x0062	0x00E2	[1]	R_INTC_SLINK_PROTERR	1	W	Interrupt clear: Sub-Link protocol error 1: Interrupt clear	-	MS
0x0062	0x00E2	[0]	R_INTC_SLINK_TMOUT	1	W	Interrupt clear: Sub-Link access time out error 1: Interrupt clear	-	MS

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master Addr(h)	Slave Addr(h)							
0x0063	-	[7:4]	reserved	4	-	-	-	-
0x0063	-	[3]	R_INT_LOCKN	1	R	Interrupt factor: Main-Link LOCKN transition 1: Interrupt (transition is detected)	-	M
0x0063	-	[2]	R_INT_HTPDN	1	R	Interrupt factor: Main-Link HTPDN transition 1: Interrupt (transition is detected)	-	M
0x0063	-	[1]	R_INT_SLAVESIDE	1	R	Interrupt factor: Sub-Link Slave side factor 1: Interrupt (factor is detected)	-	M
0x0063	-	[0]	R_INT_EXTI2C_ACSEND	1	R	Interrupt factor: remote 2-wire access on Sub-Link end 1: Interrupt (access end is detected)	-	M
0x0064	-	[7:4]	reserved	4	-	-	-	-
0x0064	-	[3]	R_INTM_LOCKN	1	RW	Interrupt mask: LOCKN transition 0: Interrupt masked (related Interrupt Low fixed)	1'b0	M
0x0064	-	[2]	R_INTM_HTPDN	1	RW	Interrupt mask: HTPDN transition 0: Interrupt masked (related Interrupt Low fixed)	1'b0	M
0x0064	-	[1]	R_INTM_SLAVESIDE	1	RW	Interrupt mask: Sub-Link Slave side factor 0: Interrupt masked (related Interrupt Low fixed)	1'b0	M
0x0064	-	[0]	R_INTM_EXTI2C_ACSEND	1	RW	Interrupt mask: remote 2-wire access on Sub-Link end 0: Interrupt masked (related Interrupt Low fixed)	1'b0	M
0x0065	-	[7:4]	reserved	4	-	-	-	-
0x0065	-	[3]	R_INTC_LOCKN	1	W	Interrupt clear: LOCKN transition 1: Interrupt clear	-	M
0x0065	-	[2]	R_INTC_HTPDN	1	W	Interrupt clear: HTPDN transition 1: Interrupt clear	-	M
0x0065	-	[1]	R_INTC_SLAVESIDE	1	W	Interrupt clear: Sub-Link Slave side factor 1: Interrupt clear	-	M
0x0065	-	[0]	R_INTC_EXTI2C_ACSEND	1	W	Interrupt clear: remote 2-wire access on Sub-Link end 1: Interrupt clear	-	M
-	0x00E6	[7:2]	reserved	6	-	-	-	-
-	0x00E6	[1]	R_INT_EXTI2CS_BUSCLR	1	R	Interrupt factor: Sub-Link Slave 2-wire master bus clear end 1: Interrupt (bus clear end is detected)	-	S
-	0x00E6	[0]	R_INT_EXTI2CS_NACK	1	R	Interrupt factor: Sub-Link Slave 2-wire NACK detection 1: Interrupt (NACK is detected)	-	S
-	0x00E7	[7:2]	reserved	6	-	-	-	-
-	0x00E7	[1]	R_INTM_EXTI2CS_BUSCLR	1	RW	Interrupt mask: Sub-Link Slave 2-wire master bus clear end 0: Interrupt masked (related Interrupt Low fixed)	1'b0	S
-	0x00E7	[0]	R_INTM_EXTI2CS_NACK	1	RW	Interrupt mask: Sub-Link Slave 2-wire NACK detection 0: Interrupt masked (related Interrupt Low fixed)	1'b0	S
-	0x00E8	[7:2]	reserved	6	-	-	-	-
-	0x00E8	[1]	R_INTC_EXTI2CS_BUSCLR	1	W	Interrupt clear: Sub-Link Slave 2-wire master bus clear end 1: Interrupt clear	-	S
-	0x00E8	[0]	R_INTC_EXTI2CS_NACK	1	W	Interrupt clear: Sub-Link Slave 2-wire NACK detection 1: Interrupt clear	-	S
0x0069	-	[7:0]	reserved	8	-	-	-	-
0x006A	-	[7:0]	reserved	8	-	-	-	-
0x006B	-	[7:0]	reserved	8	-	-	-	-
0x006C	-	[7:0]	reserved	8	-	-	-	-
0x006D	-	[7:0]	reserved	8	-	-	-	-
0x006E	0x00EE	[7:4]	R_SLINK_ERR_SEL1	4	RW	Sub-Link Polling to inform error signal select #1	4'd0	MS
0x006E	0x00EE	[3:0]	R_SLINK_ERR_SEL0	4	RW	Sub-Link Polling to inform error signal select #0	4'd0	MS
0x006F	0x00EF	[7:4]	R_EXT_ERR_SEL1	4	RW	Sub-Link operator Selected Error#1 output to GPIO	4'd0	MS
0x006F	0x00EF	[3:0]	R_EXT_ERR_SEL0	4	RW	Sub-Link operator Selected Error#0 output to GPIO	4'd0	MS

Sub-Link		Bits	Register	width	R/W	Description	Default	Master or Slave related
Master Addr(h)	Slave Addr(h)							
0x0070	0x00F0	[7:0]	R_TUNING_ENABLE1	8	RW	Tuning register access Enable (1/2) 0x03: Enable others:Disable	8'd0	MS
0x0071	0x00F1	[7:5]	reserved	3	-	-	-	-
0x0071	0x00F1	[4]	R_BDCZ_HYS	1	RW	Hysteresis level select 0: 50mV 1:150mV	1'b0	MS
0x0071	0x00F1	[3:1]	reserved	3	-	-	-	-
0x0071	0x00F1	[0]	R_BDCZ_TERMEN	1	RW	Sub-Link Termination Enable 0:Disable 1:Enable	1'b1	MS
0x0072	0x00F2	[7:6]	reserved	2	-	-	-	-
0x0072	0x00F2	[5:4]	R_BDCZ_TERM_TX	2	RW	Sub-Link Tx Termination select 11=33ohm, 10=50ohm, 01=100ohm, 00=200ohm	2'b00	MS
0x0072	0x00F2	[3:2]	reserved	2	-	-	-	-
0x0072	0x00F2	[1:0]	R_BDCZ_DRIVE_TX	2	RW	Sub-Link Tx Drive current select 11=24mA, 10=12mA, 01=6mA, 00=3mA	2'b00	MS
0x0073	0x00F3	[7:6]	reserved	2	-	-	-	-
0x0073	0x00F3	[5:4]	R_BDCZ_TERM_RX	2	RW	Sub-Link Rx Termination select 11=33ohm, 10=50ohm, 01=100ohm, 00=200ohm	2'b00	MS
0x0073	0x00F3	[3:2]	reserved	2	-	-	-	-
0x0073	0x00F3	[1:0]	R_BDCZ_DRIVE_RX	2	RW	Sub-Link Rx Drive current select 11=24mA, 10=12mA, 01=6mA, 00=3mA	2'b00	MS
0x0074	0x00F4	[7:0]	ReservedX	8	RW	[Tuning register] must be left as default 0x01	8'd1	MS
0x0075	0x00F5	[7:0]	ReservedX	8	RW	[Tuning register] must be left as default 0x09	8'd9	MS
0x0076	0x00F6	[7:0]	R_SLINK_DATA_WIDTH	8	RW	[Tuning register] Sub-Link clock pattern unit period = R_SLINK_DATA_WIDTH<7:0>+1 must be set to 0x15 (default 0x0F is supposed to be changed)	8'h0F	MS
0x0077	0x00F7	[7:0]	reserved	8	-	-	-	-
0x0078	0x00F8	[7:0]	reserved	8	-	-	-	-
0x0079	0x00F9	[7:0]	reserved	8	-	-	-	-
0x007A	0x00FA	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	MS
0x007B	0x00FB	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	MS
0x007C	0x00FC	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	MS
0x007D	0x00FD	[7:0]	ReservedL	8	RW	Must be set 0	8'd0	MS
-	0x00FE	[7]	reserved	1	-	-	-	-
-	0x00FE	[6:4]	R_WB_MSB	3	RW	Word Address Bank MSB setting on 1Byte Word-addr. access from remote Sub-Link Master (e.g. THCV236-Q) (active only when R_WA_MODE=1) 3'd1=3'b001:"Word Address MSB[15:8]" bank is "8'h00" 3'd2=3'b010:"Word Address MSB[15:8]" bank is "8'h10" 3'd3=3'b011:"Word Address MSB[15:8]" bank is "8'h11" others:Reserved	3'b0	S
-	0x00FE	[3:1]	reserved	3	-	-	-	-
-	0x00FE	[0]	R_WA_MODE	1	RW	Word Address Byte number setting from remote Sub-Link Master 0:2Byte Word Address access from remote Sub-Link Master 1:1Byte Word Address access from remote Sub-Link Master (THCV236-Q setting is "1")	1'b0	S
0x007F	0x00FF	[7:0]	R_TUNING_ENABLE2	8	RW	Tuning register access Enable (2/2) 0x19: Enable others:Disable	8'd0	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1000	[7:6]	reserved	2	-	-	-
0x1000	[5:4]	reserved	2	-	-	-
0x1000	[3:1]	reserved	3	-	-	-
0x1000	[0]	R_VX1_LANE	1	R/W	V-by-One® HS output lane number setting 0:1lane 1:2lanes	1'h1
0x1001	[7]	reserved	1	-	-	-
0x1001	[6:4]	R_OUTPUT_FMT	3	R/W	V-by-One® HS output format setting 000:Main-Link Private Format (MPRF) 001:V-by-One® HS Standard YUV422(16bit)/RAW8 010:V-by-One® HS Standard RGB888 011:V-by-One® HS Standard RGB565 100:V-by-One® HS Standard RAW10 Mode1 101:V-by-One® HS Standard RAW12 Mode1 110: V-by-One® HS Standard RAW10 Mode2 111: V-by-One® HS Standard RAW12 Mode2	3'h0
0x1001	[3:2]	reserved	2	-	-	-
0x1001	[1:0]	R_PHMODE	2	R/W	V-by-One® HS output MIPI PH(Packet Header) timing setting 00:PH in normal data packet just after DE rise (THCV242-Q default) 01:PH in CTL packet of blanking period till 1pixel before DE rise 10,11:no PH	2'h0
0x1002	[7:6]	reserved	2	-	-	-
0x1002	[5]	R_HFSEL	1	R/W	V-by-One® HS HFSEL (High Freq. SElect) mode Enable 0:HF Mode Disable 1:HF Mode Enable	1'h0
0x1002	[4]	reserved	1	-	-	-
0x1002	[3:2]	R_FS_FE_SYNCEN	2	R/W	V-by-One® HS Vsync generation Enable at MIPI FS/FE (active only when R_VS_MODE=0) 00:Vsync pulse at both FS and FE (THCV242-Q default) 01:Vsync pulse at FS only 10:Vsync pulse at FE only 11:no Vsync pulse at FS nor FE	2'h0
0x1002	[1:0]	R_LS_LE_SYNCEN	2	R/W	V-by-One® HS Hsync generation Enable at MIPI LS/LE (active only when R_HS_MODE=00, 01) 00:Hsync pulse at both LS and LE (THCV242-Q default) 01:Hsync pulse at LS only 10:Hsync pulse at LE only 11:no Hsync pulse at LS nor LE	2'h0
0x1003	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1004	[7:2]	reserved	6	-	-	-
0x1004	[1]	R_VSYNC_POL	1	R/W	V-by-One® HS Vsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x1004	[0]	R_HSYNC_POL	1	R/W	V-by-One® HS Hsync polarity 0:High pulse (High active) (THCV242-Q default) 1:Low pulse (Low active)	1'h0
0x1005	[7:1]	reserved	7	-	-	-
0x1005	[0]	R_PLL_SNRST	1	R/W	Software Reset for PLL 0:Software Reset Active 1:Software Reset Release (PLL Normal Operation)	1'h0
0x1006	[7:1]	reserved	7	-	-	-
0x1006	[0]	R_TX_SNRST	1	R/W	Software Reset for V-by-One® HS TX 0:Software Reset Active 1:Software Reset Release (Vx1HS TX Normal Operation)	1'h0

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1007	[7:4]	reserved	4	-	-	-
0x1007	[3]	R_VS_MODE	1	R/W	V-by-One@ HS VSYNC output timing mode 0:MIPI FS/FE timing direct use mode (THCV242-Q default) 1:internally generated timing mode	1'h0
0x1007	[2:0]	R_VS_OFFSET	3	R/W	V-by-One@ HS internally generated VSYNC offset offset from FE = calculatedVS-HTOTAL x R_VS_OFFSET	3'h0
0x1008	[7:0]	R_VS_WIDTH_PIX	8	R/W	V-by-One@ HS internally generated Htotal setting Generated Htotal:calculatedVS-HTOTAL = R_VS_WIDTH_PIX x 16	8'h00
0x1009	[7:5]	reserved	3	-	-	-
0x1009	[4:2]	R_VS_WIDTH_LINE	3	R/W	V-by-One@ HS internally generated VSYNC pulse width VSYNC pulse width = calculatedVS-HTOTAL x R_VS_WIDTH_LINE	3'h0
0x1009	[1:0]	R_HS_MODE	2	R/W	V-by-One@ HS HSYNC output timing mode 00, 01:MIPI LS/LE timing direct use mode (THCV242-Q default) 10:internally generated timing mode1 11:internally generated timing mode2	2'h0
0x100A	[7:5]	reserved	3	-	-	-
0x100A	[4:0]	R_VACT_LINE[12:8]	5	R/W	V-by-One@ HS Vactive line skip number MSB	5'h00
0x100B	[7:0]	R_VACT_LINE[7:0]	8	R/W	V-by-One@ HS Vactive line skip number LSB	8'h00
0x100C	[7:2]	reserved	6	-	-	-
0x100C	[1:0]	R_HS_VB_EN	2	R/W	V-by-One@ HS HSYNC output in vertical blanking period setting 00, 01:no HSYNC output in Vblank 10:HSYNC output in Vblank, starting from FE 11:HSYNC output in Vblank, starting from FS, skipping Vactive	2'h0
0x100D	[7:0]	R_HS_VB_NUM	8	R/W	V-by-One@ HS HSYNC output number in vertical blanking period	8'h00

Addr(h)	Bits	Register	width	R/W	Description	Default
0x100E	[7:6]	R_CK1_FREQ	2	R/W	PLL Auto setting input frequency choice 2'h0: Reserved 2'h1: 37.125MHz 2'h2: 27MHz 2'h3: 24MHz	2'h0
0x100E	[5:0]	R_MIP1_MULT	6	R/W	PLL Auto setting multiplying ratio MIP1 data-rate vs. F(CK1) Below formula must be met to application condition. MIP1 Data-rate = F(CK1) *(R_MIP1_MULT+1)	6'hF
0x100F	[7:1]	reserved	7	-	-	-
0x100F	[0]	R_PLL_SET_MODE	1	R/W	PLL setting mode 0:PLL Auto setting mode 1:PLL Manual setting mode	1'h0
0x1010	[7:4]	R_DIVVAL	4	R/W	SSCG modulation frequency setting $f_{mod} = F(CK1) / (128 * R_DIVVAL)$	4'h0
0x1010	[3:0]	ReservedL	4	R/W	Must be set 0	4'h0
0x1011	[7:0]	R_PLL_SETTING[47:40]	8	R/W	PLL setting value, Feedback Divider value (integer part)	8'h00
0x1012	[7:0]	R_PLL_SETTING[39:32]	8	R/W	PLL setting value, Feedback Divider value (decimal part MSB)	8'h00
0x1013	[7:0]	R_PLL_SETTING[31:24]	8	R/W	PLL setting value, Feedback Divider value (decimal part)	8'h00
0x1014	[7:0]	R_PLL_SETTING[23:16]	8	R/W	PLL setting value, Feedback Divider value (decimal part LSB)	8'h00
0x1015	[7]	R_PLL_SETTING[15]	1	R/W	PLL setting value (Must be set 0)	1'h0
0x1015	[6:4]	R_PLL_SETTING[14:12]	3	R/W	PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2)	3'h0
0x1015	[3]	R_PLL_SETTING[11]	1	R/W	PLL setting value (Must be set 0)	1'h0
0x1015	[2:0]	R_PLL_SETTING[10:8]	3	R/W	PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2)	3'h0
0x1016	[7:0]	R_PLL_SETTING[7:0]	8	R/W	PLL setting value, ReservedH (must be set to 8'h01)	8'h00
0x1017	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1018	[7:0]	reserved	8	-	-	-
0x1019	[7:5]	reserved	3	-	-	-
0x1019	[4]	ReservedL	1	R/W	Must be set 0	1'h0
0x1019	[3:0]	R_SPREAD	4	R/W	SSCG modulation rate setting 4'h0 : modulation rate =0, 4'h1 : modulation rate =+/-0.1%, 4'h2 : modulation rate =+/-0.2%, ... 4'h5 : modulation rate =+/-0.5%, ... 4'hF : modulation rate =+/-1.5%	4'h3
0x101A	[7:5]	reserved	3	-	-	-
0x101A	[4]	ReservedL	1	R/W	Must be set 0	1'h0
0x101A	[3:1]	reserved	3	-	-	-
0x101A	[0]	R_DISABLE_SSCG	1	R/W	SSCG modulation Enable/Disable setting 0:Enable 1:Disable	1'h1

Addr(h)	Bits	Register	width	R/W	Description	Default
0x101B	[7:6]	reserved	2	-	-	-
0x101B	[5:4]	R_NHSEL	2	R/W	V-by-One® HS setting 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard Low Radiation Emission mode 11 : V-by-One® HS standard High Immunity Resistance mode	2'h3
0x101B	[3:2]	reserved	2	-	-	-
0x101B	[1]	ReservedL	1	R/W	Must be set 0	1'h0
0x101B	[0]	R_LFQEN	1	R/W	V-by-One® HS Low FeqModeEnable 0:Normal 1:Low Frequency Mode	1'h0
0x101C	[7:5]	reserved	3	-	-	-
0x101C	[4]	ReservedH	1	R/W	Must be set 1	1'h1
0x101C	[3:1]	reserved	3	-	-	-
0x101C	[0]	ReservedH	1	R/W	Must be set 1	1'h1
0x101D	[7:2]	reserved	6	-	-	-
0x101D	[1:0]	R_HTPDN_SEL	2	R/W	V-by-One® HS HTPDN assignment 00:Sub-Link at PDN1=1 / HTPDN pin input at PDN1=0, 01:Reserved, 10:forced Low (Must be set at V-by-One® HS Distribution Enable), 11:forced High	2'h0
0x101E	[7:6]	reserved	2	-	-	-
0x101E	[5:4]	R_LOCKN0_SEL	2	R/W	V-by-One® HS LOCKN for lane0 assignment 00:Sub-Link, 01:LOCKN pin input, 10:forced Low , 11:forced High	2'h0
0x101E	[3:2]	reserved	2	-	-	-
0x101E	[1:0]	R_LOCKN1_SEL	2	R/W	V-by-One® HS LOCKN for lane1 assignment 00:Sub-Link, 01:LOCKN pin input, 10:forced Low , 11:forced High	2'h0
0x101F	[7:0]	reserved	8	-	-	-
0x1020	[7:6]	R_ML0_PRE	2	R/W	V-by-One® HS lane0 Pre-Emphasis w hen R_ML0_DRV=00 00 : 0% 01 : 50% 10 : 100% 11 : not allow ed w hen R_ML0_DRV=01 00 : 0% 01 : 50% 10/11 : not allow ed w hen R_ML0_DRV=10 00 : 0% 01/10/11 : not allow ed	2'h0
0x1020	[5:4]	R_ML1_PRE	2	R/W	V-by-One® HS lane1 Pre-Emphasis w hen R_ML1_DRV=00 00 : 0% 01 : 50% 10 : 100% 11 : not allow ed w hen R_ML1_DRV=01 00 : 0% 01 : 50% 10/11 : not allow ed w hen R_ML1_DRV=10 00 : 0% 01/10/11 : not allow ed	2'h0
0x1020	[3:2]	R_ML0_DRV	2	R/W	V-by-One® HS lane0 Drive Strength Select 00: VTOD=200mV 01: VTOD=300mV 10: VTOD=400mV	2'h2
0x1020	[1:0]	R_ML1_DRV	2	R/W	V-by-One® HS lane1 Drive Strength Select 00: VTOD=200mV 01: VTOD=300mV 10: VTOD=400mV	2'h2
0x1021	[7:1]	reserved	7	-	-	-
0x1021	[0]	R_C_SNRST	1	R/W	MIPI CSI-2 Soft Reset 0:Reset 1:Reset Release (MIPI CSI-2 Normal Operation)	1'h1
0x1022	[7:1]	reserved	7	-	-	-
0x1022	[0]	R_DCLKSNRST	1	R/W	Digital logic Clock Soft Reset 0:Reset 1:Reset Release (Digital logic Clock Normal Operation)	1'h1
0x1023	[7:1]	reserved	7	-	-	-
0x1023	[0]	R_MCLKSNRST	1	R/W	MIPI Clock Soft Reset 0:Reset 1:Reset Release (MIPI Clock Normal Operation)	1'h1
0x1024	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1025	[7:1]	reserved	7	-	-	-
0x1025	[0]	R_RX_PN_SW	1	R/W	MPI P/N sw ap	1'h0
0x1026	[7:6]	R_RX_LANE_SEL0	2	R/W	MPI Data Lane RX0P/RX0N pin input mapping/sw ap select MPI standard format lane# assignment used on RX0P/RX0N input The same setting as R_RX_LANE_SEL1/2/3 is prohibited.	2'h0
0x1026	[5:4]	R_RX_LANE_SEL1	2	R/W	MPI Data Lane RX1P/RX1N pin input mapping/sw ap select MPI standard format lane# assignment used on RX1P/RX1N input The same setting as R_RX_LANE_SEL0/2/3 is prohibited.	2'h1
0x1026	[3:2]	R_RX_LANE_SEL2	2	R/W	MPI Data Lane RX2P/RX2N pin input mapping/sw ap select MPI standard format lane# assignment used on RX2P/RX2N input The same setting as R_RX_LANE_SEL0/1/3 is prohibited.	2'h2
0x1026	[1:0]	R_RX_LANE_SEL3	2	R/W	MPI Data Lane RX3P/RX3N pin input mapping/sw ap select MPI standard format lane# assignment used on RX3P/RX3N input The same setting as R_RX_LANE_SEL0/1/2 is prohibited.	2'h3
0x1027	[7:6]	reserved	2	-	-	-
0x1027	[5:0]	R_DATA_TYP_SEL	6	R/W	MPI ID error additional DataType(=DT) check option. [5]: 0=DATA_TYP Check ON, 1= All Data Typ Check OFF [4]:0=Generic Embedded 8bit non Image Data Check OFF, 1=ON [3]:0=Generic Blanking Data Check OFF, 1=ON [2]:0=Generic Null Check OFF, 1=ON [1]:0=Short Packet Reserved Check OFF, 1=ON [0]:0=Generic Short Packet Check OFF, 1=ON	6'h1f
0x1028	[7:0]	ReservedH	8	R/W	Must be set 1	8'hff
0x1029	[7:0]	ReservedH	8	R/W	Must be set 1	8'hff
0x102A	[7:0]	reserved	8	R/W	Must be set 8'h01	8'h01
0x102B	[7:0]	R_RX_THS_SETTLE	8	R/W	MPI THS(SETTLE-TERM_EN) setting	8'h01
0x102C	[7:5]	reserved	3	-	-	-
0x102C	[4]	reserved	1	-	-	-
0x102C	[3:1]	reserved	3	-	-	-
0x102C	[0]	R_RX_CLKLANE_EN	1	R/W	MPI Clock Lane Enable 0:Disable 1:Enable	1'h0
0x102D	[7:5]	reserved	3	-	-	-
0x102D	[4]	R_RX_DATA_LANE_EN	1	R/W	MPI Data Lane Enable 0:Disable 1:Enable, following R_RX_LANE_SEL_EN	1'h0
0x102D	[3:2]	reserved	2	-	-	-
0x102D	[1:0]	R_RX_LANE_SEL_EN	2	R/W	MPI Valid Data Lane number select 00:1Lane (lane0 Enable) 01,10:2Lane (lane<1:0> Enable) 11:4Lane (lane<3:0> Enable)	2'h3
0x102E	[7:0]	reserved	8	-	-	-
0x102F	[7:4]	ReservedL	4	R/W	Must be set 4'h0	4'h0
0x102F	[3:0]	reserved	4	-	-	-
0x1030	[7:0]	reserved	8	-	-	-
0x1031	[7:0]	reserved	8	-	-	-
0x1032	[7:0]	reserved	8	-	-	-
0x1033	[7:2]	reserved	6	-	-	-
0x1033	[1]	reserved	1	-	-	-
0x1033	[0]	ReservedH	1	R/W	Must be set 1	1'h1
0x1034	[7]	reserved	1	-	-	-
0x1034	[6:0]	ReservedL	7	R/W	Must be set 0	7'h0
0x1035	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1036	[7:1]	reserved	7	-	-	-
0x1036	[0]	R_COL_SEL	1	R/W	V-by-One® HS COL (COLor depth) Byte mode setting method 0:AUTO (COL_FMT defined by output format setting) 1:Manual (R_COL_MAN)	1'h0
0x1037	[7:6]	reserved	2	-	-	-
0x1037	[5:4]	R_COL_MAN[1:0]	2	R/W	V-by-One® HS Manual Color Depth Select 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved	2'h2
0x1037	[3:1]	reserved	3	-	-	-
0x1037	[0]	reserved	1	-	-	-
0x1038	[7]	reserved	1	-	-	-
0x1038	[6:4]	R_GPIO_SEL0	3	R/W	GPIO0 Error / status output select 3b'000:Normal 3b'001:R_ERR_SEL1(Internal Selected Error1) 3b'010:R_ERR_SEL2(Internal Selected Error2) 3b'011:R_EXT_ERR_SEL0(External Selected Error1) 3b'100:R_EXT_ERR_SEL1(External Selected Error2) Others:Normal	3'h0
0x1038	[3]	reserved	1	-	-	-
0x1038	[2:0]	R_GPIO_SEL1	3	R/W	GPIO1 Error / status output select 3b'000:Normal 3b'001:R_ERR_SEL1(Internal Selected Error1) 3b'010:R_ERR_SEL2(Internal Selected Error2) 3b'011:R_EXT_ERR_SEL0(External Selected Error1) 3b'100:R_EXT_ERR_SEL1(External Selected Error2) Others:Normal	3'h0
0x1039	[7]	reserved	1	-	-	-
0x1039	[6:4]	R_GPIO_SEL2	3	R/W	GPIO2 Error / status output select 3b'000:Normal 3b'001:R_ERR_SEL1(Internal Selected Error1) 3b'010:R_ERR_SEL2(Internal Selected Error2) 3b'011:R_EXT_ERR_SEL0(External Selected Error1) 3b'100:R_EXT_ERR_SEL1(External Selected Error2) Others:Normal	3'h0
0x1039	[3]	reserved	1	-	-	-
0x1039	[2:0]	R_GPIO_SEL3	3	R/W	GPIO3 Error / status output select 3b'000:Normal 3b'001:R_ERR_SEL1(Internal Selected Error1) 3b'010:R_ERR_SEL2(Internal Selected Error2) 3b'011:R_EXT_ERR_SEL0(External Selected Error1) 3b'100:R_EXT_ERR_SEL1(External Selected Error2) Others:Normal	3'h0
0x103A	[7:4]	reserved	4	-	-	-
0x103A	[3]	ReservedH	1	R/W	Must be set 1	1'h1
0x103A	[2:0]	reserved	3	R/W	Must be set 3'h3	3'h3
0x103B	[7]	reserved	1	-	-	-
0x103B	[6:4]	reserved	3	R/W	Must be set 3'h3	3'h3
0x103B	[3:2]	reserved	2	-	-	-
0x103B	[1:0]	reserved	2	-	-	-
0x103C	[7:1]	reserved	7	-	-	-
0x103C	[0]	ReservedH	1	R/W	Must be set 1	1'h1

Addr(h)	Bits	Register	width	R/W	Description	Default
0x103D	[7:4]	reserved	4	-	-	-
0x103D	[3:0]	R_GPIO_TYP	4	R/W	GPIO Mode Select [3]: 0:GPIO3 Register Mode, 1:GPIO3 Sub-Link Polling [2]: 0:GPIO2 Register Mode, 1:GPIO2 Sub-Link Polling [1]: 0:GPIO1 Register Mode, 1:GPIO1 Sub-Link Polling* [0]: 0:GPIO0 Register Mode, 1:GPIO0 Sub-Link Polling* *Sub-Link Polling is compatible with THCV236 GPIO Through mode	4'h0
0x103E	[7:4]	R_GPIO_OUT	4	R/W	GPIO0-3 Output Data Register [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0	4'h0
0x103E	[3:0]	R_GPIO_OEN	4	R/W	GPIO0-3 Input/Output Select [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:GPIO Output Mode 1:GPIO Input Mode	4'hf
0x103F	[7:4]	reserved	4	-	-	-
0x103F	[3:0]	R_GPIO_CMOSEN	4	R/W	GPIO0-3 CMOS/OpenDrain Select(for GPIO Output Mode) [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:OpenDrain 1:CMOS	4'h0
0x1040	[7:4]	reserved	4	-	-	-
0x1040	[3:0]	R_GPIO_TDRV	4	R/W	GPIO0-3 CMOS IO Drive Strength Select [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0: Normal Drive(4mA) 1: Strong Drive(8mA)	4'h0
0x1041	[7:1]	reserved	7	-	-	-
0x1041	[0]	R_INT_CMOSEN	1	R/W	[IO] INT CMOS/OpenDrain Select 0:OpenDrain 1:CMOS	1'h0
0x1042	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1043	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1044	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1045	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1046	[7:1]	reserved	7	-	-	-
0x1046	[0]	ReservedL	1	R/W	Must be set 0	1'h0
0x1047	[7]	ReservedL	1	R/W	Must be set 0	1'h0
0x1047	[6:0]	R_IO_DRV[7:0]	8	R/W	CMOS IO Drive Strength Select [6]:INT, [3]:CKO, [1]:SDA, [0]:SCL [5], [4], [2]:ReservedL 0: Normal Drive(4mA) 1: Strong Drive(8mA)	7'h00

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1048	[7:4]	reserved	4	-	-	-
0x1048	[3:0]	R_IOFLT_RANGE1	4	R/W	CMOS IO Input Signal Noise Filter Setting for PDN1, MSSEL, AIN 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*16 (ns)	4'h4
0x1049	[7:4]	reserved	4	-	-	-
0x1049	[3:0]	R_IOFLT_RANGE2	4	R/W	CMOS IO Input Signal Noise Filter Setting for SCL, SDA 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h2
0x104A	[7:4]	reserved	4	-	-	-
0x104A	[3:0]	R_IOFLT_RANGE3	4	R/W	CMOS IO Input Signal Noise Filter Setting for GPIO0 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104B	[7:4]	reserved	4	-	-	-
0x104B	[3:0]	R_IOFLT_RANGE4	4	R/W	CMOS IO Input Signal Noise Filter Setting for GPIO1 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104C	[7:4]	reserved	4	-	-	-
0x104C	[3:0]	R_IOFLT_RANGE5	4	R/W	CMOS IO Input Signal Noise Filter Setting for GPIO2 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104D	[7:4]	reserved	4	-	-	-
0x104D	[3:0]	R_IOFLT_RANGE6	4	R/W	CMOS IO Input Signal Noise Filter Setting for GPIO3 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104E	[7:4]	reserved	4	-	-	-
0x104E	[3:0]	R_IOFLT_RANGE7	4	R/W	CMOS IO Input Signal Noise Filter Setting for LOCKN 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*2 (ns)	4'h4
0x104F	[7:4]	reserved	4	-	-	-
0x104F	[3:0]	R_IOFLT_RANGE8	4	R/W	CMOS IO Input Signal Noise Filter Setting for PDN0 0:No Filter n:Filtering Glitch Signal w hen Pulse Width is Less than tOSC*n*16 (ns)	4'hF
0x1050	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1051	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1052	[7:2]	reserved	6	-	-	-
0x1052	[1]	R_ML_BETEN	1	R/W	V-by-One® HS Main Filed-BET Enable 0: Normal Mode 1: Filed-BET Mode	1'h0
0x1052	[0]	R_ML_OE_SWAP	1	R/W	V-by-One® HS 1st Pixel Start Timing Select 0:1st pixel assign on lane0 1:1st pixel assign on lane1	1'h0
0x1053	[7:1]	reserved	7	-	-	-
0x1053	[0]	R_DIST_EN	1	R/W	V-by-One® HS Distribution mode Enable 0:Disable 1:Enable	1'h0
0x1054	[7:1]	reserved	7	-	-	-
0x1054	[0]	R_CRC_OFF	1	R/W	V-by-One® HS CRC generator ON/OFF (ON default) 0: CRC output ON 1: CRC output OFF	1'h0
0x1055	[7:2]	reserved	6	-	-	-
0x1055	[1:0]	R_BITMAP_SEL	2	R/W	V-by-One® HS output data mapping select 00:MAP1, 01:MAP2, 10:MAP3, 11:MAP4	2'h0
0x1056	[7:1]	reserved	7	-	-	-
0x1056	[0]	R_SUB_BETEN	1	R/W	Sub-Link Filed-BET Enable 0: Normal Mode 1: Filed-BET Mode	1'h0
0x1057	[7:0]	R_SUB_BETSEL	8	R/W	Sub-Link Filed-BET MODE Signal Select [7:6] 10 : GPIO3 BETOUT 01 : GPIO3 LATEN 11,00 : Don't Care [5:4] 10 : GPIO2 BETOUT 01 : GPIO2 LATEN 11,00 : Don't Care [3:2] 10 : GPIO1 BETOUT 01 : GPIO1 LATEN 11,00 : Don't Care [1:0] 10 : GPIO0 BETOUT 01 : GPIO0 LATEN 11,00 : Don't Care	8'h06
0x1058	[7:4]	reserved	4	-	-	-
0x1058	[3:0]	R_GPIO_INTM_DETECT	4	R/W	Interrupt Mask for GPI [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:Interrupt No Mask 1:Interrupt Mask	4'hf
0x1059	[7:1]	reserved	7	-	-	-
0x1059	[0]	ReservedL	1	R/W	Must be set 0	1'h0
0x105A	[7:1]	reserved	7	-	-	-
0x105A	[0]	ReservedL	1	R/W	Must be set 0	1'h0
0x105B	[7:0]	R_PLL_CTERM	8	R/W	PLL parameter change automatic reset recovery time length 00 Disable(Disable Auto Soft Reset) 01 1*256*OSC (typ.3.2us) 02 2*256*OSC (typ.6.4us) 03 3*256*OSC (typ.9.6us) : : FE 254*256*OSC (typ.812.8us) FF 255*256*OSC (typ.816us)	8'h55
0x105C	[7:0]	R_TX_CTERM	8	R/W	V-by-One® HS parameter change automatic reset recovery time length 00 Disable(Disable Auto Soft Reset) 01 1*256*OSC (typ.3.2us) 02 2*256*OSC (typ.6.4us) 03 3*256*OSC (typ.9.6us) : : FE 254*256*OSC (typ.812.8us) FF 255*256*OSC (typ.816us)	8'h55
0x105D	[7:4]	R_ERR_SEL1	4	R/W	Internal Selected Error#1 output to GPIO and Sub-Link launcher	4'h0
0x105D	[3:0]	R_ERR_SEL2	4	R/W	Internal Selected Error#2 output to GPIO and Sub-Link launcher	4'h0
0x105E	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x105F	[7:1]	reserved	7	-	-	-
0x105F	[0]	R_BISTEN	1	R/W	BIST Enable 0:Disable 1:Enable	1'h0
0x1060	[7:5]	reserved	3	-	-	-
0x1060	[4:0]	R_BIST_PTN	5	R/W	BIST pattern select 00: Automatic pattern sw itching repetition from 01 to 0E 01~05: raster patterns 06~07: color bar patterns 08~0B: ramp patterns 0C: 16x16 pixel checker 0D: Frame 0E: Sub checker 0F: reserved 10: Frame2 11~16: checkers 17: Cursor 18~1F: reserved	5'h00
0x1061	[7:0]	R_GS_SEL_R	8	R/W	BIST Gradient Setting Red 00:Black <=> FF:Red	8'hff
0x1062	[7:0]	R_GS_SEL_G	8	R/W	BIST Gradient Setting Green 00:Black <=> FF:Green	8'hff
0x1063	[7:0]	R_GS_SEL_B	8	R/W	BIST Gradient Setting Blue 00:Black <=> FF:Blue	8'hff
0x1064	[7:4]	reserved	4	-	-	-
0x1064	[3:0]	R_CURSOR_H[11:8]	4	R/W	BIST Cursor position on horizontal direction	4'h0
0x1065	[7:0]	R_CURSOR_H[7:0]	8	R/W	BIST Cursor position on horizontal direction	8'h00
0x1066	[7:4]	reserved	4	-	-	-
0x1066	[3:0]	R_CURSOR_V[11:8]	4	R/W	BIST Cursor position on vertical direction	4'h0
0x1067	[7:0]	R_CURSOR_V[7:0]	8	R/W	BIST Cursor position on vertical direction	8'h00
0x1068	[7:2]	reserved	6	-	-	-
0x1068	[1:0]	R_HACTIVE_V[9:8]	2	R/W	BIST Hactive pixel number setting Hactive pixel number = "R_HACTIVE_V" x4	2'h1
0x1069	[7:0]	R_HACTIVE_V[7:0]	8	R/W	BIST Hactive pixel number Hactive pixel number = "R_HACTIVE_V" x4	8'hE0
0x106A	[7:3]	reserved	5	-	-	-
0x106A	[2:0]	R_VACTIVE_V[10:8]	3	R/W	BIST Vactive line number (must be even number)	3'h4
0x106B	[7:0]	R_VACTIVE_V[7:0]	8	R/W	BIST Vactive line number (must be even number)	8'h38
0x106C	[7:2]	reserved	6	-	-	-
0x106C	[1:0]	R_HBLANK_V[9:8]	2	R/W	BIST Hblank pixel number setting Hblank pixel number = "R_HBLANK_V" x4	2'h0
0x106D	[7:0]	R_HBLANK_V[7:0]	8	R/W	BIST Hblank pixel number Hblank pixel number = "R_HBLANK_V" x4	8'h46
0x106E	[7:2]	reserved	6	-	-	-
0x106E	[1:0]	R_VBLANK_V[9:8]	2	R/W	BIST Vblank line number	2'h0
0x106F	[7:0]	R_VBLANK_V[7:0]	8	R/W	BIST Vblank line number	8'h27
0x1070	[7:1]	reserved	7	-	-	-
0x1070	[0]	R_HBP_V[8]	1	R/W	BIST Hbackporch pixel number setting Hbackporch pixel number = "R_HBP_V" x4	1'h0
0x1071	[7:0]	R_HBP_V[7:0]	8	R/W	BIST Hbackporch pixel number setting Hbackporch pixel number = "R_HBP_V" x4	8'h28
0x1072	[7]	reserved	1	-	-	-
0x1072	[6:0]	R_VBP_V	7	R/W	BIST Vbackporch line number	7'h10
0x1073	[7:0]	reserved	8	-	-	-
0x1074	[7:0]	reserved	8	-	-	-
0x1075	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1076	[7]	ReservedL	1	R/W	Must be set 0	1'h0
0x1076	[6]	R_CKOSTOP	1	R/W	CKO output source select 0:CKI, 1: Low fix	1'h1
0x1076	[5]	reserved	1	-	-	-
0x1076	[4]	ReservedH	1	R/W	Must be set 1	1'h1
0x1076	[3]	ReservedL	1	R/W	Must be set 0	1'h0
0x1076	[2]	ReservedL	1	R/W	Must be set 0	1'h0
0x1076	[1]	reserved	1	-	-	-
0x1076	[0]	ReservedL	1	R/W	Must be set 0	1'h0
0x1077	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1078	[7]	R_ERR_CRC_MSK	1	R/W	Interrupt mask: MIPI CRC error 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x1078	[6]	R_ERR_ECCCOR_MSK	1	R/W	Interrupt mask: MIPI ECC 1bit error 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x1078	[5]	R_ERR_ECCDBL_MSK	1	R/W	Interrupt mask: MIPI ECC 2bit error 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x1078	[4]	R_ERR_ID_MSK	1	R/W	Interrupt mask: MIPI ID error (MIPI ID is not equal to Main-Link setting) 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x1078	[3:0]	R_ERR_SOT_HS_MSK	4	R/W	Interrupt mask: MIPI SoT sequence not detected error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 4'hf: Interrupt masked (related Interrupt Low fixed)	4'hf
0x1079	[7:4]	R_RX_IGNORE_DERR	4	R/W	Interrupt mask: MIPI SYNCCODE SoT 1bit error [7]:lane3, [6]:lane2, [5]:lane1, [4]:lane0 4'h0: Interrupt masked (related Interrupt Low fixed)	4'h0
0x1079	[3:0]	R_ERR_FRAME_SYNC_MSK	4	R/W	Interrupt mask: MIPI FRAME SYNC FS/FE position error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 4'hf: Interrupt masked (related Interrupt Low fixed)	4'hf
0x107A	[7:0]	reserved	8	R/W	Must be set 8'h1f	8'h1f
0x107B	[7:5]	reserved	3	-	-	-
0x107B	[4:0]	R_ERR_CTL_MSK	5	R/W	Interrupt mask: MIPI control state error [4]:clock lane, [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 5'h1f: Interrupt masked (related Interrupt Low fixed)	5'h1f
0x107C	[7:6]	reserved	2	-	-	-
0x107C	[5]	R_DHNDL_INT_MSK	1	R/W	Interrupt mask: Main-Link Data Handle error 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x107C	[4]	R_PLL_SET_NG_MSK	1	R/W	Interrupt mask: PLL auto configuration setting error 1: Interrupt masked (related Interrupt Low fixed)	1'h1
0x107C	[3:0]	R_INT_FS_MSK	4	R/W	Interrupt mask: MIPI FS [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 4'hf: Interrupt masked (related Interrupt Low fixed)	4'hf
0x107D	[7:4]	reserved	4	-	-	-
0x107D	[3:0]	R_INT_FE_MSK	4	R/W	Interrupt mask: MIPI FE [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 4'hf: Interrupt masked (related Interrupt Low fixed)	4'hf
0x107E	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x107F	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1080	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1081	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1082	[7:5]	reserved	3	R/W	-	-
0x1082	[4]	R_CRC_CMP_OFF	1	R/W	MIPI CRC error monitoring OFF Enable/Disable 0:Enable 1:Disable	1'h0
0x1082	[3:1]	reserved	3	R/W	-	-
0x1082	[0]	R_ECC_CMP_OFF	1	R/W	MIPI ECC error monitoring and correction OFF Enable/Disable 0:Enable 1:Disable	1'h0
0x1083	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1084	[7]	reserved	1	-	-	-
0x1084	[6:4]	R_SUB_GPIO0_SEL	3	R/W	GPIO0 assignment to Sub-Link packet# at R_GPIO_TYF[0]=1 3b'000: Sub-Link GPO[0]/GP[0] packet 3b'001: Sub-Link GPO[1]/GP[1] packet 3b'010: Sub-Link GPO[2]/GP[2] packet 3b'011: Sub-Link GPO[3]/GP[3] packet 3b'100: Sub-Link GPO[4]/GP[4] packet 3b'101: Sub-Link GPO[5]/GP[5] packet 3b'110: Sub-Link GPO[6]/GP[6] packet 3b'111: Sub-Link GPO[7]/GP[7] packet	3'h0
0x1084	[3]	reserved	1	-	-	-
0x1084	[2:0]	R_SUB_GPIO1_SEL	3	R/W	GPIO1 assignment to Sub-Link packet# at R_GPIO_TYF[1]=1 3b'000: Sub-Link GPO[0]/GP[0] packet 3b'001: Sub-Link GPO[1]/GP[1] packet 3b'010: Sub-Link GPO[2]/GP[2] packet 3b'011: Sub-Link GPO[3]/GP[3] packet 3b'100: Sub-Link GPO[4]/GP[4] packet 3b'101: Sub-Link GPO[5]/GP[5] packet 3b'110: Sub-Link GPO[6]/GP[6] packet 3b'111: Sub-Link GPO[7]/GP[7] packet	3'h0
0x1085	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1086	[7:0]	reserved	8	-	-	-
0x1087	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1088	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x1089	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x108A	[7:0]	ReservedL	8	R/W	Must be set 0	8'h00
0x108B	[7:0]	ReservedH	8	R/W	Must be set 8'hff	8'hff
0x108C	[7:0]	reserved	8	-	-	-
0x108D	[7:0]	reserved	8	-	-	-
0x108E	[7:0]	reserved	8	-	-	-
0x108F	[7:0]	reserved	8	-	-	-
0x1090 ~ 0x10FE	[7:0]	reserved	8	-	-	-
0x10FF	[7:0]	R_REGSNRST	8	R/W	Register Soft Reset AA:Reset others:Reserved	8'h00

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1100	[7:0]	reserved	8	-	-	-
0x1101	[7:0]	reserved	8	-	-	-
0x1102	[7:0]	reserved	8	-	-	-
0x1103	[7:0]	reserved	8	-	-	-
0x1104	[7:0]	reserved	8	-	-	-
0x1105	[7:0]	reserved	8	-	-	-
0x1106	[7:6]	R_RX_VC	2	R	MPII received VC data	-
0x1106	[5:0]	reserved	6	-	-	-
0x1107	[7:6]	reserved	2	-	-	-
0x1107	[5:0]	R_RX_DATA_TYP	6	R	MPII received DT data	-
0x1108	[7:0]	R_RX_WC[15:8]	8	R	MPII received WC data MSB	-
0x1109	[7:0]	R_RX_WC[7:0]	8	R	MPII received WC data LSB	-
0x110A	[7:0]	R_RX_V_NUM0[15:8]	8	R	MPII received Frame number (VC0) MSB	-
0x110B	[7:0]	R_RX_V_NUM0[7:0]	8	R	MPII received Frame number (VC0) LSB	-
0x110C	[7:0]	R_RX_V_NUM1[15:8]	8	R	MPII received Frame number (VC1) MSB	-
0x110D	[7:0]	R_RX_V_NUM1[7:0]	8	R	MPII received Frame number (VC1) LSB	-
0x110E	[7:0]	R_RX_V_NUM2[15:8]	8	R	MPII received Frame number (VC2) MSB	-
0x110F	[7:0]	R_RX_V_NUM2[7:0]	8	R	MPII received Frame number (VC2) LSB	-
0x1110	[7:0]	R_RX_V_NUM3[15:8]	8	R	MPII received Frame number (VC3) MSB	-
0x1111	[7:0]	R_RX_V_NUM3[7:0]	8	R	MPII received Frame number (VC3) LSB	-
0x1112	[7:0]	R_RX_L_NUM0[15:8]	8	R	MPII received Line number (VC0) MSB	-
0x1113	[7:0]	R_RX_L_NUM0[7:0]	8	R	MPII received Line number (VC0) LSB	-
0x1114	[7:0]	R_RX_L_NUM1[15:8]	8	R	MPII received Line number (VC1) MSB	-
0x1115	[7:0]	R_RX_L_NUM1[7:0]	8	R	MPII received Line number (VC1) LSB	-
0x1116	[7:0]	R_RX_L_NUM2[15:8]	8	R	MPII received Line number (VC2) MSB	-
0x1117	[7:0]	R_RX_L_NUM2[7:0]	8	R	MPII received Line number (VC2) LSB	-
0x1118	[7:0]	R_RX_L_NUM3[15:8]	8	R	MPII received Line number (VC3) MSB	-
0x1119	[7:0]	R_RX_L_NUM3[7:0]	8	R	MPII received Line number (VC3) LSB	-
0x111A	[7:0]	reserved	8	-	-	-
0x111B	[7:0]	R_ECC_DATA	8	R	MPII received ECC data	-
0x111C	[7:0]	R_CRC_DATA[15:8]	8	R	MPII received CRC data MSB	-
0x111D	[7:0]	R_CRC_DATA[7:0]	8	R	MPII received CRC data LSB	-
0x111E	[7:0]	reserved	8	-	-	-
0x111F	[7:0]	reserved	8	-	-	-
0x1120	[7:0]	reserved	8	-	-	-
0x1121	[7:4]	R_GPIO_IMON	4	R	GPIO0-3 Input Monitor Register [7]:GPIO3, [6]:GPIO2, [5]:GPIO1, [4]:GPIO0	-
0x1121	[3:0]	R_GPIO_INT_DETECT	4	R	Interrupt Signal for GPI [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:No Interrupt 1:Interrupt (detect for asserted or negated of GPI Input)	-
0x1122	[7:4]	reserved	4	-	-	-
0x1122	[3:0]	R_GPIO_INTC_DETECT	4	W	Interrupt Clear for GPI [3]:GPIO3, [2]:GPIO2, [1]:GPIO1, [0]:GPIO0 0:Interrupt No Clear 1:Interrupt Clear	-
0x1123	[7:0]	reserved	8	-	-	-
0x1124	[7:0]	reserved	8	-	-	-
0x1125	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1126	[7:0]	C_PLL_SETTING[7:0]	8	R	PLL setting calculated value as a combination of parameters, ReservedH (monitored as 8'h01)	-
0x1127	[7:0]	reserved	8	-	-	-
0x1128	[7:0]	C_PLL_SETTING[47:40]	8	R	PLL setting calculated value as a combination of parameters, Feedback Divider (integer part) (e.g. as a result of PLL auto setting)	-
0x1129	[7:0]	C_PLL_SETTING[39:32]	8	R	PLL setting calculated value as a combination of parameters, Feedback Divider (decimal part MSB) (e.g. as a result of PLL auto setting)	-
0x112A	[7:0]	C_PLL_SETTING[31:24]	8	R	PLL setting calculated value as a combination of parameters, Feedback Divider (decimal part) (e.g. as a result of PLL auto setting)	-
0x112B	[7:0]	C_PLL_SETTING[23:16]	8	R	PLL setting calculated value as a combination of parameters, Feedback Divider (decimal part LSB) (e.g. as a result of PLL auto setting)	-
0x112C	[7:4]	reserved	4	-	-	-
0x112C	[3]	C_PLL_SETTING[15]	1	R	PLL setting calculated value (monitored as 0)	-
0x112C	[2:0]	C_PLL_SETTING[14:12]	3	R	PLL setting calculated value as a combination of parameters, OutDiv1 (e.g. as a result of PLL auto setting)	-
0x112D	[7:4]	reserved	4	-	-	-
0x112D	[3]	C_PLL_SETTING[11]	1	R	PLL setting calculated value (monitored as 0)	-
0x112D	[2:0]	C_PLL_SETTING[10:8]	3	R	PLL setting calculated value as a combination of parameters, OutDiv2 (e.g. as a result of PLL auto setting)	-
0x112E	[7:0]	reserved	8	-	-	-
0x112F	[7:1]	reserved	7	-	-	-
0x112F	[0]	C_PLL_SET_NG	1	R	PLL Auto Setting control invalid indicator 0: PLL Auto Setting control valid or PLL Manual setting mode 1: PLL Auto Setting control invalid	-
0x1130	[7:1]	reserved	7	-	-	-
0x1130	[0]	C_LOCKN0_O	1	R	V-by-One® HS LOCKN status for lane0 on calculated assignment as a combination of parameters (Sub-Link or External LOCKN)	-
0x1131	[7:1]	reserved	7	-	-	-
0x1131	[0]	C_LOCKN1_O	1	R	V-by-One® HS LOCKN status for lane1 on calculated assignment as a combination of parameters (Sub-Link or External LOCKN)	-
0x1132	[7:2]	reserved	6	-	-	-
0x1132	[1:0]	C_COL_O	2	R	V-by-One® HS calculated Byte mode as a combination of parameters, (e.g. Manual Color Depth Select) 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved	-
0x1133	[7:1]	reserved	7	-	-	-
0x1133	[0]	C_HTPDN_O	1	R	V-by-One® HS HTPDN status on calculated assignment as a combination of parameters (Sub-Link or External HTPDN)	-
0x1134	[7:1]	reserved	7	-	-	-
0x1134	[0]	C_LANE0EN_O	1	R	V-by-One® HS Lane0 Enable status on calculated assignment as a combination of parameters (e.g. Distribution mode)	-
0x1135	[7:1]	reserved	7	-	-	-
0x1135	[0]	C_LANE1EN_O	1	R	V-by-One® HS Lane1 Enable status on calculated assignment as a combination of parameters (e.g. Distribution mode)	-
0x1136	[7:0]	reserved	8	-	-	-
0x1137	[7:0]	reserved	8	-	-	-
0x1138	[7:0]	reserved	8	-	-	-
0x1139	[7:0]	reserved	8	-	-	-
0x113A	[7:0]	reserved	8	-	-	-
0x113B	[7:0]	reserved	8	-	-	-
0x113C	[7:0]	reserved	8	-	-	-
0x113D	[7:0]	reserved	8	-	-	-
0x113E	[7:0]	reserved	8	-	-	-
0x113F	[7:0]	reserved	8	-	-	-
0x1140	[7:0]	reserved	8	-	-	-
0x1141	[7:0]	reserved	8	-	-	-
0x1142	[7:0]	reserved	8	-	-	-
0x1143	[7:0]	reserved	8	-	-	-
0x1144	[7:0]	reserved	8	-	-	-
0x1145	[7:0]	reserved	8	-	-	-
0x1146	[7:0]	reserved	8	-	-	-
0x1147	[7:0]	reserved	8	-	-	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1148	[7]	R_ERR_CRC	1	R	Interrupt factor: MIPI CRC error 1: Interrupt (error is detected)	-
0x1148	[6]	R_ERR_ECCCOR	1	R	Interrupt factor: MIPI ECC 1bit error 1: Interrupt (error is detected)	-
0x1148	[5]	R_ERR_ECCDBL	1	R	Interrupt factor: MIPI ECC 2bit error 1: Interrupt (error is detected)	-
0x1148	[4]	R_ERR_ID	1	R	Interrupt factor: MIPI ID error (MIPI ID is not equal to Main-Link setting) 1: Interrupt (error is detected)	-
0x1148	[3:0]	R_ERR_SOTSYNC	4	R	Interrupt factor: MIPI SoT sequence not detected error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt (error is detected)	-
0x1149	[7:4]	R_ERR_SYNCCODE	4	R	Interrupt factor: MIPI SYNCCODE SoT 1bit error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt (error is detected)	-
0x1149	[3:0]	R_ERR_FRAMESYNC	4	R	Interrupt factor: MIPI FRAME Sync FS/FE position error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt (error is detected)	-
0x114A	[7:0]	reserved	8	-	-	-
0x114B	[7:5]	reserved	3	-	-	-
0x114B	[4:0]	R_ERR_CONTROL	5	R	Interrupt factor: MIPI Control state error [4]:clock lane, [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt (error is detected)	-
0x114C	[7:4]	R_INT_FS	4	R	Interrupt factor: MIPI Frame Start (FS) 1: Interrupt (event is detected)	-
0x114C	[3:0]	R_INT_FE	4	R	Interrupt factor: MIPI Frame End (FE) 1: Interrupt (event is detected)	-
0x114D	[7:1]	reserved	7	-	-	-
0x114D	[0]	R_DHNDL_INT	1	R	Interrupt factor: Main-Link Data Handle error 1: Interrupt (error is detected)	-
0x114E	[7]	R_CRC_ERR_CLR	1	W	Interrupt clear: MIPI CRC error 1: Interrupt clear	-
0x114E	[6]	R_ECC_CRCT_ERR_CLR	1	W	Interrupt clear: MIPI ECC 1bit error 1: Interrupt clear	-
0x114E	[5]	R_ECC_DOUBLE_ERR_CLR	1	W	Interrupt clear: MIPI ECC 2bit error 1: Interrupt clear	-
0x114E	[4]	R_ERR_ID_CLR	1	W	Interrupt clear: MIPI ID error (MIPI ID is not equal to Main-Link setting) 1: Interrupt clear	-
0x114E	[3:0]	R_SOT_SYNC_HS_CLR	4	W	Interrupt clear: MIPI SoT sequence not detected error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt clear	-
0x114F	[7:4]	R_SOT_SYNCCODE_CLR	4	W	Interrupt clear: MIPI SYNCCODE SoT 1bit error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt clear	-
0x114F	[3:0]	R_ERR_FR_SYNC_ON_CLR	4	W	Interrupt clear: MIPI FRAME Sync FS/FE position error [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt clear	-

Addr(h)	Bits	Register	width	R/W	Description	Default
0x1150	[7:0]	reserved	8	-	-	-
0x1151	[7:5]	reserved	3	-	-	-
0x1151	[4:0]	R_ERR_CTL_CLR	5	W	Interrupt clear: MIPI Control state error [4]:clock lane, [3]:lane3, [2]:lane2, [1]:lane1, [0]:lane0 1: Interrupt clear	-
0x1152	[7:4]	R_INT_FS_ON_CLR	4	W	Interrupt clear: MIPI Frame Start (FS) 1: Interrupt clear	-
0x1152	[3:0]	R_INT_FE_ON_CLR	4	W	Interrupt clear: MIPI Frame End (FE) 1: Interrupt clear	-
0x1153	[7:1]	reserved	7	-	-	-
0x1153	[0]	R_DHNDL_INT_CLR	1	W	Interrupt clear: Main-Link Data Handle error 1: Interrupt clear	-
0x1154	[7:1]	reserved	7	-	-	-
0x1154	[0]	R_DHNDL_ERR	1	R	Error indicator: Main-Link Data Handle error 1: Error	-
0x1155	[7:0]	R_RX_CRC_ERR_CNT[15:8]	8	R	Error counter: MIPI CRC error MSB	-
0x1156	[7:0]	R_RX_CRC_ERR_CNT[7:0]	8	R	Error counter: MIPI CRC error LSB	-
0x1157	[7:0]	R_RX_ECC_ERR_CRCT_CNT[15:8]	8	R	Error counter: MIPI ECC 1bit error MSB	-
0x1158	[7:0]	R_RX_ECC_ERR_CRCT_CNT[7:0]	8	R	Error counter: MIPI ECC 1bit error LSB	-
0x1159	[7:0]	R_RX_ECC_ERR_DBLE_CNT[15:8]	8	R	Error counter: MIPI ECC 2bit error MSB	-
0x115A	[7:0]	R_RX_ECC_ERR_DBLE_CNT[7:0]	8	R	Error counter: MIPI ECC 2bit error LSB	-
0x115B	[7:3]	reserved	5	-	-	-
0x115B	[2]	R_CRC_ERR_CNT_CLR	1	W	Error counter clear: MIPI CRC error 1: Error counter clear	-
0x115B	[1]	R_ECC_ERR_CRCT_CNT_CLR	1	W	Error counter clear: MIPI ECC 1bit error 1: Error counter clear	-
0x115B	[0]	R_ECC_ERR_DBLE_CNT_CLR	1	W	Error counter clear: MIPI ECC 2bit error 1: Error counter clear	-
0x115C	[7:0]	reserved	8	-	-	-
0x115D	[7:1]	reserved	7	-	-	-
0x115D	[0]	R_PLL_LOCK	1	R	PLL Lock Signal 1: PLL Lock to CKI input	-
0x115E	[7:0]	reserved	8	-	-	-
0x115F	[7:0]	reserved	8	-	-	-
0x1060 ~ 0x11FE	[7:0]	reserved	8	-	-	-
0x11FF	[7:0]	reserved	8	-	-	-

Notices and Requests

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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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