THPM4401A

4-28V Input 8A Output POL Power Module

Features

- Integrated Point of Load power module using in Inductor technology
- Small Footprint, low-profile, 15.2mm x 9.2mm x 3mm, with LGA Package (0.63 mm pads)
- Efficiency of 94% at 4A and 93% at 6A for 5V output, 12V input
- Up to 8A maximum output current; up to 6A at 85°C ambient with no air flow
- Single resistor output voltage programming for voltages from 0.6V to 5V
- Output voltage remote sensing
- Input voltage range 4V to 28V
- Pre-bias start up capability
- Enable signal input and Power Good signal output
- Output voltage sequencing
- Programmable Under Voltage Lock Out (UVLO)
- Output Over-Current Protection (OCP)
- Operating temperature range -40°C to 85°C

Applications

- Broadband and communications equipment
- DSP and FPGA Point of Load applications
- High density distributed power systems
- PCI express / PXI express
- Automated test and medical equipment

Description

THPM4401A is an easy-to-use 8A output integrated Point of Load (POL) power supply module. It contains power MOSFETs, driver, PWM controller, a high-performance inductor, input and output capacitors and other passive components in one low profile LGA package using Inductor technology.

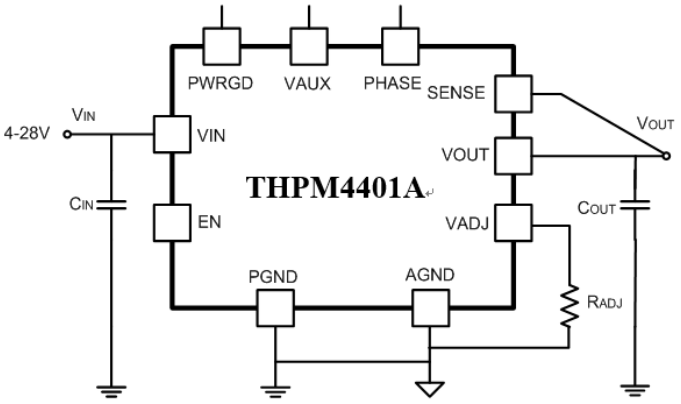
There is no need for loop compensation, sensitive PCB layout, inductor selection, or in-circuit production testing.

The THPM4401A can be programmed for any output voltage between 0.6V and 5.0V using a single external resistor. For an output voltage of 0.6V no resistor is required.

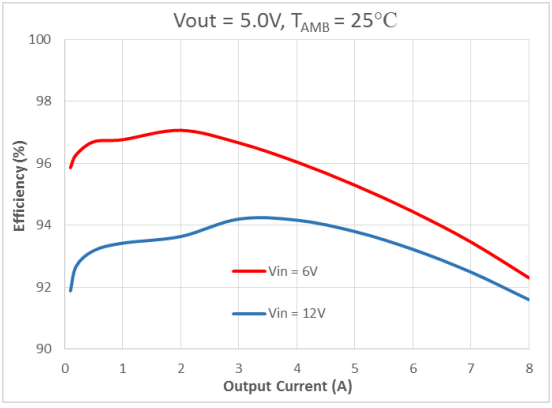
The THPM4401A delivers up to 8A load current, and can deliver up to 6A at 85°C ambient temperature with no airflow.

Small size (15.2mm x 9.2mm) and low profile (3mm) allows the THPM4401A to be placed very close to its load, or on the back side of the PCB board for high density applications.

SIMPLIFIED APPLICATION



EFFICIENCY VS LOAD CURRENT



ABSOLUTE MAXIMUM(1) RATINGS over operating temperature range (unless otherwise noted)

		VALUE		Unit
		MIN	MAX	
Inputs	VIN	-0.3	30	V
	EN	-0.3	30	V
	VSENSE	-0.3	30	V
	VADJ	-0.3	4	V
Outputs	VOUT	-0.6	10	V
	PHASE	-0.6	VIN	V
	PWRGD	-0.3	30	V
	VAUX	-0.3	4	V
Temperature	Operating Junction Temperature	-	150	℃
	Storage Temperature	-55	150	℃
	Peak solder reflow body temperature	-	245	℃

(1) Stresses beyond these absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Output Voltage	Module Part Number	Pad Finish	Package Type	Temperature Range
Adjustable	THPM4401A	Au (RoHS)	LGA	-40˚C to 85˚C

ELECTRICAL CHARACTERISTICS

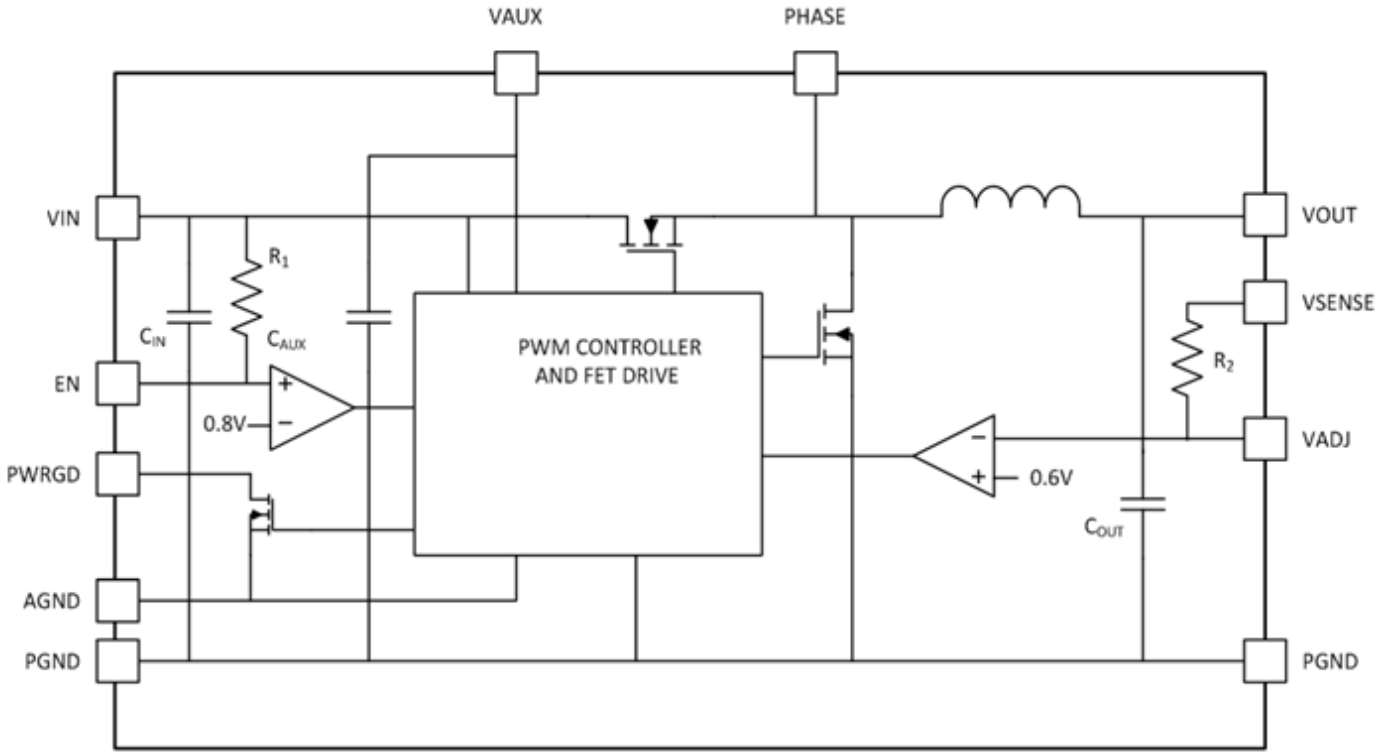
The electrical performance is based on the following conditions unless otherwise stated: 25°C ambient temperature, no air flow; V_{IN} = 12V, I_{OUT} = 6A, C_{IN} = 4×22μF ceramic, C_{OUT} = 2×100μF ceramic.

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Specifications							
V_{IN}	Input voltage [**Note 1**]	Over I_{OUT} range		4	12	28	V
V_{START}	Start up voltage [**Note 2**]	Over I_{OUT} range		-	3.65	-	V
V_{EN_ON}	Enable on voltage	Enable high voltage (module turned on)		0.8	-	-	V
V_{EN_OFF}	Enable off voltage	Enable low voltage (module turned off)		-	-	0.4	V
UVLO Under Voltage Lock Out [**Note 2**]				-	3.55	-	V
UVLO Hysteresis				-	0.1	-	V
Output Specifications							
I_{OUT}:	Output continuous current	T_A = -40°C to 85°C, natural convection		0	-	6	A
I_{OUT}:	Maximum current	T_A = -40°C to 50°C, refer to Fig. 29-Fig. 31		-	-	8	A
V_{OUT}	Set point accuracy [**Note 3**]	T_A = 25°C, V_{IN} = 12V, I_{OUT} = 3A		-	±1.5%	-	-
	Temperature variation	-40°C < T_A < +85°C, I_{OUT} = 3A		-	±1%	-	-
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 3A		-	±0.5%	-	-
	Load regulation	Over I_{OUT} range, T_A = 25°C, V_{IN} = 12V		-	±1%	-	-
$V_{OUT(adj)}$: Output voltage adjust range		Over I_{OUT} range [**Note 1**]		0.6	-	5.0	V
V_{o_rip},	Output voltage ripple	20MHz bandwidth, V_{IN} = 12V, I_{OUT} = 6A		-	20	-	mVpp
V_{AUX}: Auxiliary output		Output voltage		-	3.3	-	V
OVP	Over-voltage Protection	OVP threshold (percentage of nominal)		115%	120%	125%	-
		OVP shutdown delay		-	20	-	μs
PWRGD	Power Good Signal	V_{OUT} rising (% of V_{OUT})	PWRGD high	88%	90%	92%	-
			PWRGD delay	-	10	-	μs
		V_{OUT} falling (% of V_{OUT})	Hysteresis	-	2%	-	-
F_S	Switching frequency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A		-	760	-	kHz
Performance Specifications							
η	Efficiency (V_{OUT} = 5V)	V_{IN} = 12V	I_{OUT} = 3A	-	94.2%	-	-
			I_{OUT} = 6A	-	93.2%	-	-
Current Limit and Thermal Specifications							
I_{LIM}	Current Limit Point	V_{IN} = 12V		-	11	-	A
Thermal shutdown (die temperature)		Thermal shutdown		-	150	-	°C
		Thermal shutdown recovery hysteresis		-	15	-	°C

Note 1: There must be enough margin between the input and output voltage (refer to Fig. 15 on page 11)
Note 2: Startup voltage and UVLO are with no external resistor; startup and UVLO can be increased using an external programming resistor – refer to Startup Voltage on page 13.
Note 3: With 0.1% tolerance external voltage set resistor.

POWER MODULE INFORMATION

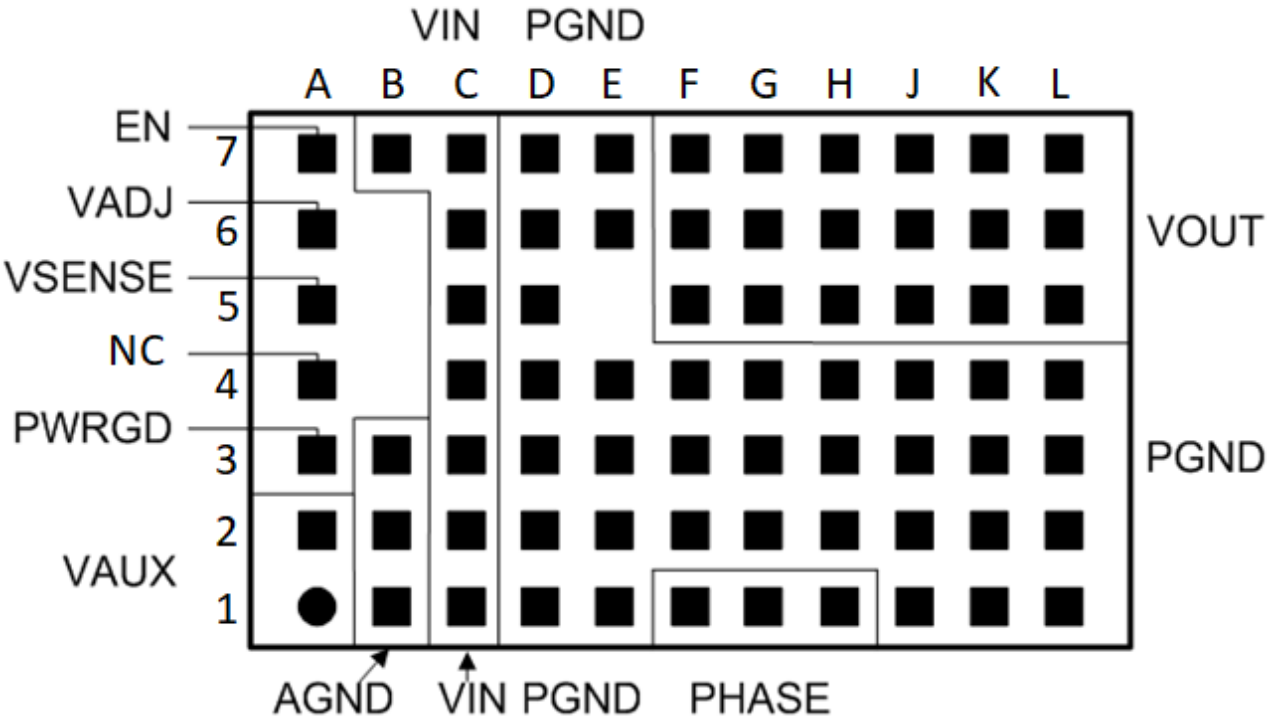
FUNCTIONAL BLOCK DIAGRAM for THPM4401A



PIN DESCRIPTIONS

PIN Name	Description
VIN (C1-C7, B7)	**Input voltage pins, referenced to PGND**. Connect input ceramic capacitors between these pins and PGND plane, close to the power module. It is suggested to place the ceramic capacitors at both sides of the module, one between PIN A3 and PIN A4-A5 and one between PIN G2-G3 and PIN G4-G5.
VAUX (A1, A2)	**Auxiliary output** from an LDO in the module, which is referenced to AGND. An external capacitor is not normally necessary. **Note:** VAUX pin is not capable of high current.
PHASE (F1-H1)	**Switching node of the Buck converter**. Please connect these pins together using a small and isolated copper plane under the device for better thermal performance. Do not connect any external component to these pins. Do not use these pins for other functions.
VOUT (F5-L5, F6-L6, F7-L7)	**Output voltage pins.** Connect these pins together onto a copper plane. Connect external output filter capacitors between these pins and PGND plane, close to the device.
PGND (D1-E1, J1-L1, D2-L2, D3-L3, D4-L4, D5, D6-E6, D7-E7)	**Zero DC voltage reference for power circuitry**. These pins should be connected directly to the PCB ground plane. All pins must be connected together externally with a copper plane or poured directly under the module.
AGND (B1- B3)	**Zero DC voltage reference for the analog control circuitry.** A small analog ground plane is recommended. VADJ, SS, and VSENSE pins should be referenced to analog ground. These pins should be connected directly to the PCB analog ground plane. A single point connection between AGND and PGND in motherboard is recommended.
EN (A7)	**Enable pin**. When above Enable On Voltage (V_{EN_ON}), the power module will be turned on when the power input voltage (VIN) is above start up voltage (V_{START}). When EN pin is below Enable Off Voltage (V_{EN_OFF}), the power module will be off.
VADJ (A6)	**Output voltage programming pin.** Connect a resistor between this pin and PGND top set the output voltage.
VSENSE (A5)	**Remote sensing pin.** Connect this pin to VOUT close to the load for improved voltage regulation. **Note**: this pin is not connected to VOUT inside the module, and must be connected externally.
NC (A4)	There is no connection to this pin. Leave open or connect to PGND
PWRGD (A3)	**Power Good pin**, an open drain output. A resistor connected between PWRGD and any voltage up to V_{IN} can be used. PWRGD is high if the output voltage is higher than 90% of the nominal value. It will be pulled down if the output voltage is less than 80% or higher than 120% of the nominal value.

LGA PACKAGE
73 PINS,
(TOP VIEW)



TYPICAL EFFICIENCY AND POWER LOSS DATA (Note 1)

A. Efficiency and power loss at 12V input

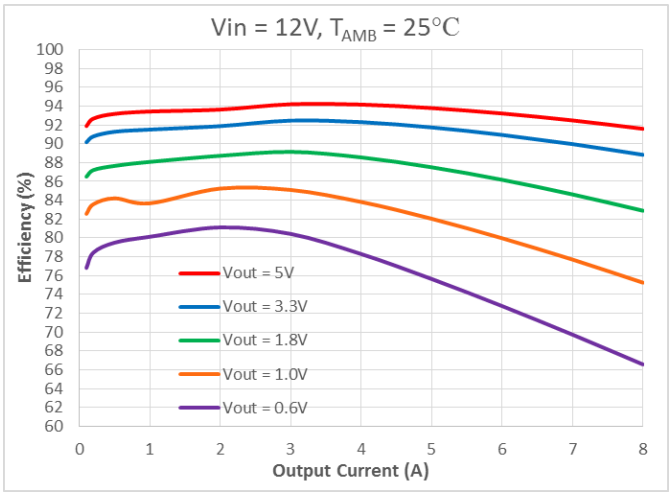


Fig. 1 Efficiency vs Output Current (V_{IN}=12V)

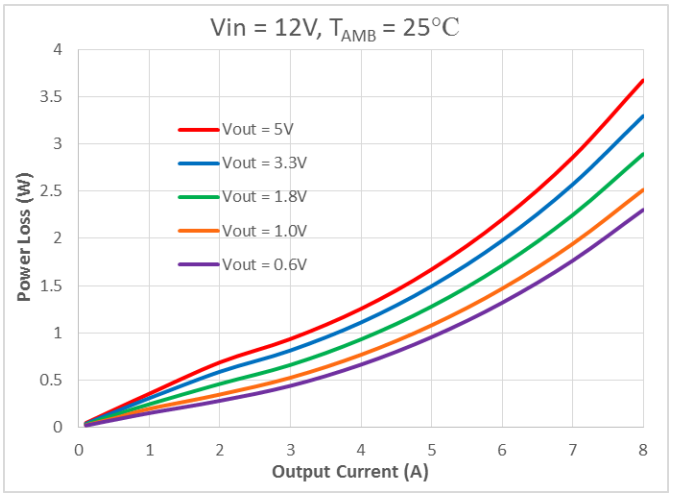


Fig. 2 Power Dissipation vs Output Current (V_{IN}=12V)

B. Efficiency and power loss at min, nominal and max input

V_{OUT} = 5V, T_A = 25°C

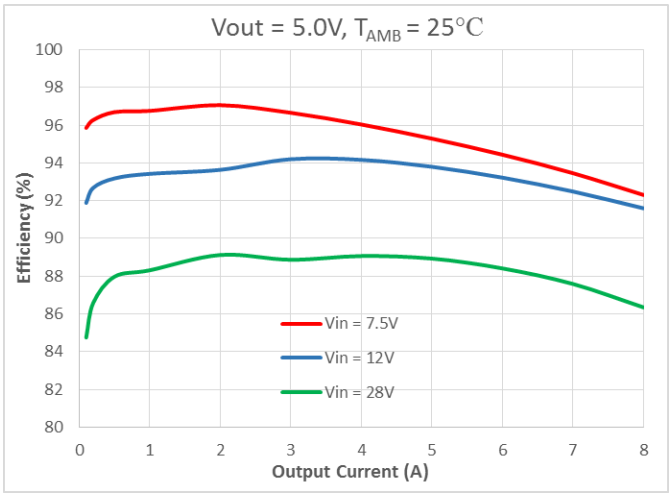


Fig. 3 Efficiency vs Output Current (V_{OUT}=5V)

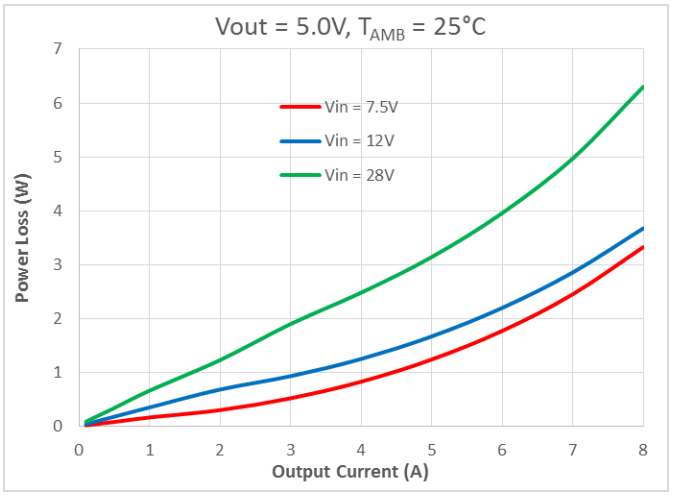


Fig. 4 Power Dissipation vs Output Current (V_{OUT}=5V)

V_{OUT} = 3.3V, T_A = 25°C

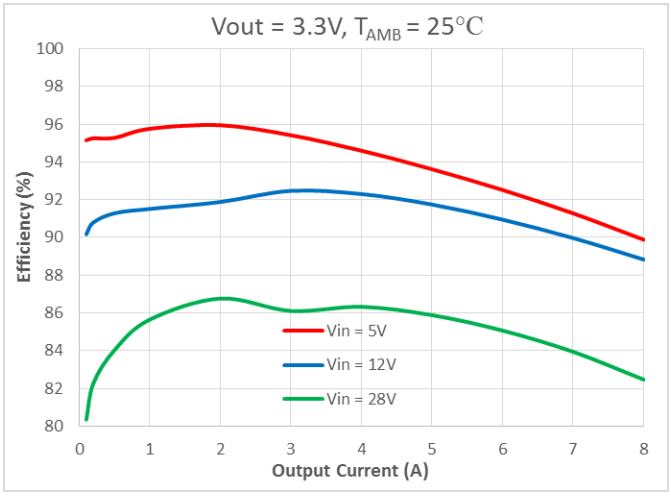


Fig. 5 Efficiency vs Output Current (V_{OUT}=3.3V)

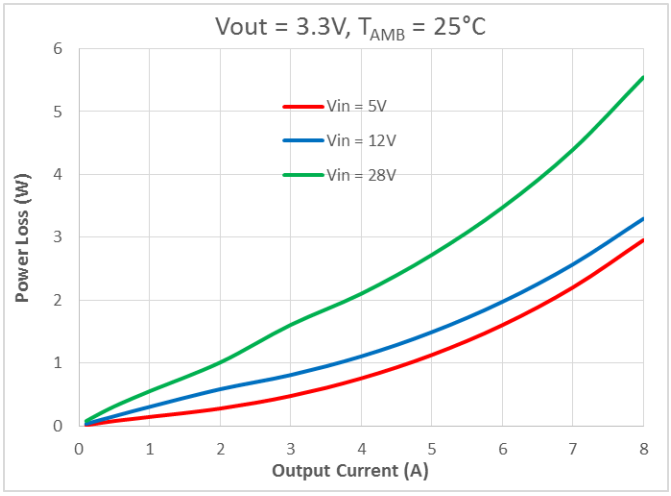


Fig. 6 Power Dissipation vs Output Current (V_{OUT}=3.3V)

V_{OUT} = 1.8V, T_A = 25°C

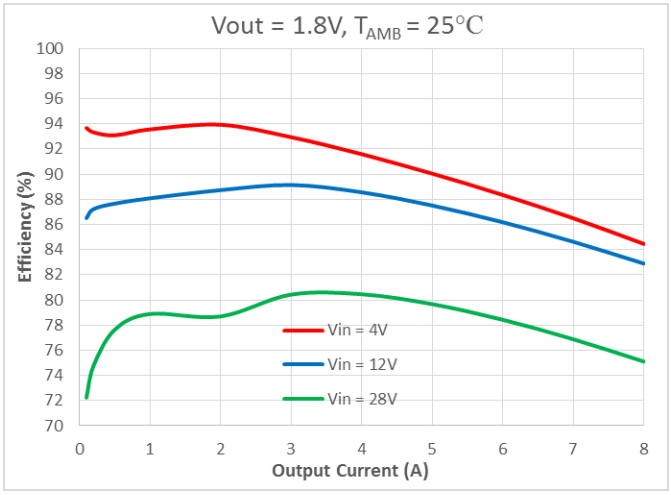


Fig. 7 Efficiency vs Output Current (V_{OUT}=1.8V)

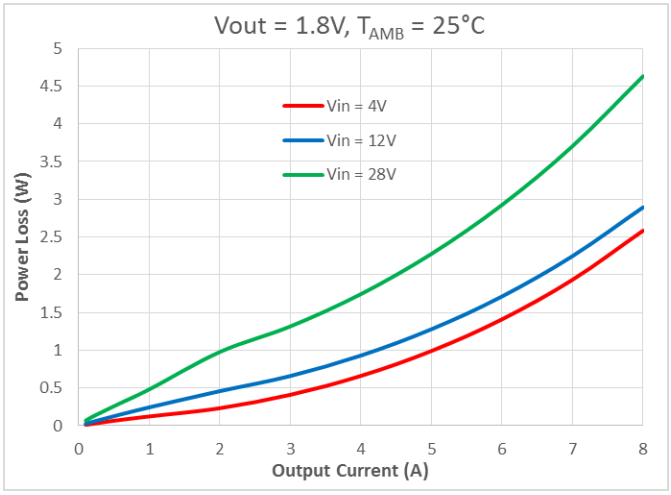


Fig. 8 Power Dissipation vs Output Current (V_{OUT}=1.8V)

V_{OUT} = 1.0V, T_A = 25°C

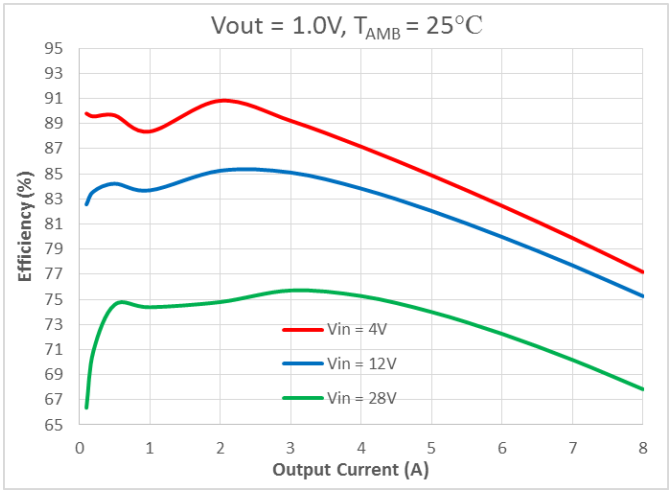


Fig. 9 Efficiency vs Output Current (V_{OUT}=1.0V)

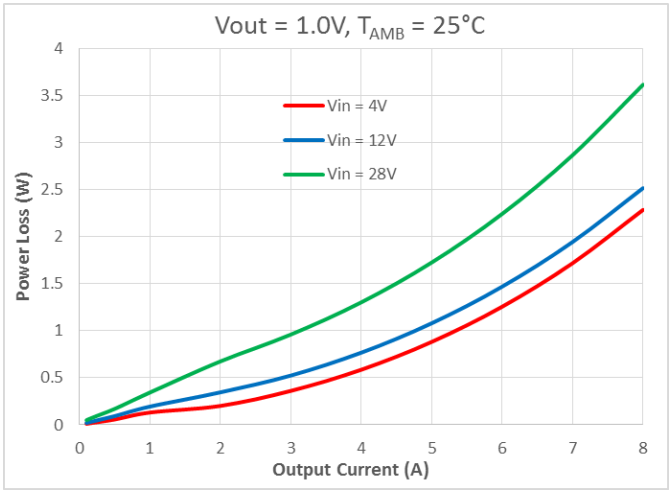


Fig. 10 Power Dissipation vs Output Current (V_{OUT}=1.0V)

V_{OUT} = 0.6V, T_A = 25°C

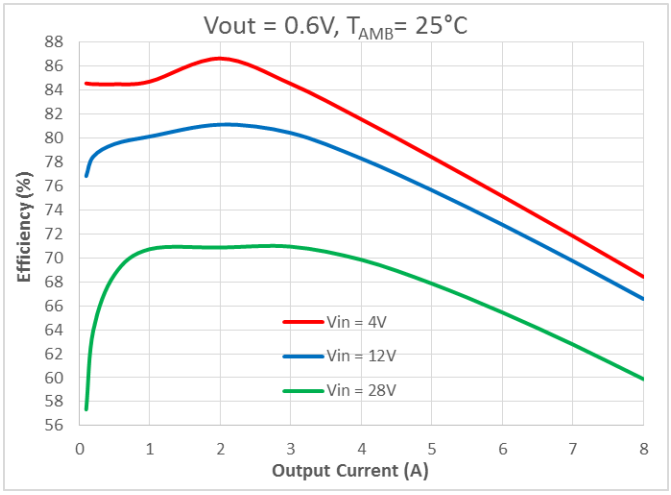


Fig. 11 Efficiency vs Output Current (V_{OUT}=0.6V)

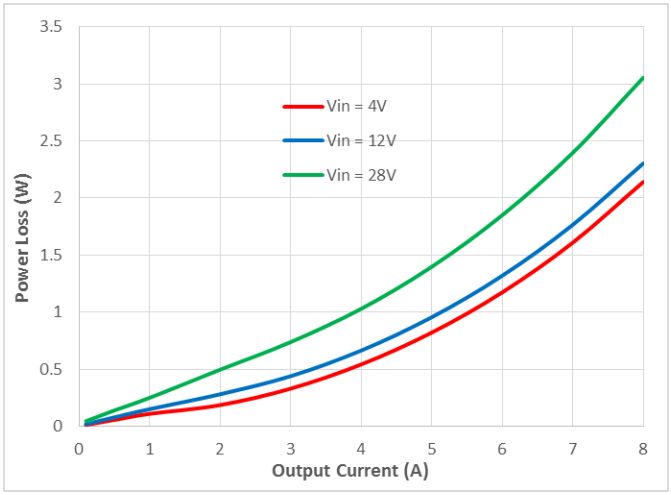


Fig. 12 Power Dissipation vs Output Current (V_{OUT}=0.6V)

Note 1: The above curves (Fig. 1 to Fig. 12) are derived from measured data taken on samples of the THPM4401A tested at room temperature (25°C), and are typical for the product.

APPLICATION INFORMATION

Output Voltage Programming

The output voltage is programmed using a resistor R_{PROG} from VADJ to PGND, as shown in Fig. 13. By default, the output voltage is 0.6V without a resistor connected.

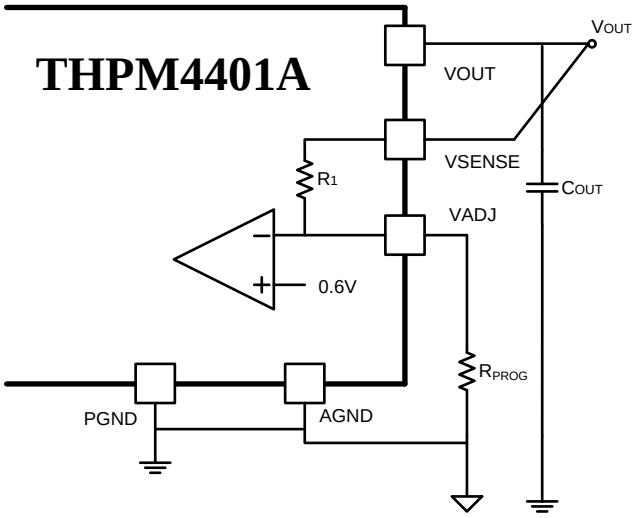


Fig. 13 Output Voltage Programming Circuit

A single standard resistor can be used to program for any of the common voltages shown in Table 1. For applications requiring a precise voltage set-point, it is recommended to use a 0.1% tolerance resistor.

Table 1 - Output Voltage Programming Resistor

0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
33.2kΩ	16.5kΩ	11kΩ	7.32kΩ	5.49kΩ	3.48kΩ	2.43kΩ	1.5kΩ

The programming resistor can be calculated for any output voltage using equation (1).

$$R_{PROG} = \frac{11k\Omega}{V_{OUT} / 0.6V - 1} \quad (1)$$

Note that the VADJ pin is noise sensitive and the connections to this pin should be kept as short as possible.

To further adjust the output voltage, another resistor R_{TRIM} may be connected between VSENSE and VADJ, as shown Fig. 14. The resulting output voltage is a function of equation (2).

$$V_{OUT} = 0.6V * (1 + \frac{(\frac{R_{TRIM} * 11k\Omega}{R_{TRIM} + 11k\Omega})}{R_{PROG}}) \quad (2)$$

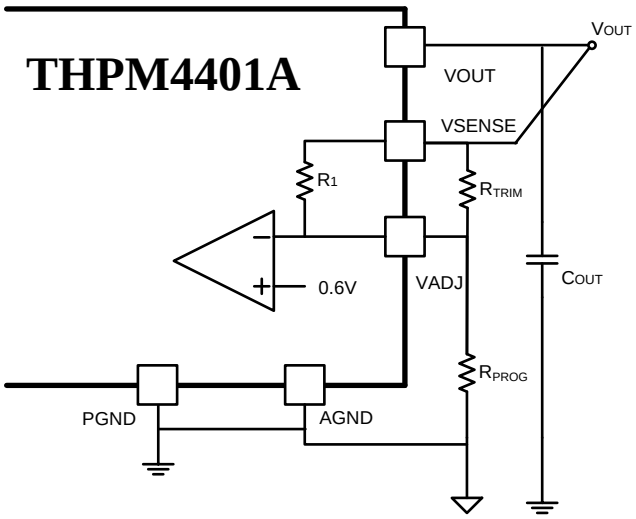


Fig. 14 Output Voltage Trim Circuit

To guarantee normal operation and regulation, there must be sufficient input-output voltage differential. Fig. 15 indicates the minimum input voltage required.

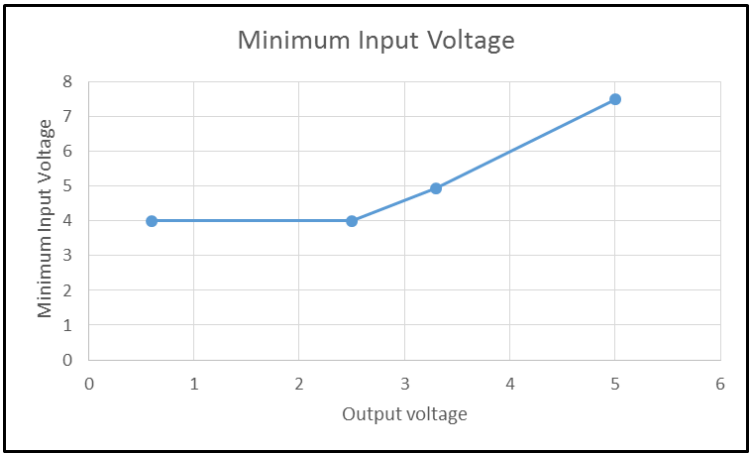


Fig. 15 Minimum Input Voltage

Enable (EN) Control

The EN pin provides an electrical on/off control of the power module. Once the voltage at the EN pin exceeds the threshold voltage (0.8V) or is left open, the power module starts operation when the input voltage is higher than the input start-up voltage (V_{START}).

When the voltage at EN pin is pulled below the threshold voltage, the switching converter stops switching and the power module enters low quiescent current state.

If an application requires controlling the EN pin, an open drain or open collector output logic can be used to interface with the pin, as shown in Fig. 16, where high ON/OFF signal (low EN) disables the power module.

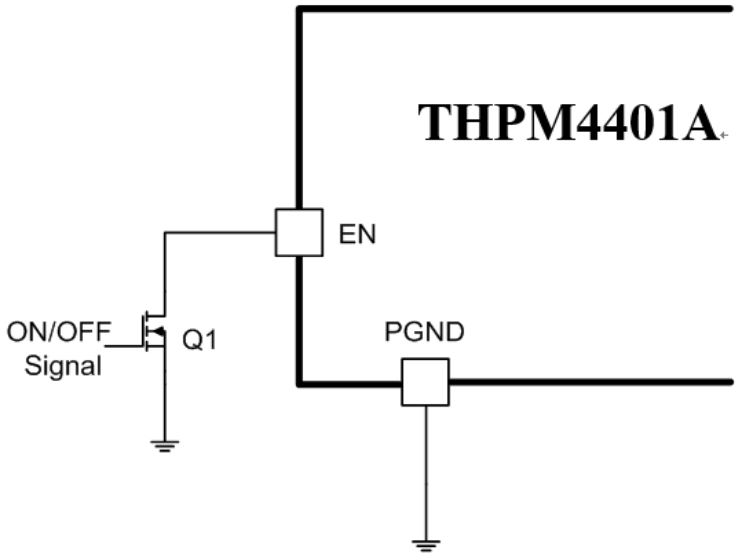


Fig. 16 Typical ON/OFF Control

When EN pin is open (or connected to a logic high voltage), THPM4401A produces a regulated output voltage following the application of a valid input voltage. Fig. 17 shows the startup waveform for THPM4401A without EN control. The top trace is input voltage, the middle trace is Power Good signal (PWRGD), and the bottom trace is the output voltage.

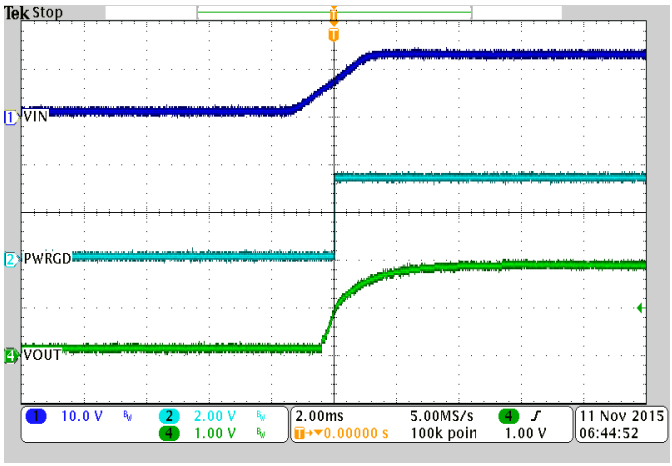


Fig. 17 Start-Up Waveforms for THPM4401A
(set to 1.8V output) without EN control

Fig. 18 and Fig. 19 show the typical output voltage waveforms when THPM4401A is turned on and turned off by the EN pin. In these figures, the top trace is enable signal (EN), the middle trace is Power Good signal (PWRGD), and the bottom trace is the output voltage.

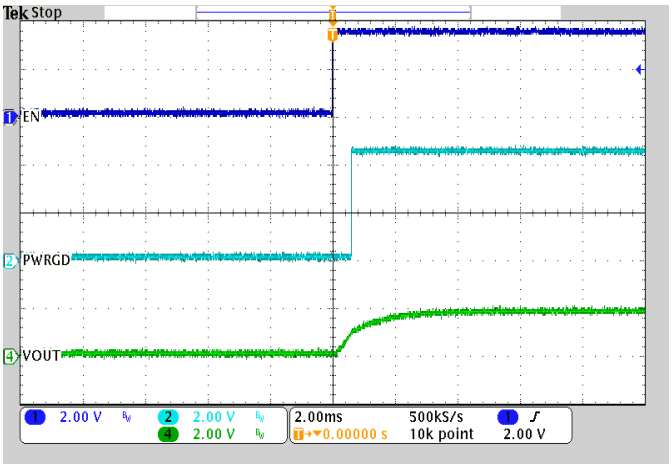


Fig. 18 Enable Turn-On for THPM4401A (set to 1.8V, with I_{OUT} = 6A)

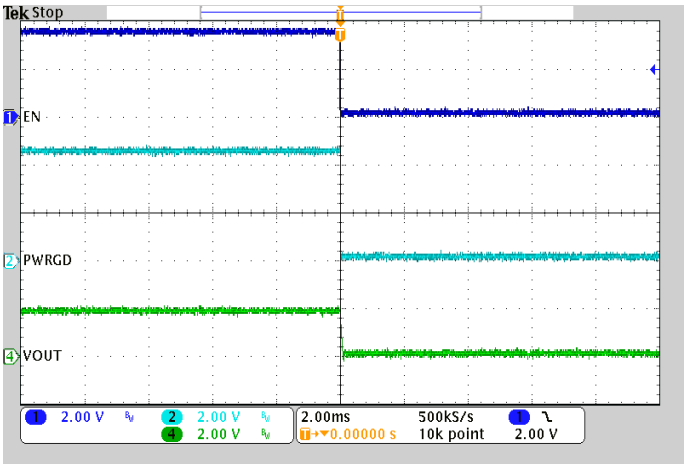


Fig. 19 Enable Turn-Off for THPM4401A (set to 1.8V, with I_{OUT} = 6A)

Pre-bias Startup

Some applications require startup when there is a residual pre-bias voltage on the output. The THPM4401A can start in this condition and as long as the pre-bias voltage is lower than the final output the start-up waveform will be normal. Fig. 20 illustrates start up with pre-bias of approximately 50% of the nominal output voltage. Fig. 21 shows the start-up when the pre-bias is about 80% of the nominal output.

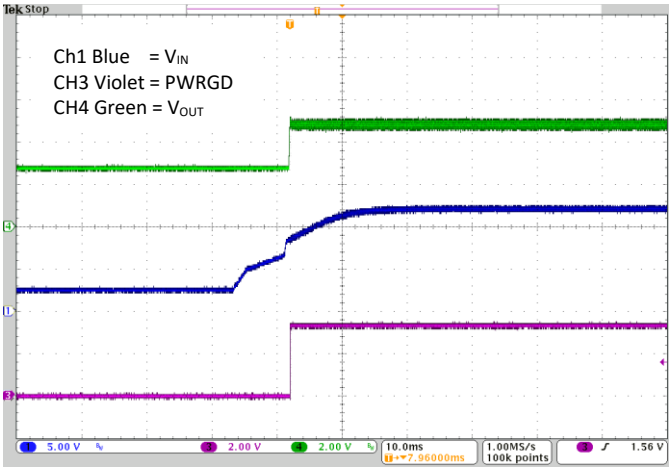


Fig. 20 Start-up with pre-bias 2.62V (V_{OUT}=5V)

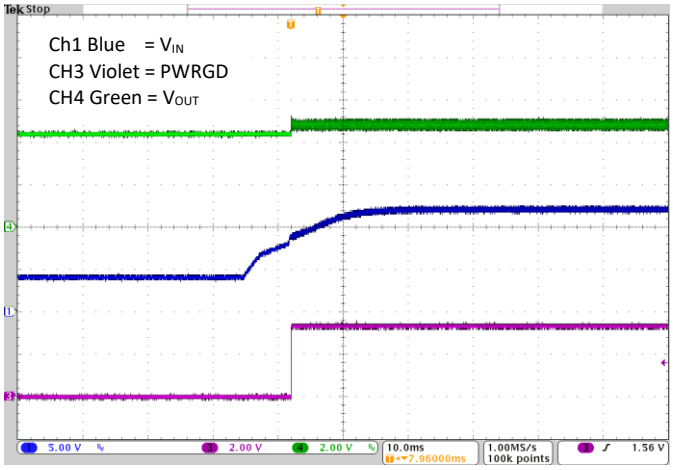


Fig. 21 Start-up with pre-bias 4.21V (V_{OUT}=5V)

Start Up Voltage

By default, the THPM4401A will turn on when the input voltage reaches the startup voltage (V_{START}). The THPM4401A will turn off when the input voltage reduces to below the Under-Voltage Lock-Out (UVLO) level. Startup voltage cannot be reduced below the values provided in the table of Electrical Characteristics. Startup voltage can be increased by an external resistor (R_{EN}) connected between EN pin and PGND pin.

The resistor value R_{EN} (in kΩ) can be calculated using equation (3) below based on the required start up voltage, V_{START}. Note: V_{START} must be higher than 3.9V.

$$R_{EN} = \frac{400}{(5V_{START} - 4)} \quad (3)$$

For example, to set the start-up voltage to 9.0V the value of R_{EN} will be 9.76 kΩ.

The shutdown voltage is given by equation (4) below:

$$V_{SHUTDOWN} = \frac{0.4 * (100k\Omega + R_{EN})}{R_{EN}} \quad (4)$$

For example, if R_{EN} = 9.76 kΩ the shutdown voltage will be 4.5V.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Connect a pull up resistor (10kΩ to 100kΩ) between PWRGD pin and VAUX pin, or to a suitable external voltage. [Note: maximum voltage on this pin is V_{IN}, but any lower voltage logic level can be used.] PWRGD signal becomes high when the output voltage reaches 90% of normal output voltage. The PWRGD signal becomes low when the output voltage is lower than 80% or higher than 120% of the normal output voltage.

Soft Start Operation

Soft-start operation is internal to the THPM4401A. It has an internally programmed fixed start-up time.

Input and Output Capacitance

Recommended minimum capacitance is 47µF ceramic (input) and 150µF ceramic (output). Additional capacitors can be connected in parallel if required, to reduce output ripple and improve transient response.

Application Schematics

Fig. 22 shows a typical application schematic for 12V input and 3.3V output. Startup voltage is set to 9V using the resistor R_{EN}, with value 9.76 kΩ. If required, a MOSFET can also be connected to the EN pin, as shown in Fig. 16 to provide on-off control.

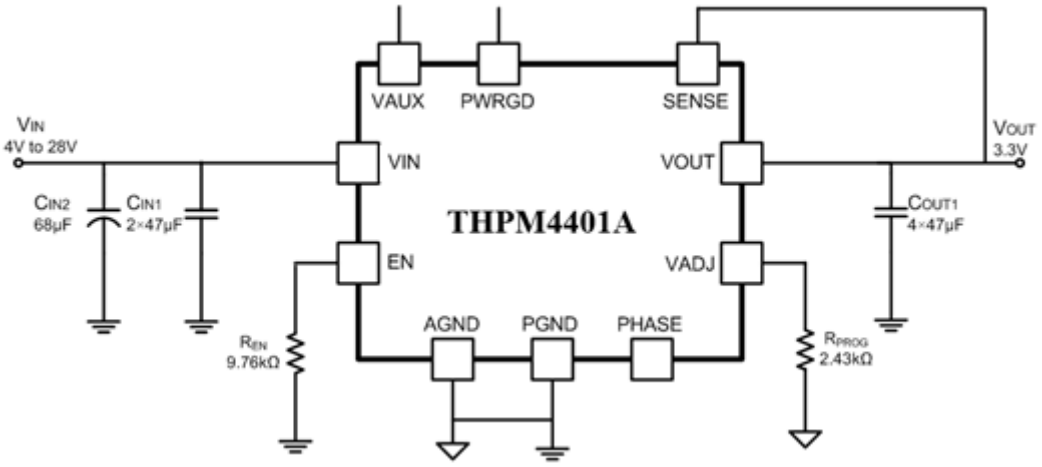


Fig. 22 Typical schematic for V_{IN} = 12V, V_{OUT} = 3.3V with start-up voltage set to 9V

Sequencing Operation

The term sequencing is used when two or more separate modules are configured to start one after the other, in sequence.

Sequencing operation between two or more THPM4401A power modules can be implemented with PWRGD pin and EN pin. Fig. 23 shows an example configuration when one THPM4401A (set to 5V) starts first and a second THPM4401A (set to 3.3V) starts after the output voltage of the first THPM4401A has reached 5V. In this case, the Power Good signal (PWRGD) of the first module turns on the second module through the EN pin.

Fig. 24 shows the output voltage waveforms of two THPM4401A modules used in sequential start-up mode. It shows that PWRGD signal becomes high when the first THPM4401A enters into regulation, and then the second THPM4401A starts up.

Note: The THPM4401A can start in sequence with another THPM4401A or with any other POL having a compatible Power Good output.

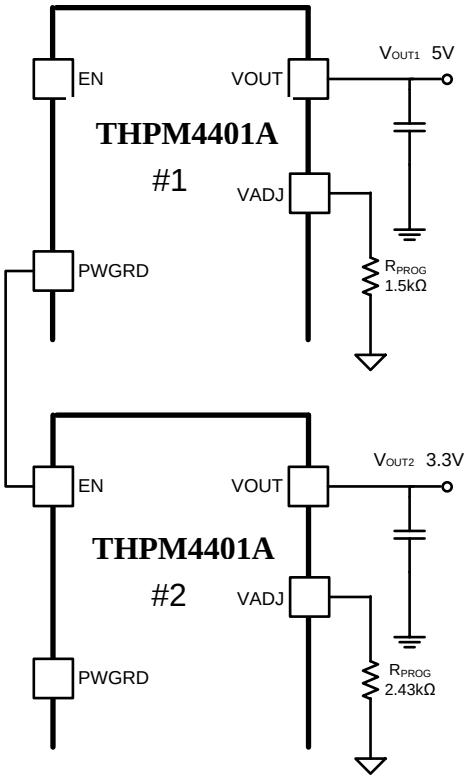


Fig. 23 Sequential Startup, V_{OUT1} = 5V, V_{OUT2} = 3.3V

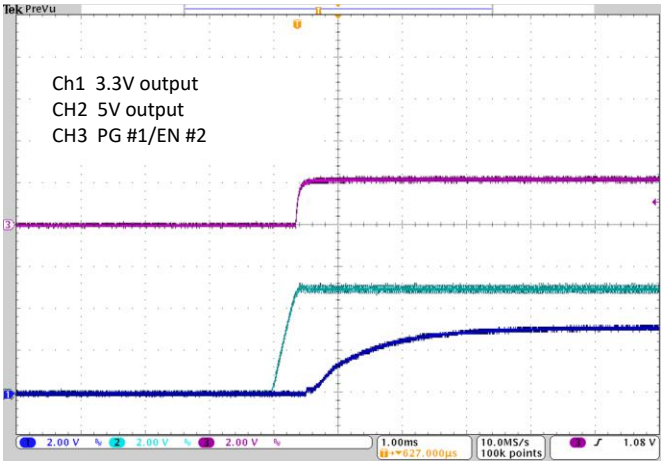


Fig. 24 Typical sequential startup waveforms

Transient Response

THPM4401A uses instant PWM control and achieves excellent transient performance. The following table summarizes the measured data when the load current undergoes a step change between 2A and 5A for output voltage setting of 5V and input voltage of 12V. The slew rate for the load current change is 1A/μs.

V_{OUT} setting	Transient voltage (3A step)	Recovery time
5V	40mV	150μs
0.6V	20mV	50μs

The measured transient waveform for 5V output is given in Fig. 25, and for 0.6V output in Fig. 26.

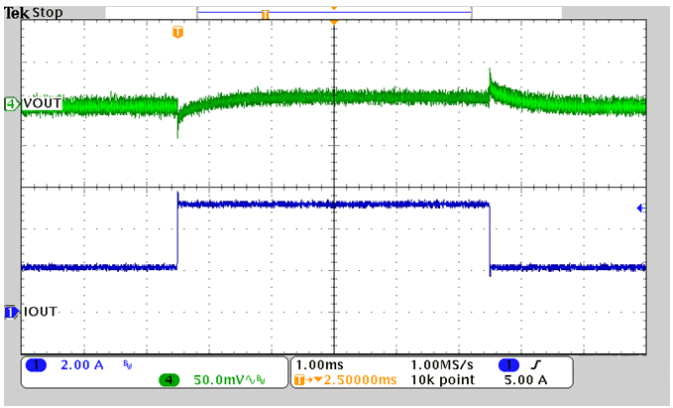


Fig. 25 Transient Response (V_{IN} = 12V, V_{OUT} = 5V)

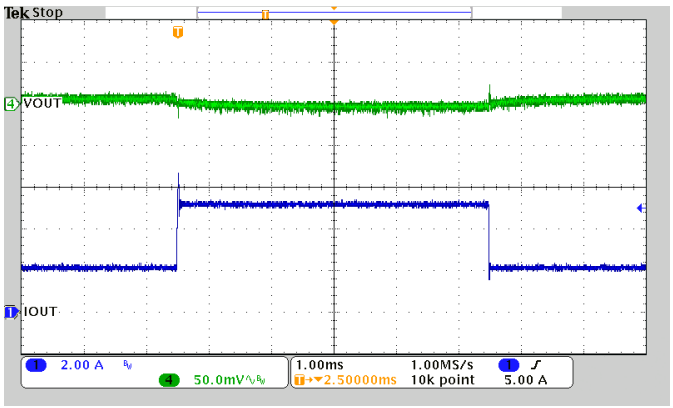


Fig. 26 Transient Response (V_{IN} = 12V, V_{OUT} = 0.6V)

The above figures show the typical output voltage waveform when the load current undergoes a step change between 2A and 5A (3A step), showing that the THPM4401A can achieve excellent dynamic performance.

Over Current Protection

For protection against over-current faults, THPM4401A will shut down when the load current is higher than the over-current protection (OCP) level. During an over-current condition, THPM4401A will operate in hiccup mode and will try to re-start automatically. The hiccup operation will continue until the over-current condition is removed or input power is removed.

Fig. 27 shows the output voltage and output current waveforms during over-current protection operation for THPM4401A set to 1.8V output. Performance at other output voltage settings is similar. When the over-current condition is removed, the output voltage recovers automatically to the nominal voltage, as shown in Fig. 28.

Note: Extended operation at the current limit point may cause the THPM4401A to latch off. If so, normal operation will resume after either the EN pin or the input power is momentarily cycled OFF and ON.

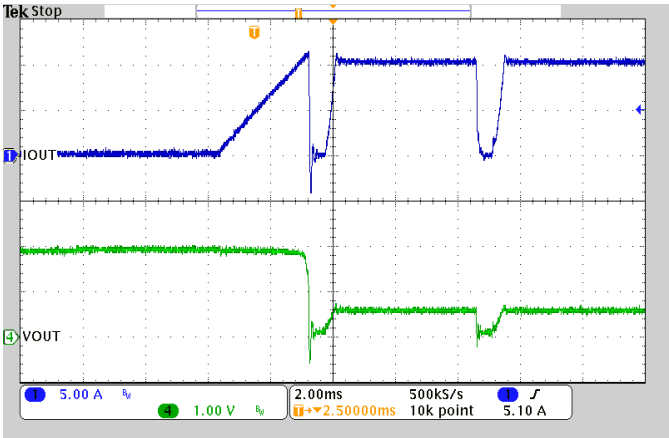


Fig. 27 Overcurrent protection (hiccup mode)

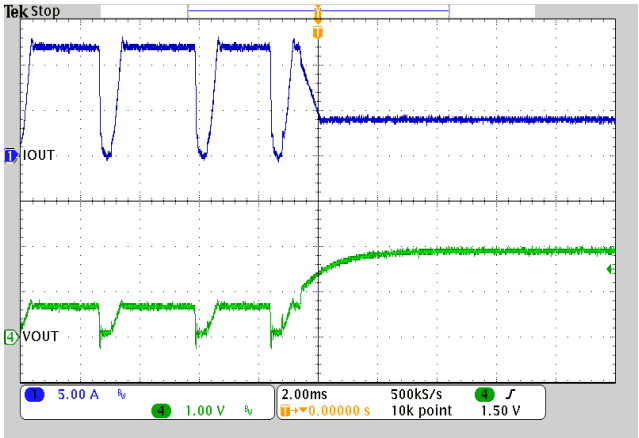


Fig. 28 Recovery from overcurrent

Input protection

In most applications, the input power source provides current limiting (typically fold-back or hiccup mode) and as long as the average fault current is limited to approximately 10A or less, no further protection is required.

If the THPM4401A is powered from a battery or other high current source, it is recommended to include an external fuse (maximum 10A) in the input to the module. The THPM4401A includes full protection against output overcurrent or short-circuit, and the fuse will not operate under any output overload condition.

Thermal Considerations

The maximum continuous current rating depends on the ambient temperature, input voltage and output voltage as shown in Fig. 29, Fig. 30 and Fig. 31. Output current can exceed these values for short periods, as long as the average does not exceed the derating curve.

The maximum rating is also influenced by the PCB layout; thermal performance can be improved by using more copper on the motherboard. The derating shown in these curves is measured using the THine Evaluation Module (EVM) layout. Derating also depends on airflow; these curves are based on data measured under natural convection (no forced air).

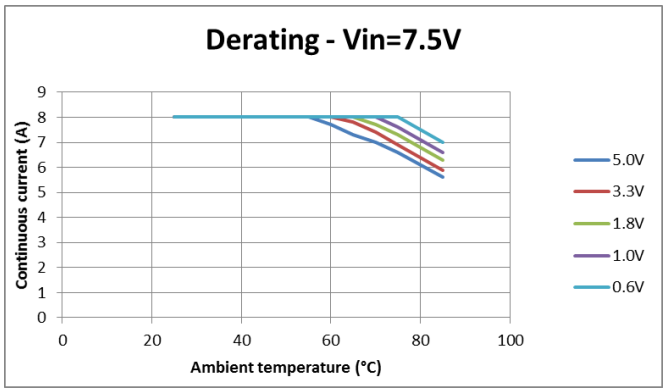


Fig. 29 Output current derating (7.5V input)

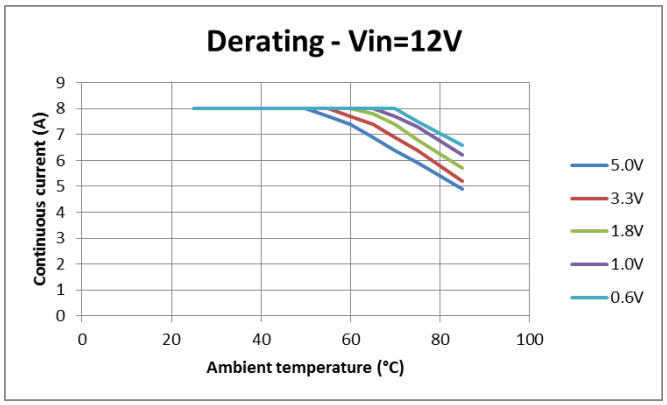


Fig. 30 Output current derating (12V input)

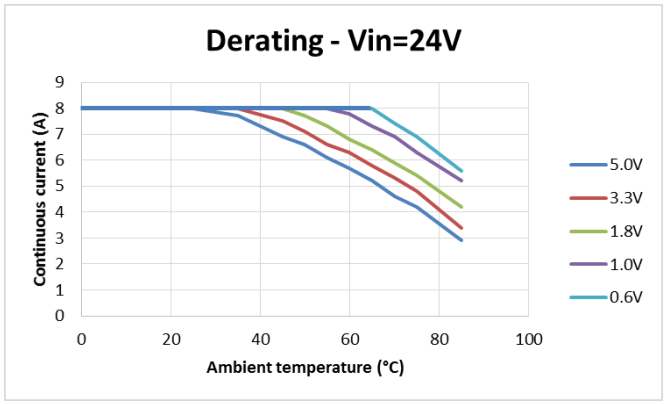


Fig. 31 Output current derating (24V input)

The absolute maximum operating junction temperature is 150°C and it is recommended to keep the operating temperature well below this value under worst-case conditions. Maximum recommended case temperature is 115°C, which corresponds to a junction temperature of approximately 125°C.

The thermal resistance from case to ambient (θ_{CA}) depends on the PCB layout as well as the amount of cooling airflow. When mounted on the EVM, θ_{CA} is approximately 15°C/watt in still air.

The THPM4401A implements an internal thermal shutdown to protect itself against over-temperature conditions. When the junction temperature of the power MOSFET is above 150°C, the power module stops operating to protect itself from thermal damage. When the MOSFET temperature reduces to approximately 135°C (with hysteresis of 15°C), THPM4401A will restart automatically.

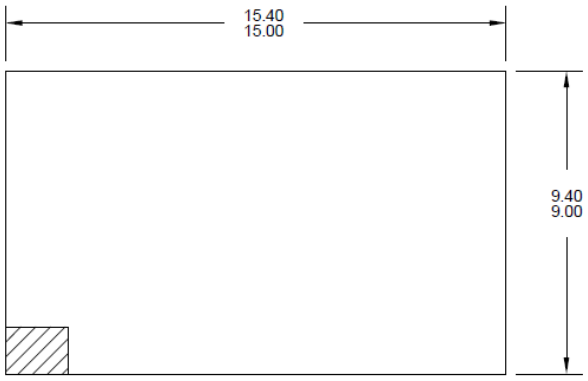
Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Some considerations for an optimized layout are:

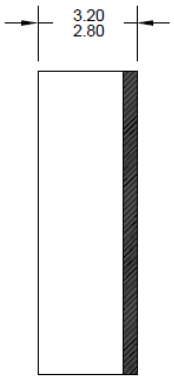
- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress;
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise;
- Locate additional output capacitors between the main ceramic capacitor and the load;
- Connect AGND plane and PGND plane at single point;
- Place resistors and capacitors connected to SENSE and VADJ pins as close as possible to their respective pins;
- Do not connect PHASE pin to other components;
- Use multiple vias to connect the power planes to internal layers.

Package Dimensions and PCB pads

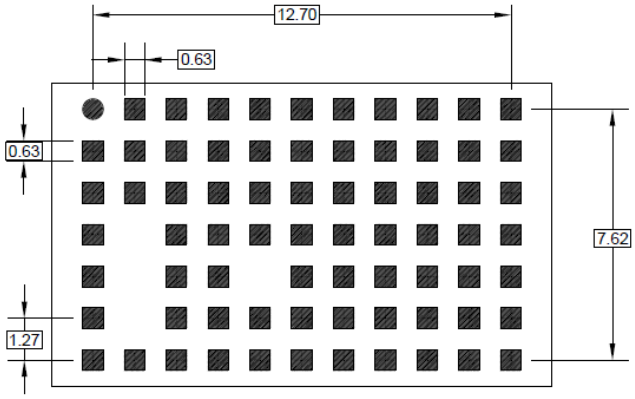
ALL DIMENSIONS IN MILLIMETERS
FLATNESS OF LGA PLANE: MAX 0.1mm



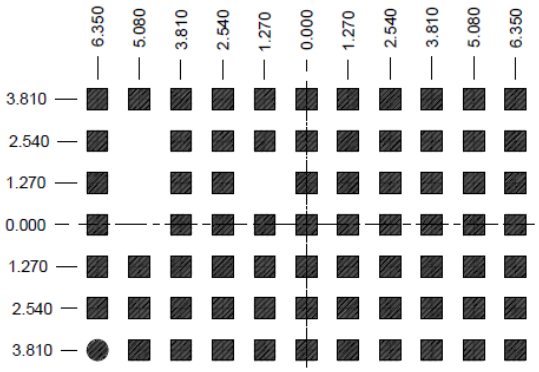
Package Top View



Package Side View



Package Bottom View



Suggested PCB Layout
Top View

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