THPM4301A

3.3V/5V Input 6A Output POL Power Module

Features

- Integrated Point of Load power module using in Inductor technology
- Small footprint, low-profile, 11mm x 9.1mm x 2.8mm, with LGA Package (0.63 mm Pads)
- Efficiency up to 96%
- High output current, 6A without derating at 85°C ambient with no air flow
- Wide output voltage adjustment: 0.6V to 3.6V
- Pre-bias startup capability
- User adjustable switching frequency
- Synchronization to external clock signal
- Adjustable soft-start time for output voltage
- Output voltage sequencing / tracking
- Enable signal input and Power Good signal output
- Programmable Under Voltage Lock Out (UVLO)
- Output Over Current Protection (OCP)
- Over temperature protection
- Operating temperature range -40°C to 85°C

Applications

- Broadband and communications equipment
- DSP and FPGA Point of Load applications
- High density distributed power systems
- PCI express / PXI express
- Automated test and medical equipment

Description

THPM4301A is an easy-to-use 6A output integrated Point of Load (POL) power supply module. It contains integrated power MOSFETs, driver, PWM controller, a high-performance inductor, input and output capacitors and other passive components in one low profile LGA package using Inductor technology.

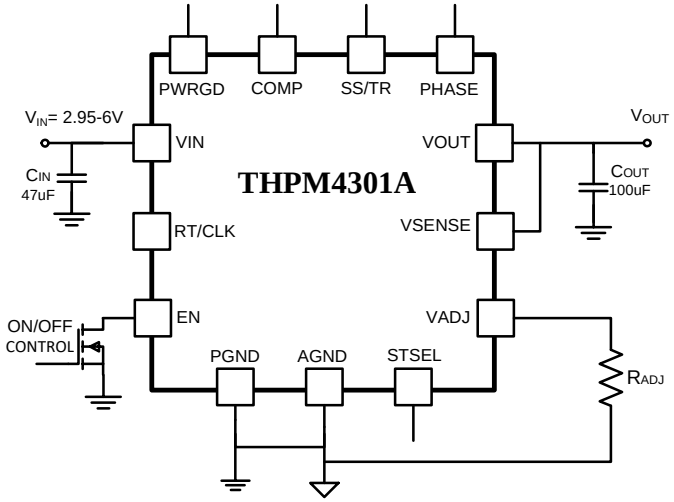
There is no need for loop compensation, sensitive PCB layout, inductor selection or in-circuit production testing. Each module is fully tested.

The THPM4301A can be programmed for any output voltage between 0.6V and 3.6V using a single external resistor. For an output voltage of 0.6V no resistor is required.

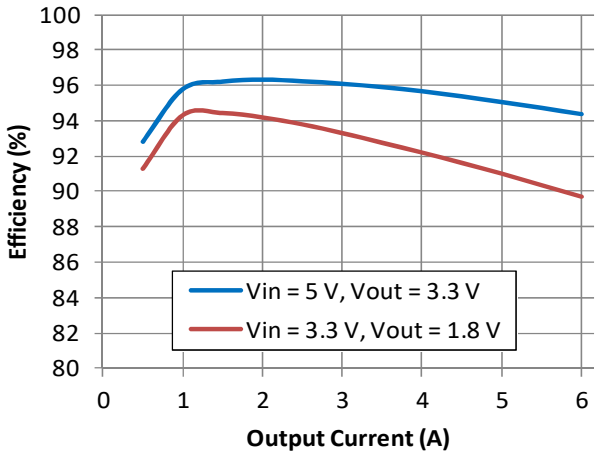
THPM4301A can deliver full 6A load current without derating at 85°C ambient temperature with no airflow.

Small size (11mm x 9.1mm) and low profile (2.8mm) allows the THPM4301A to be placed very close to its load or on the back side of the PCB for high density applications.

SIMPLIFIED APPLICATION



EFFICIENCY VS LOAD CURRENT



ABSOLUTE MAXIMUM (1) RATINGS over operating temperature range (unless otherwise noted)

		VALUE		Unit
		MIN	MAX	
Input Voltage	VIN	-0.3	7	V
	EN	-0.3	7	V
	VSENSE	-0.3	VOUT	V
	COMP	-0.3	3	V
	PWRGD	-0.3	6	V
	SS / TR	-0.3	3	V
	STSEL	-0.3	3	V
	RT / CLK	-0.3	6	V
Output Voltage	VOUT	-0.6	VIN	V
Source Current	EN		100	μA
	RT / CLK		100	μA
Sink Current	COMP		100	μA
	PWRGD		10	mA
	SS / TR		100	μA
Temperature	Operating Junction Temperature		150	°C
	Storage Temperature	-55	150	°C
	Peak solder reflow body temperature		245	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect reliability.

ORDERING INFORMATION

Output Voltage	Module Part Number	Pad Finish	Package Type	Temperature Range
Adjustable	THPM4301A	Au (RoHS)	LGA	-40˚C to 85˚C

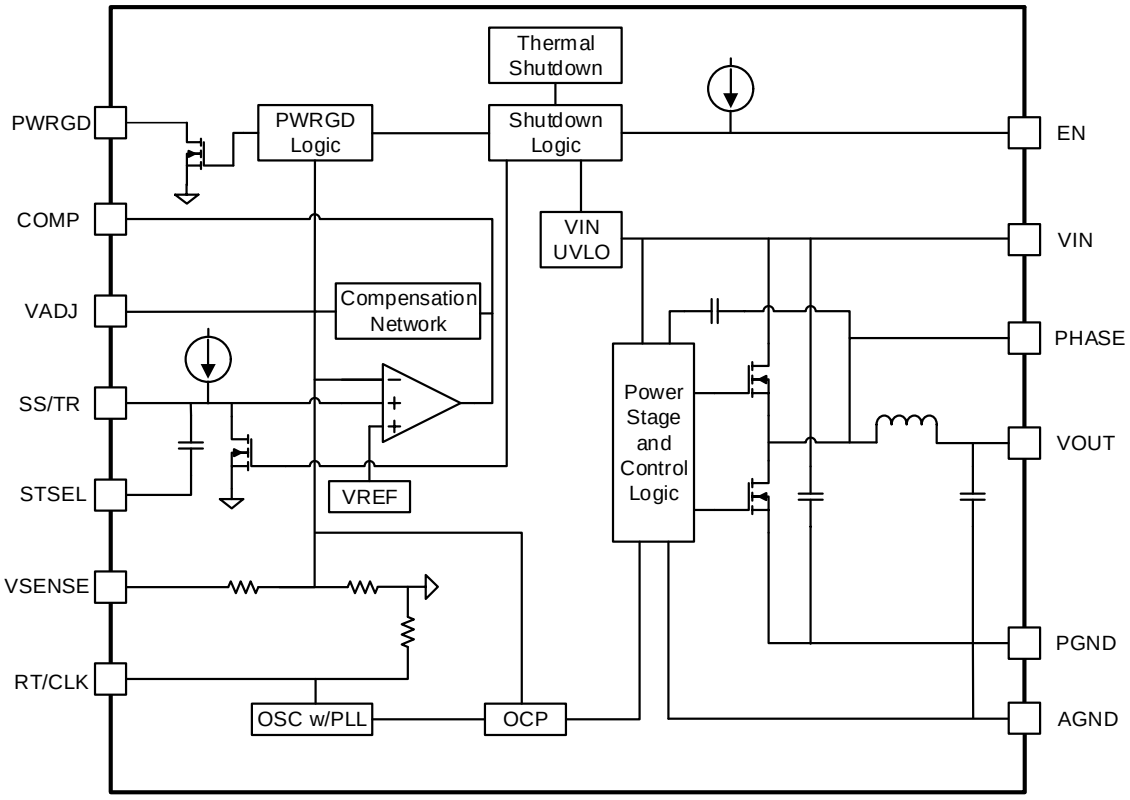
ELECTRICAL CHARACTERISTICS:

The electrical performance is based on the following conditions unless otherwise stated: 25°C ambient temperature, no air flow; V_{IN} = 5V, (1) V_{OUT} = 1.8V, I_{OUT} = 6A, C_{IN1} = 47µF ceramic, C_{OUT} = 2×47µF ceramic.

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}: Output current		T_A = -40°C to 85°C, natural convection		0		6	A
V_{IN}: Input voltage		Over I_{OUT} range, -40°C to 85°C		2.95		6	V
V_{START} Startup voltage		Over I_{OUT} range, -40°C to 85°C [**Note 1**]			2.8		V
UVLO Under Voltage Lock Out		Over I_{OUT} range, -40°C to 85°C [**Note 1**]			2.5		V
Hysteresis between V_{START} and UVLO		Over I_{OUT} range [**Note 1**]			0.3		V
V_{OUT}	Set point accuracy	T_A = 25°C, I_{OUT} = 3A [**Note 2**]			±1%		
	Temperature variation	-40°C < T_A < +85°C, I_{OUT} = 3A			±0.3%		
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 3A			±0.2%		
	Load regulation	Over I_{OUT} range, T_A = 25°C, V_{IN} = 5V			±0.2%		
$V_{OUT(adj)}$: Output voltage adjust range		Over I_{OUT} range, T_A = -40°C to 85°C		0.6		3.6	V
η Efficiency		V_{IN} = 5V	V_{OUT} = 3.3V, I_{OUT} = 3A		96.1%		
			V_{OUT} = 3.3V, I_{OUT} = 6A		94.2%		
		V_{IN} = 3.3V	V_{OUT} = 2.5V, I_{OUT} = 3A		95.4%		
			V_{OUT} = 2.5V, I_{OUT} = 6A		92.3%		
F_S Switching frequency [**Note 3**]		R_T = 127KΩ between RT/CLK and AGND			750		kHz
Output voltage ripple		20MHz bandwidth			20		mVpp
I_{LIM} Current Limit Point					9.0		A
V_{EN-H} Enable control		Enable high voltage			1.3		V
V_{EN-L} Enable control		Enable low voltage			1.18		V
PWR Good:		V_{OUT} rising threshold	Good		93%		
			Fault		105%		
		V_{OUT} falling threshold	Good		103%		
			Fault		91%		
Thermal shutdown		Thermal shutdown			170		°C
		Thermal shutdown recovery hysteresis			15		°C

Note 1: With R_{EN1} = 14.7k Ω and R_{EN2} = 12.7k Ω as shown in Fig. 28.
Note 2: With 0.1% tolerance external voltage set resistor.
Note 3: 750kHz is suitable for 3.3V output, but lower switching frequencies are recommended for lower output voltages. See Table 3 for recommended switching frequency, and refer to page 19 for information on adjusting the frequency.

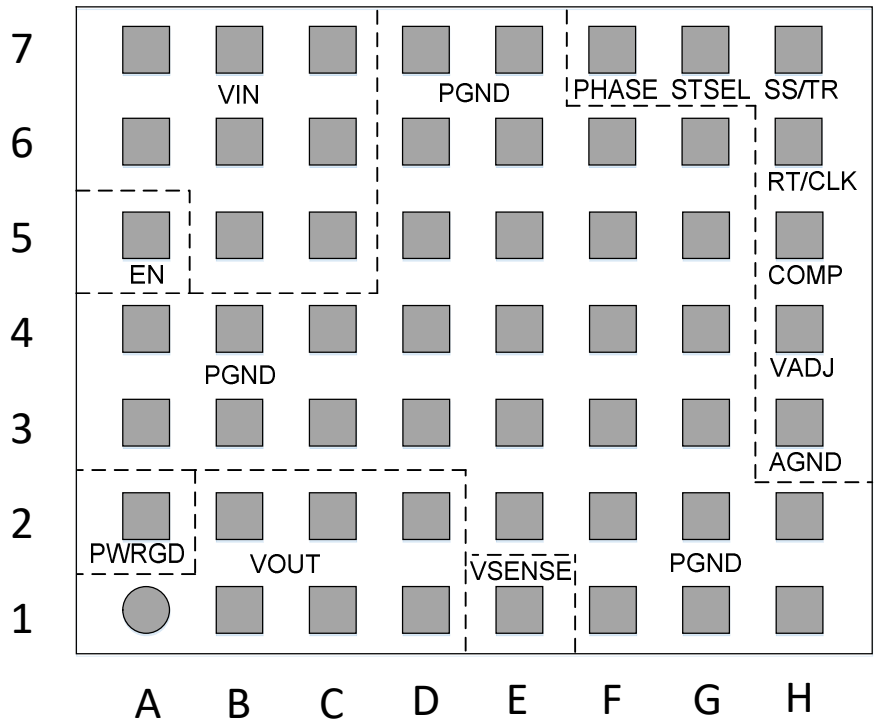
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN Name	Description
VIN (B5-C5, A6-C6, A7-C7)	**The positive input voltage power pin**, which is referenced to PGND. Connect external input filter capacitors between these pins and PGND plane, close to module.
PHASE (F7)	**Switching node pin**. Connect this pin to a small copper island under the module for best thermal performance. Do not connect any external component to this pin or use this pin for any other functions.
VOUT (A1-D1, B2-D2)	**Output voltage.** Connect external output filter capacitors between these pins and PGND plane, close to the module.
PGND (F1-H1, E2-H2, A3-G3, A4-G4, D5-G5, D6-G6, D7-E7)	**Zero DC voltage reference for power circuitry**. These pins should be connected directly to the PCB ground plane. The module's heat transfer is through these pins and all of them must be connected together externally with a copper plane located directly under the module.
AGND (H3)	**Zero DC voltage reference for the analog control circuitry**. A small analog ground plane is recommended. RT/CLK, STSEL, SS/TR pins should be referenced to analog ground. AGND and PGND should be connected at a single point is such a way that load current does not flow in the AGND plane.
STSEL (G7)	**Startup mode selection**. Short to AGND for soft-start operation with extended soft-start time determined by a capacitor connected between SS/TR pin and AGND. Leave this pin open for tracking operation or selecting default soft-start time that is nominally 1.1ms. See SS/TR pin description below for more details.
SS/TR (H7)	**Soft-start or tracking operation**. When SS/TR pin is open and STSEL pin is shorted to AGND, the power module operates in soft-start mode with the default soft-start time of 1.1ms. Longer soft-start time can be achieved with an additional capacitor connected between SS/TR pin and AGND. Capacitor value can be selected based on Equation 4 or values provided in Table 2. For tracking operation, leave STSEL open and do not connect additional capacitor between SS/TR and AGND. Connect this pin to the voltage to be tracked. Refer to Fig. 30 for more details.
RT/CLK (H6)	**Switching frequency and external synchronization pin**. An internal 90.9KΩ resistor is connected between RT/CLK and AGND to set the switching frequency to 450KHz. An external synchronization clock can be connected to RT/CLK pin to synchronize the switching frequency of the module. More details are provided on page 19.
EN (A5)	**Enable pin** with internal pull-up current source. Pull this pin to below 1.18V to disable the power module. Float this pin or pull to above 1.3V to enable the power module. This pin can be used to adjust the under voltage lockout (UVLO) level with two additional resistors forming a voltage divider from V_{IN} to AGND as shown in Fig. 28.
COMP (H5)	**Compensation pin**. The COMP pin should be open.
VADJ (H4)	**Output voltage adjustment pin**. Connect a resistor, R_{ADJ}, between VADJ pin and AGND pin to set the desired output voltage, as shown in Fig. 15.
PWRGD (A2)	**Power Good pin**. An open drain output that is pulled low when VSENSE voltage is less than 91% or greater than 105% of the nominal output voltage. PWRGD is floating when the voltage at VSENSE pin is between 93% and 103% of the nominal output voltage.
VSENSE (E1)	**Remote sensing pin for the output voltage**. Connect this signal to VOUT close to the load for improved regulation. Do not use an LC filter between VOUT pins of the module and the point where VSENSE is connected. **Note**: this pin is not connected to VOUT inside the module and must be connected externally.

LGA PACKAGE
56 PINS
(TOP VIEW)



TYPICAL CHARACTERISTICS (Note 1)

V_{OUT} = 3.3V

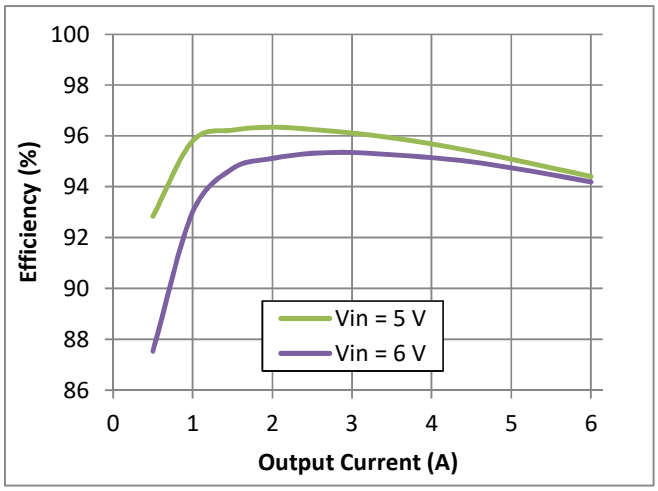


Fig. 1 Efficiency vs Output Current

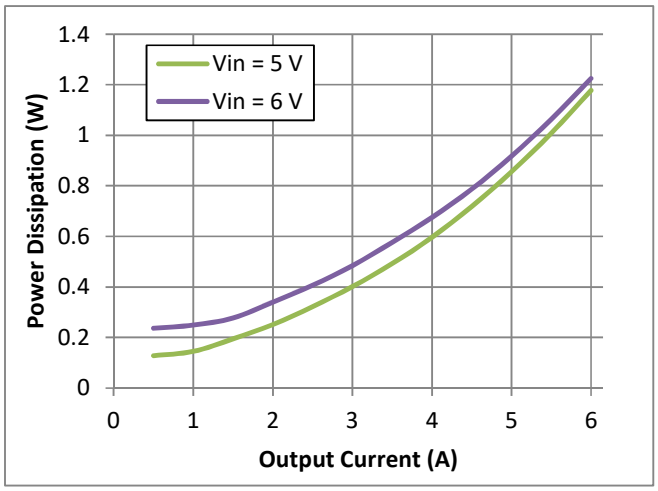


Fig. 2 Power Dissipation vs Output Current

V_{OUT} = 2.5V

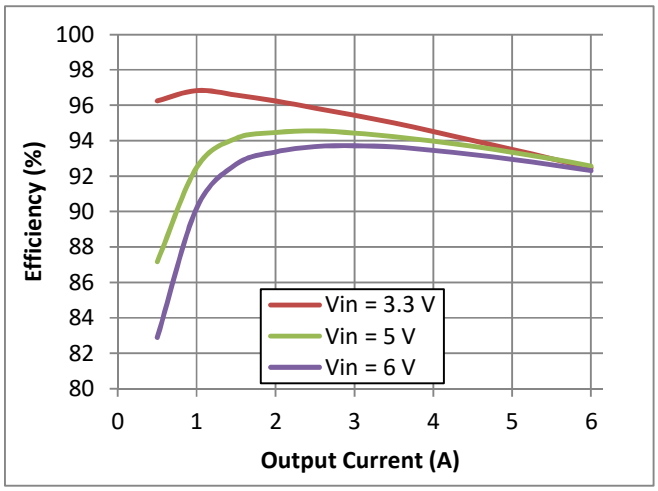


Fig. 3 Efficiency vs Output Current

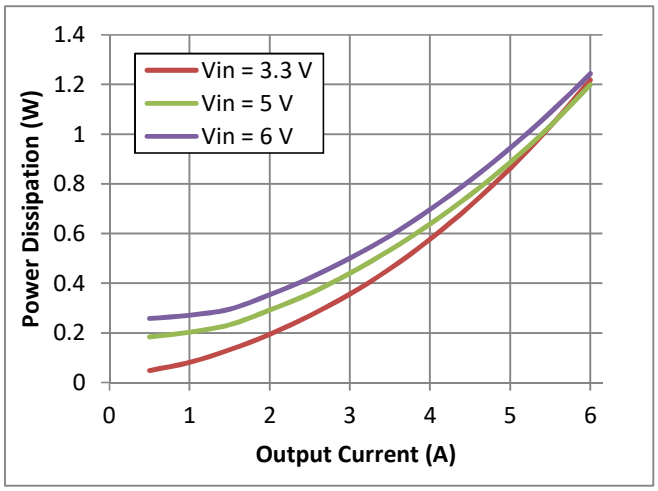


Fig. 4 Power Dissipation vs Output Current

V_{OUT} = 1.8V

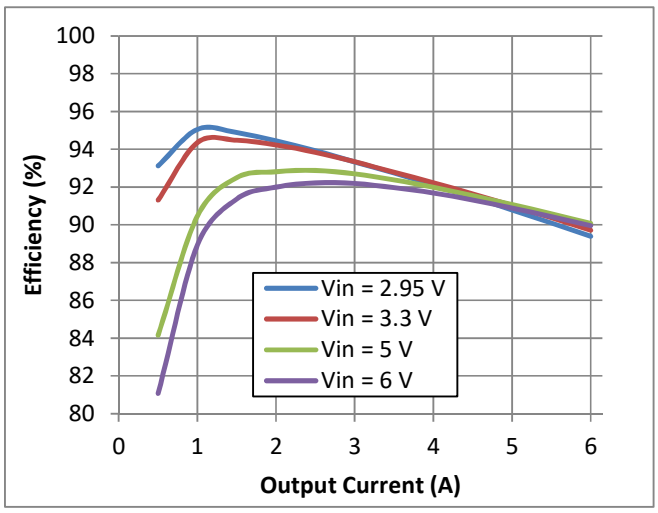


Fig. 5 Efficiency vs Output Current

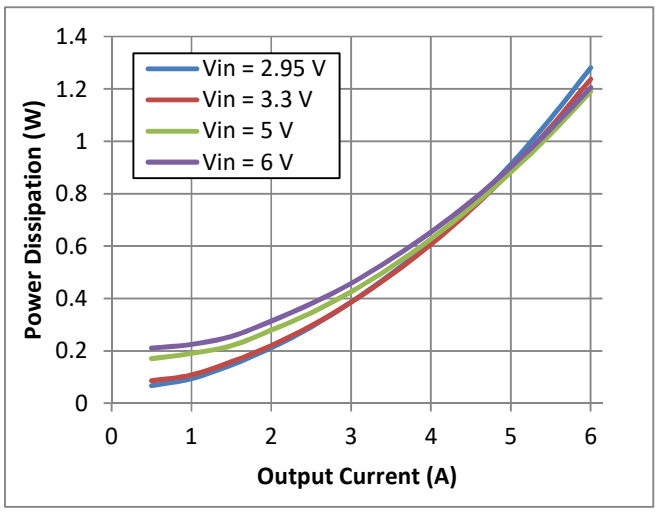


Fig. 6 Power Dissipation vs Output Current

V_{OUT} = 1.5V

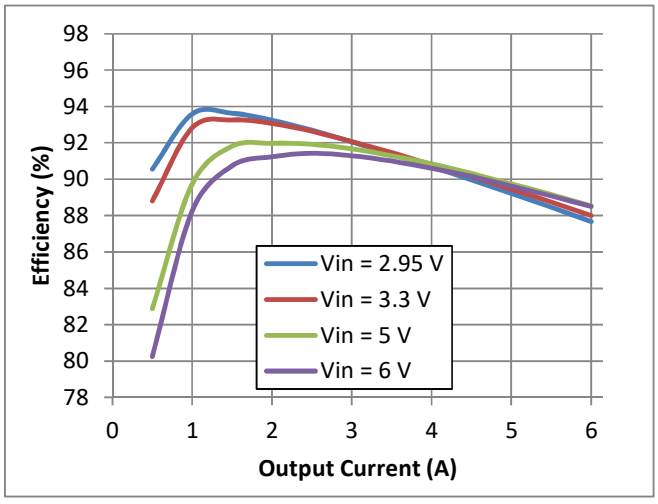


Fig. 7 Efficiency vs Output Current

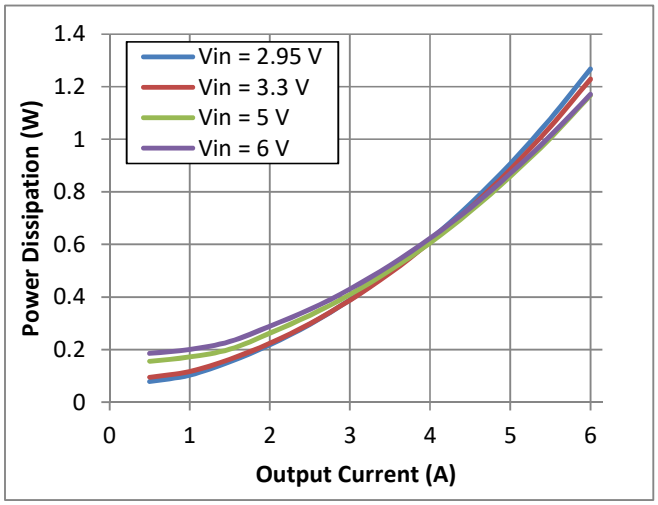


Fig. 8 Power Dissipation vs Output Current

V_{OUT} = 1.0V

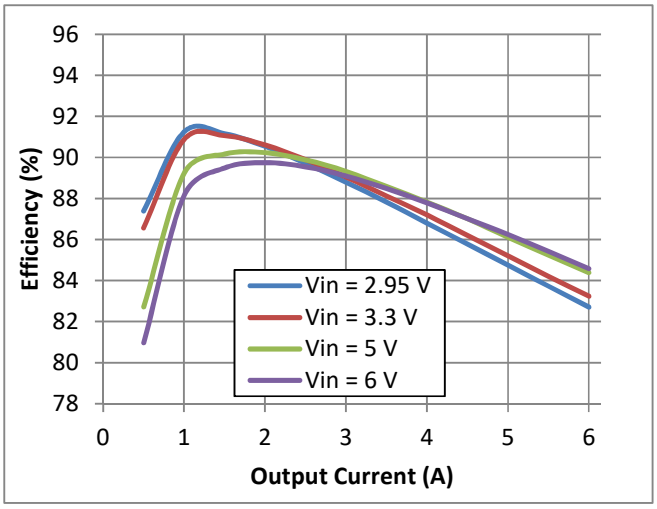


Fig. 9 Efficiency vs Output Current

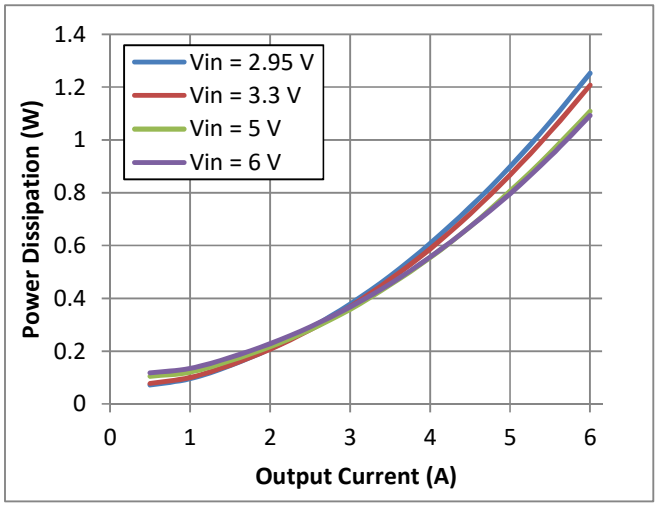


Fig. 10 Power Dissipation vs Output Current

V_{OUT} = 0.8V

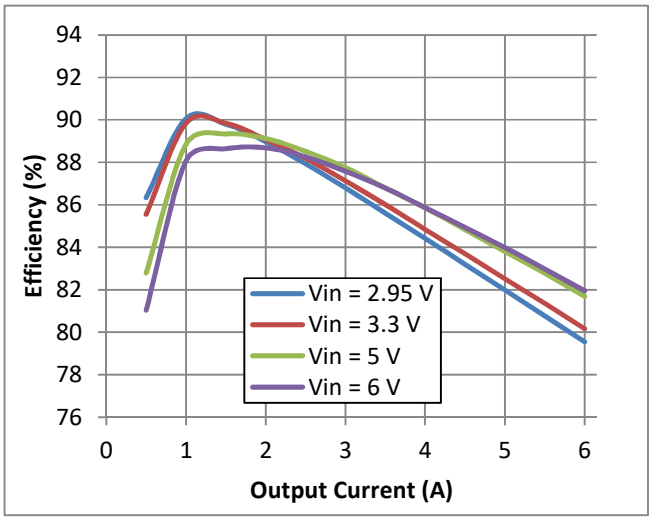


Fig. 11 Efficiency vs Output Current

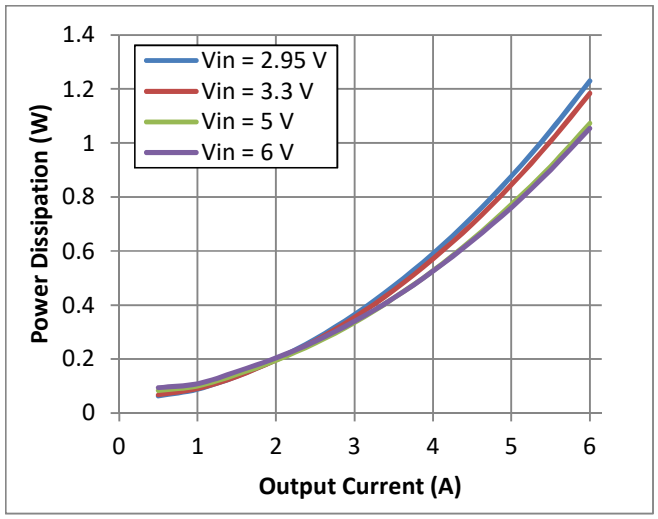


Fig. 12 Power Dissipation vs Output Current

V_{OUT} = 0.6V

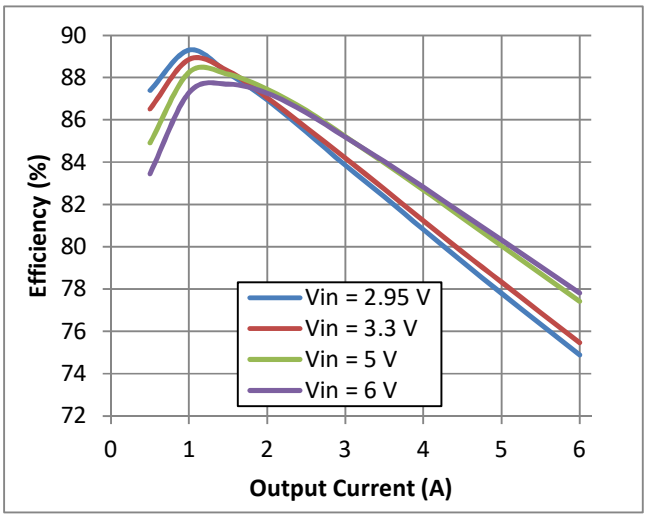


Fig. 13 Efficiency vs Output Current

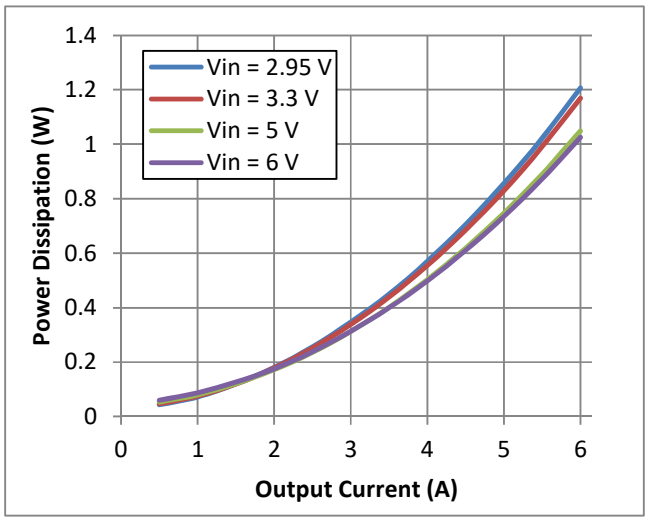


Fig. 14 Power Dissipation vs Output Current

Note 1: The above curves (Fig. 1 to Fig. 14) are derived from measured data taken on samples of the THPM4301A tested at room temperature (25°C), and are considered to be typical for the product.

APPLICATION INFORMATION

Output Voltage Adjustment

The output voltage of THPM4301A can be adjusted from 0.6V to 3.6V using an external resistor between VADJ pin and AGND pin, as shown in Fig. 15. The required resistor value R_{ADJ} can be calculated using equation (1).

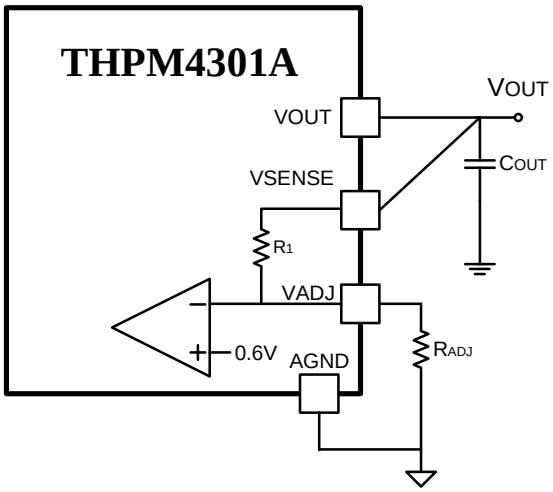


Fig. 15 Output Voltage Setting

$$R_{ADJ}(K\Omega) = \frac{R_1 \times 0.6}{V_O - 0.6} \quad (1)$$

where R1 = 20kΩ and V_O is the desired output voltage in Volts. For best set-point accuracy, it is recommended to use a 0.1% tolerance resistor. [**Note**: R1 is internal to the module as shown in Fig. 15].

Transient Response

The following table summarizes the measured output voltage overshoot and undershoot when the load current undergoes a step change between 2A and 5A. The slew rate for the current change is 1A/μs. The measured waveforms are given from Fig. 16 to Fig. 21. The measurement is obtained when the input capacitor consists of one 47μF ceramic capacitor in parallel with one 220μF electrolytic capacitor, and the output capacitor consists of four 47μF ceramic capacitors in parallel. If smaller output voltage deviation is required, larger output capacitor values can be used.

Table 1. Output Voltage Transient Response

Testing Conditions: C_{IN1} = 1 x 47μF CERAMIC, C_{IN2} = 220μF ELECTROLYTIC, C_{OUT} = 4 × 47μF CERAMIC

V_{IN} (V)	V_{OUT} (V)	3A LOAD STEP, 2A to 5A, (1A/μs)	
		VOLTAGE DEVIATION (mV)	RECOVERY TIME (μs)
3.3	1.0	50	155
5.0		45	145
3.3	1.2	55	150
5		50	150
3.3	1.8	70	170
5		65	165

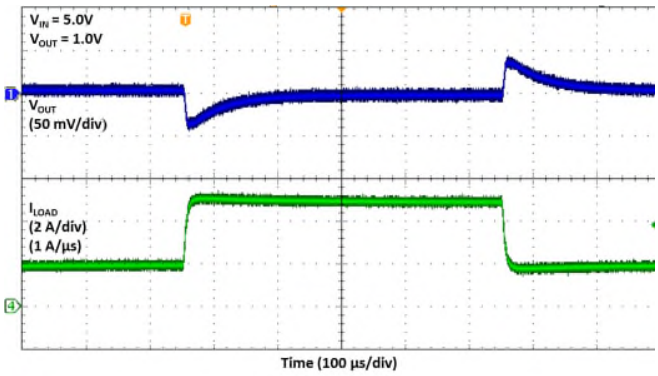


Fig. 16 V_{IN} = 5V, V_{OUT} = 1.0V, 3A Load Step

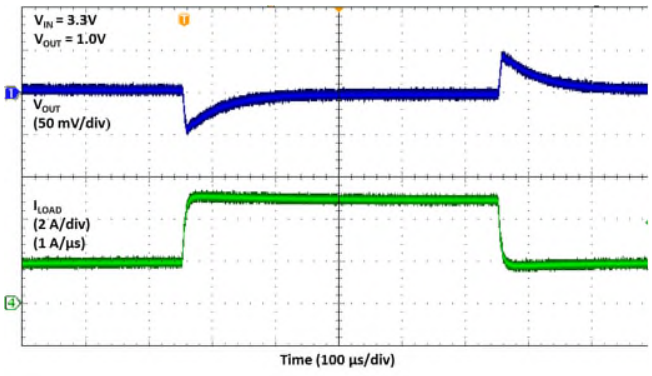


Fig. 17 V_{IN} = 3.3V, V_{OUT} = 1.0V, 3A Load Step

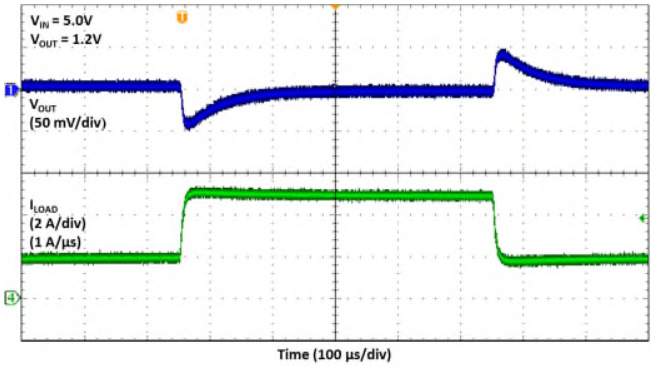


Fig. 18 V_{IN} = 5V, V_{OUT} = 1.2V, 3A Load Step

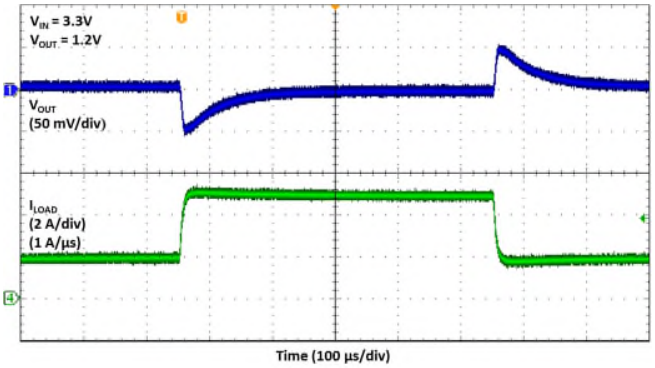


Fig. 19 V_{IN} = 3.3V, V_{OUT} = 1.2V, 3A Load Step

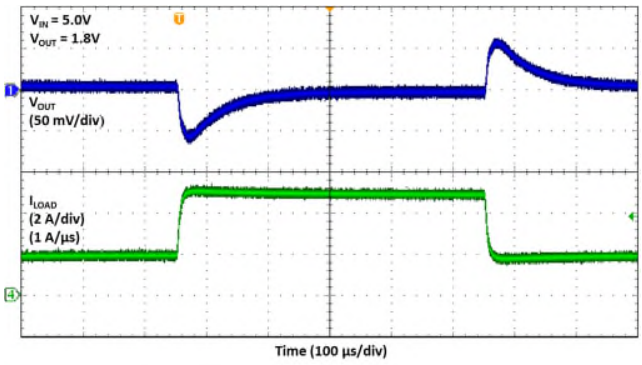


Fig. 20 V_{IN} = 5V, V_{OUT} = 1.8V, 3A Load Step

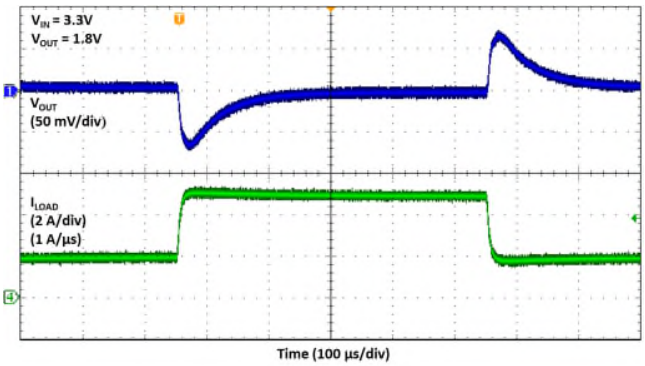


Fig. 21 V_{IN} = 3.3V, V_{OUT} = 1.8V, 3A Load Step

Application Schematics

Fig. 22 shows a typical schematic for a 1.2V output application using THPM4301A with switching frequency of 500 kHz. The adjustment resistor, R_{ADJ}, is selected as 20kΩ calculated based on Equation (1). RT/CLK is connected to ground with a 787kΩ resistor to select the recommended switching frequency. STSEL pin is connected to AGND to select the default startup time. The ON/OFF CONTROL signal is used to turn on and off the power module.

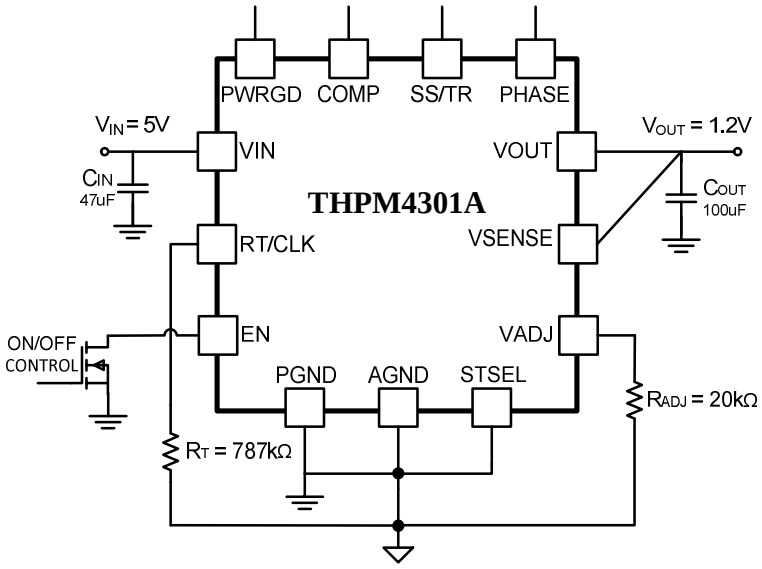


Fig. 22 Typical Schematic V_{IN} = 2.95V to 6.0V, V_{OUT} = 1.2V, F_S = 500kHz

Fig. 23 shows a typical schematic for a 5V input, 3.6V output application using THPM4301A. The adjustment resistor, R_{ADJ}, is selected as 4.02kΩ calculated based on Equation (1). In this example, the switching frequency is selected as 750kHz by connecting the timing resistor of 127kΩ between RT/CLK pin and AGND pin.

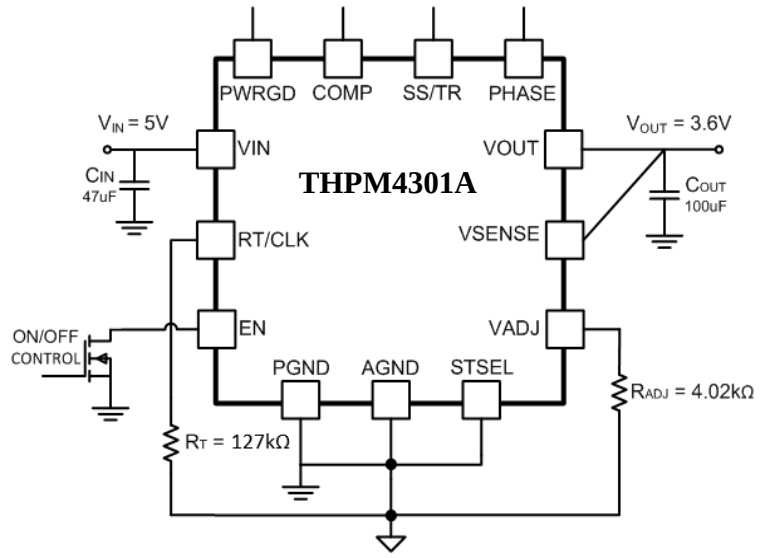


Fig. 23 Typical Schematic V_{IN} = 4.4V to 6.0V, V_{OUT} = 3.6V, F_S = 750kHz

Power Good (PWRGD)

The PWRGD pin is an open drain output, and can be used to indicate when the output voltage is within the normal operating range. This pin is pulled low when VSENSE voltage is less than 91% or greater than 105% of the nominal output voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, or if the EN pin is pulled low.

There is a 2% hysteresis, so once the VSENSE pin is within 93% to 103% of the nominal output voltage the PWRGD pin is de-asserted and the pin floats.

It is recommended to use a pull-up resistor between 1kΩ and 100kΩ to a voltage source that is 5.5V or less. The PWRGD will be in a valid state (high or low as above) once the VIN input voltage is greater than 1.2V.

Power-Up Characteristics

When configured as shown in the front page schematic (page 1), THPM4301A produces a regulated output voltage whenever a valid input voltage is present.

During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the charging current to the output capacitor.

Fig. 24 shows the startup waveforms for THPM4301A, operating from a 5V input and with the output voltage adjusted to 1.8V. The waveform is measured with a 3A constant current load.

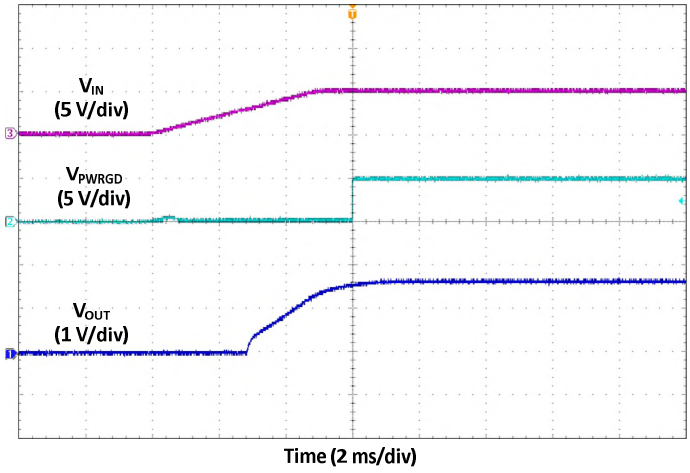


Fig. 24 Startup Waveforms

Enable (On/Off) Operation and Under Voltage Lockout (UVLO) Setup

The EN pin provides an external on/off control of the power module and is lightly pulled up internally with a current source. The module is enabled if this pin is left open or its voltage exceeds the V_{EN-H} threshold voltage, and the power module starts operation once the input voltage is higher than V_{START}.

When the voltage at EN pin is below the V_{EN-L} threshold voltage, the power module stops switching and enters low quiescent current state.

If an application requires controlling the EN pin, an open drain or open collector logic can be used to interface with the pin, as shown in Fig. 25. In this figure, high ON/OFF CONTROL signal level (Low EN) disables the power module.

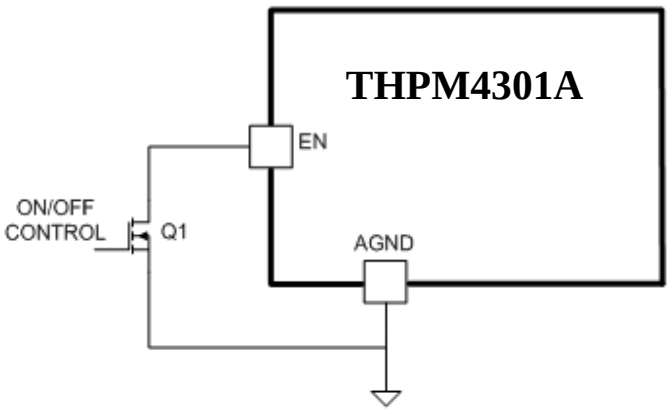


Fig. 25 Typical ON/OFF Control Schematic

Fig. 26 and Fig. 27 show the typical output voltage waveforms when THPM4301A is enabled (turned on) and disabled (turned off) by the EN pin. In these figures, the top trace is the power good signal, the middle trace is the EN pin voltage, and the bottom trace is the output voltage.

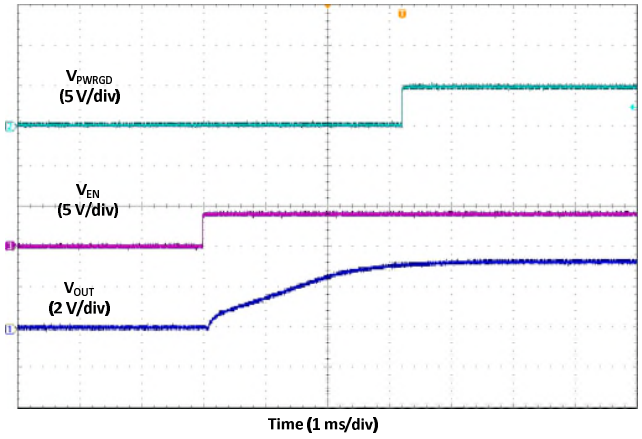


Fig. 26 Waveforms at Enable Turn-On

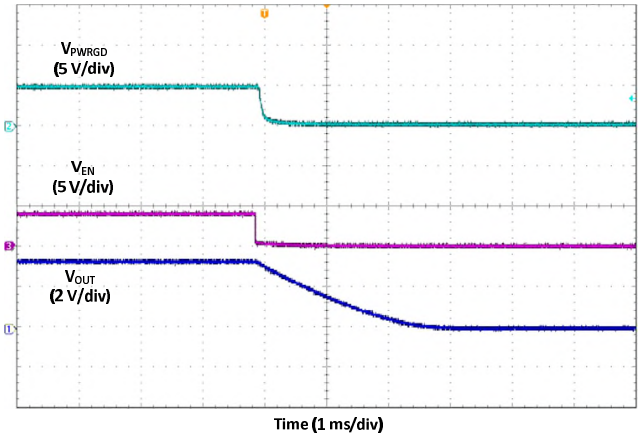


Fig. 27 Waveforms at Enable Turn-Off

Under-voltage lockout can be used to prevent the output from starting until the input voltage is within its normal range. For input under voltage lockout (UVLO) adjustment, use the EN pin as shown in Fig. 28 to set the UVLO level by using two external resistors. Once the EN pin voltage exceeds 1.3V, an additional 2.8μA of current is added to provide input voltage hysteresis. Resistor R_{EN1} and R_{EN2} can be calculated using Equations (4) and (5) based on the required startup voltage and shutdown voltage.

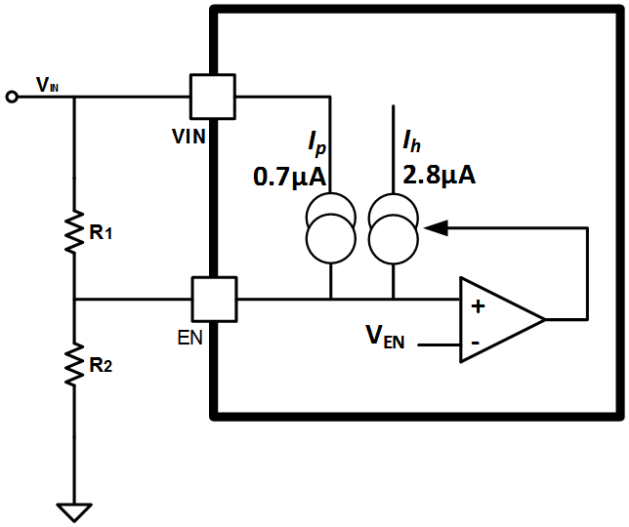


Fig. 28 Input Under-Voltage Lockout Setup

$$R_{EN1} = \frac{V_{START}\left(\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) - UVLO}{I_p\left(1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_h} \quad (4)$$

$$R_{EN2} = \frac{R_{EN1} \times V_{EN\_FALLING}}{UVLO - V_{EN\_FALLING} + R_{EN1} \times (I_p + I_h)} \quad (5)$$

I_h = 2.8μA, I_p = 0.7μA, V_{EN_RISING} = 1.3V, $V_{EN\_FALLING}$ = 1.18V.

As an example, if R_{EN1} = 14.7k Ω and R_{EN2} = 12.7k Ω, V_{START} will be 2.8V and UVLO will be 2.5V.

It is recommended to set the minimum UVLO level of the module at 2.45V or higher to ensure proper operation before shutdown.

Soft-Start or Tracking Pin (SS/TR)

The soft-start function forces the output voltage to rise gradually to its nominal value rather than rising as rapidly as possible. Soft-Start mode is selected when the module is used independently without tracking or sequencing. To select soft-start operation mode the STSEL pin is connected to AGND. This will activate the internal soft-start capacitor for a nominal soft-start time of 1.1ms. An external capacitor between the SS/TR pin to ground can be used to increase the soft-start time to higher values if desired.

Table 2 shows the soft-start time using typical soft-start capacitor values.

Table 2. Soft-start capacitor values and soft-start time

External capacitor (nF)	open	4.7	10
SS Time (ms)	1.1	2.7	4.4

If other startup time is needed, Equation (6) provides the relationship between the external soft-start capacitor value C_{SS} and the soft-start time, T_{SS}.

$$C_{SS} = 3 \times T_{SS}(ms) - 3.3(nF) \quad (6)$$

During the soft-start period, VSENSE voltage will follow the SS/TR pin voltage up to 90% of the nominal voltage setpoint. When the SS/TR voltage is greater than 90% of the nominal voltage, the effective system reference voltage will be changed from the SS/TR voltage to the internal voltage reference to close the voltage loop.

If the input voltage falls below the UVLO, or a thermal shutdown event occurs, or the EN pin is pulled down to below 1.18V, the THPM4301A will stop switching and the SS/TR will be discharged to below 60mV before the module restarts.

Sequencing and Tracking

The term sequencing is used when two or more separate modules are configured to start one after the other, in sequence. The term tracking is used when two or more modules are configured so that they start together, with their output voltages tracking each other during startup. This is done by having one module act as a master and the other(s) act as slave(s). Sequencing and tracking startup can be implemented using the SS/TR, EN and PWRGD pins.

The sequential startup connection is shown in Fig. 29. The power good pin (PWRGD) of the first THPM4301A module is connected to the EN pin of the second THPM4301A module, which will be enabled only after the output voltage of the first THPM4301A module reaches regulation range and its PWRGD is asserted. **Note**: The THPM4301A can start in sequence with another THPM4301A or with any other POL having a compatible Power Good output.

With tracking mode the output voltage of the THPM4301A is controlled by another voltage applied to its SS/TR input. Tracking startup of two THPM4301A modules can be achieved by connecting a resistor network of R_1 and R_2 as shown in Fig. 30, where the output voltage of the second THPM4301A module (bottom) will track the output voltage of the first THPM4301A module (top). In this case, the soft-start time of THPM4301A module #1 is determined by the capacitor connected to its SS/TR pin and the STSEL pin is connected to ground. The voltage at SS / TR pin of the second THPM4301A module is directly controlled by the output voltage of the first THPM4301A module through the resistor divider (R_1 and R_2). The STSEL pin of the second THPM4301A module should be left open.Resistor divider R_1 and R_2 in Fig. 30 can be calculated using Equations (7) and (8). **Note**: The THPM4301A can track any external voltage, so the master can be a THPM4301A or any other POL.

$$R_1 = \frac{V_{OUT1} \times 5}{0.9} (k\Omega) \quad (7)$$

$$R_2 = \frac{0.9 \times R_1}{V_{OUT1} - 0.9} (k\Omega) \quad (8)$$

Fig. 31 gives the output voltage waveforms of two THPM4301A modules operating in sequential startup mode. It shows that PWRGD signal becomes high when the first THPM4301A (2.5V output in this example) enters regulation and then the second THPM4301A (1.2V output in the example) begins to start up.

Fig. 32 gives the output voltage waveforms of two THPM4301A modules operating in tracking startup mode. It shows that V_{OUT1} follows V_{OUT2} until the lower voltage rail (V_{OUT2}) enters regulation (1.2V in this example). Then, V_{OUT1} continues to rise to its steady state value (2.5V in the example).

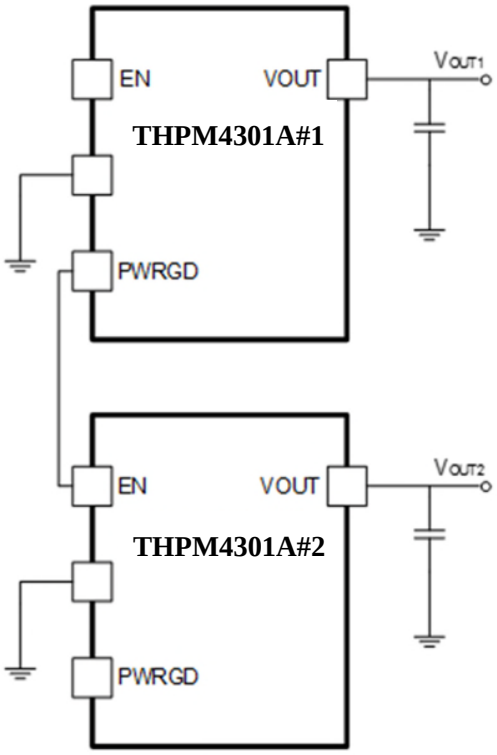


Fig. 29 Sequencing Startup Schematic

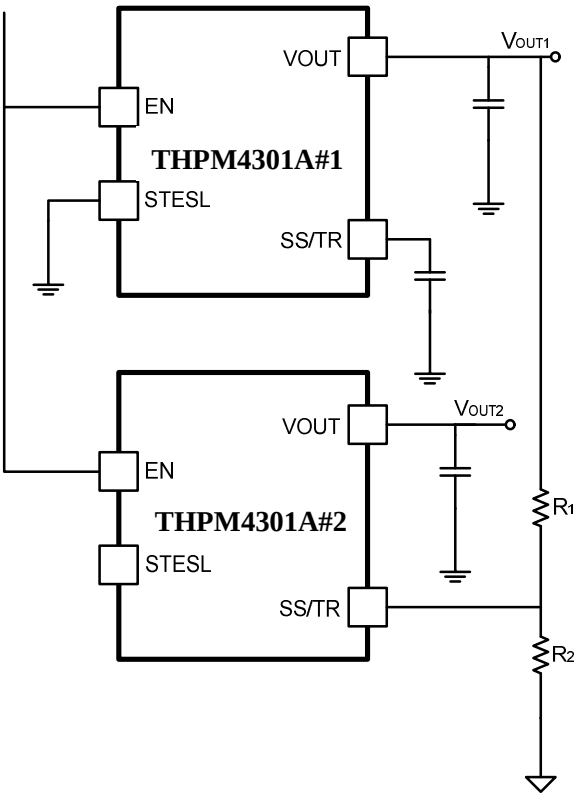


Fig. 30 Tracking Startup Schematic

Note: when used in tracking mode, if the slave unit (module #2 in Fig. 30) shuts down while the other module is still operating, a latch-up condition can occur where the slave unit does not restart. To avoid this, it is necessary to pull down the SS/TR pin of module #2 to below 60mV momentarily, to initiate a normal start-up sequence.

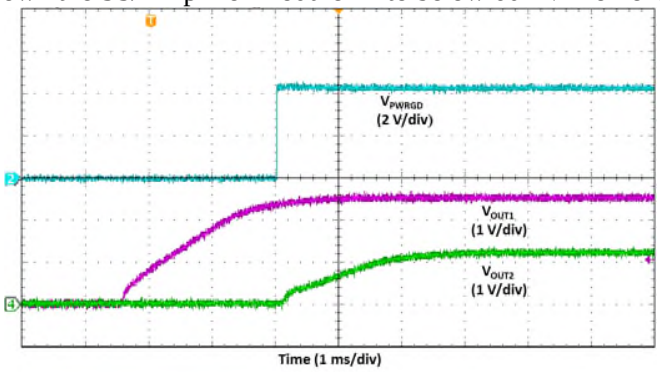


Fig. 31 Sequencing Startup,
V_{OUT1} = 2.5V, V_{OUT2} = 1.2V

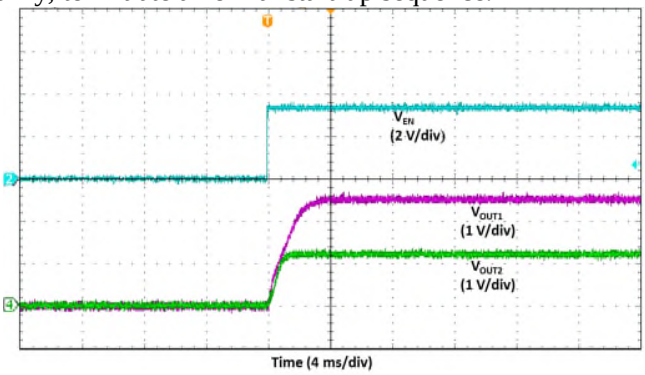


Fig. 32 Tracking Startup,
V_{OUT1} = 2.5V, V_{OUT2} = 1.2V

Switching Frequency Selection and Timing Resistor (RT/CLK Pin)

The switching frequency of the THPM4301A can be adjusted over a wide range from approximately 450 kHz to 750kHz. A resistor between RT/CLK and AGND can be used to increase the switching frequency. An internal resistor, R_{CLK} = 90.9kΩ, sets the minimum (default) switching frequency to 450 KHz. Generally, a higher frequency is preferred for higher output voltages as indicated in Table 3 .

The user can increase the switching frequency by adding an external resistor, R_T, between RT/CLK pin and AGND, as shown in Fig. 33, where R_T is calculated using Equation (9). The relationship between switching frequency and R_T resistor value is shown in Fig. 34.

$$R_T(k\Omega) = \frac{R_{CLK}}{\frac{[F_{SW}(kHz)]^{1.052}}{56183} \times R_{CLK} - 1} \quad (9)$$

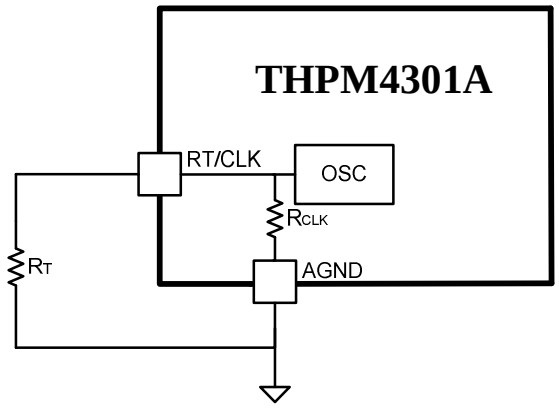


Fig. 33 Switching Frequency Adjustment

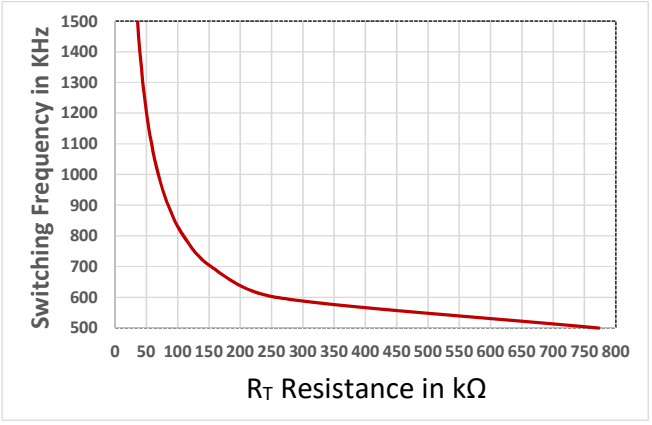


Fig. 34 Switching Frequency vs R_T for THPM4301A

The recommended switching frequency for different output voltages is shown in Table 3, which also shows the nearest standard 1% values for R_T.

Table 3. - Recommended switching frequency and R_T value

Output voltage	Recommended switching frequency (kHz)	Resistor R_T
3.3	750	127kΩ
2.5	650	191kΩ
1.8	600	255kΩ
1.5	550	383kΩ
1.2	500	787kΩ
1.0	500	787kΩ
0.8	450	Open
0.6	450	Open

Synchronization with RT/CLK pin

RT/CLK pin can also be used to synchronize the THPM4301A to an external system clock, as shown in Fig. 35. To implement the synchronization feature, a clock signal with on time of at least 75ns should be applied to the RT/CLK pin. The logic zero level of the clock signal must be lower than 0.6V and the logic high level of the clock signal must be higher than 1.6V. The synchronization frequency range is between 450kHz and 750kHz.

The rising edge of the phase node (PHASE) will be synchronized to the falling edge of RT/CLK pin.

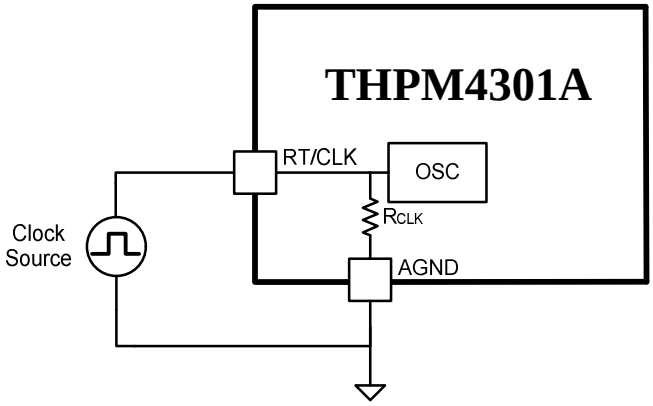


Fig. 35 Synchronizing to a System Clock

Over-Current Protection

A hiccup current limiting function is provided in the THPM4301A to protect against output overload or short-circuit. During an over-current condition, the load current is initially limited to approximately 9A and the output voltage is reduced to approximately 0.8V as shown in Fig. 36. If the over-current condition is not removed within approximately 1ms, the module will be shut down, as shown in Fig. 37. [Please note that the time scale is different for these two figures.

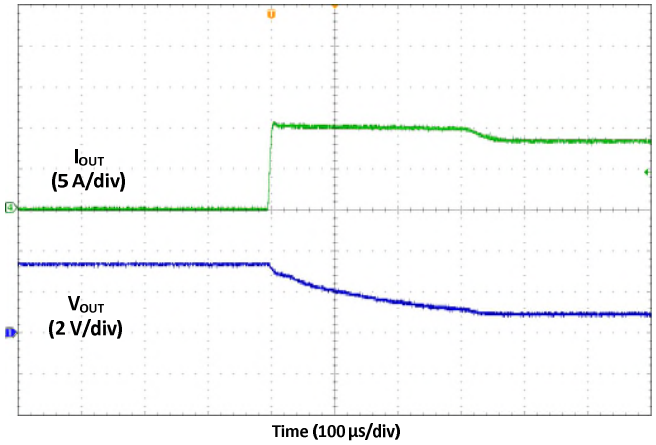


Fig. 36 Over-current Limiting

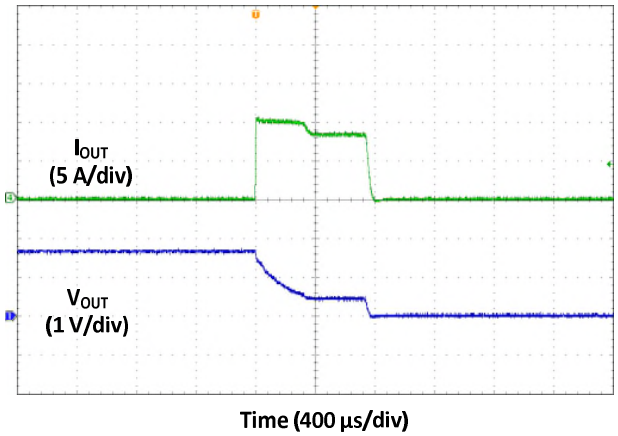


Fig. 37 Hiccup Mode Current Limit Shut-down

When the over-current condition is removed, the output voltage recovers automatically to the nominal voltage, as shown in Fig. 38. If the over-current condition is not removed, the power module operates in hiccup mode, as shown in Fig. 39. The hiccup period is about 25ms.

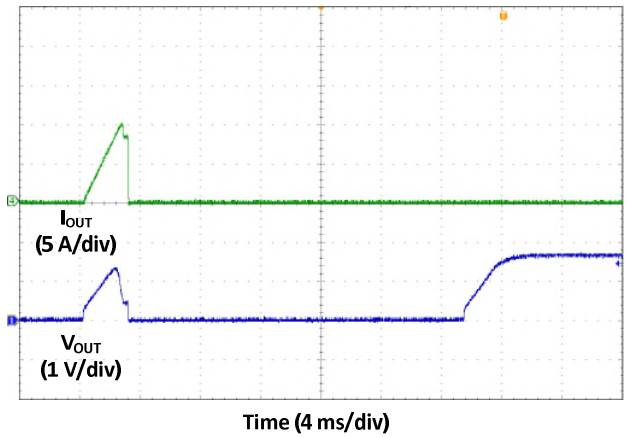


Fig. 38 Recovery from Over-current Shut-down

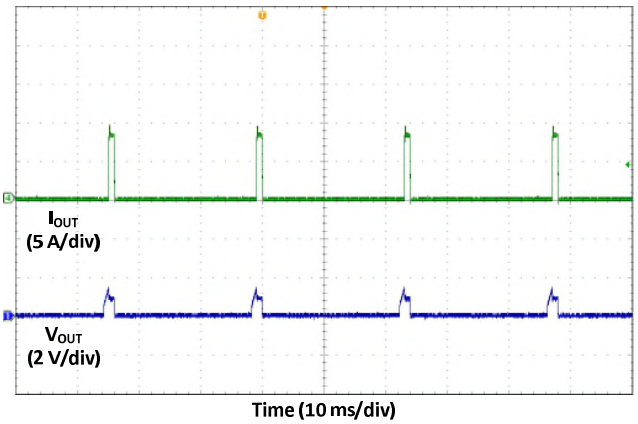


Fig. 39 Hiccup Mode Current Limit Restart into Short-Circuit

Input protection

In most applications, the input power source provides current limiting (typically fold-back or hiccup mode) and as long as the average fault current is limited to approximately 10A or less, no further protection is required.

If the THPM4301A is powered from a battery or other high current source, it is recommended to include an external fuse (maximum 10A) in the input to the module. The THPM4301A includes full protection against output overcurrent or short-circuit, and the fuse will not operate under any output overload condition.

Thermal Considerations

The absolute maximum junction temperature is 150°C but it is recommended to keep the operating temperature well below this value. Maximum recommended case temperature is 115°C, which corresponds to a junction temperature of approximately 125°C.

The thermal resistance from case to ambient (θ_{CA}) depends on the PCB layout as well as the amount of cooling airflow. When mounted on the EVM, θ_{CA} is approximately 15°C/watt in still air.

THPM4301A implements an internal thermal shutdown to protect itself if the junction temperature of the power MOSFET exceeds 170°C. The thermal shutdown forces the module to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature reduces by about 15°C, the module restarts automatically.

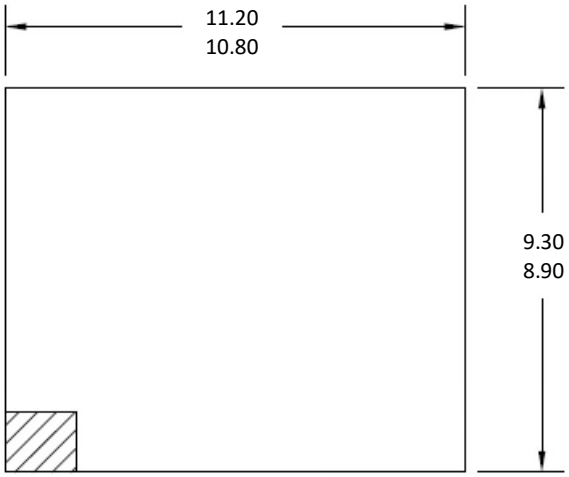
Layout Considerations

To achieve the best electrical and thermal performance, an optimized PCB layout is required. Some considerations for the PCB layout are:

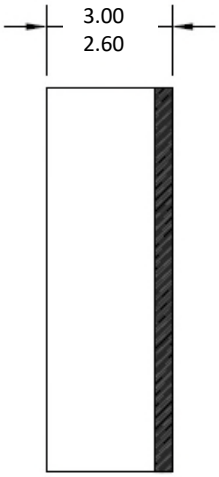
- Use large copper areas for power planes (V_{IN}, V_{OUT}, and especially PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Place any additional output capacitors between the main ceramic capacitor and the load.
- Connect the AGND and PGND copper areas at a single point, preferable under the AGND pin of the module.
- Place R_{SENSE}, R_T, and C_{SS} as close as possible to their respective pins.
- Do not connect the PHASE pin to any other components.
- Use multiple vias to connect the power planes to internal layers.

Package dimensions and PCB pads

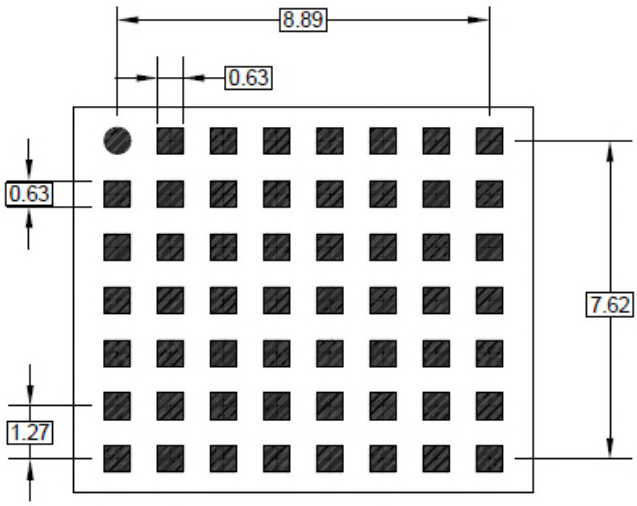
ALL DIMENSIONS IN MILLIMETERS
FLATNESS OF LGA PLANE: MAX 0.1mm



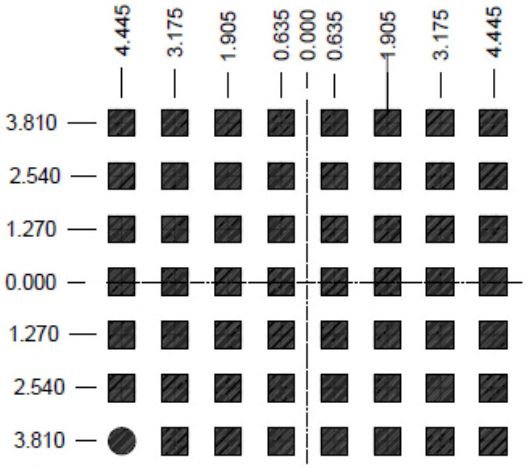
Package Top View



Package Side View



Package Bottom View



Suggested PCB Layout
Top View

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