THV3056

3ch Buck/Boost 2ch CP 1ch HVLDO 1ch LVLDO Controller

Description

THV3056 is a 3ch Buck/Boost Controller IC which enables to design simple & low cost multi-channel power supply system.
Ch-1(fixed Boost), ch-2 and ch-3(fixed Buck) are PWM controllers. As to ch-2, the output of 1.2V is available because the reference voltage of ch-2 is 0.85V.
VGH and VGL are selectable Positive/Negative charge pumps and PFM controller.
Built-in high voltage LDO and Vcom buffer amplifier facilitate to design various power supply systems for large scale TFT panels.
THV3056 achieves easy phase compensation even with a ceramic capacitor for the output.
SS_1/2/3, SS_SW, DTC1/2/3, DTC_VGH/DTC_VGL and SCP help to design user defined soft start time, dead time and timer latch delay time. Two types of startup sequence are selectable by controlling SEL1 pin.
THV3056 is suitable for power supply system of TFT LCD bias and system board with multi -channel power supply.

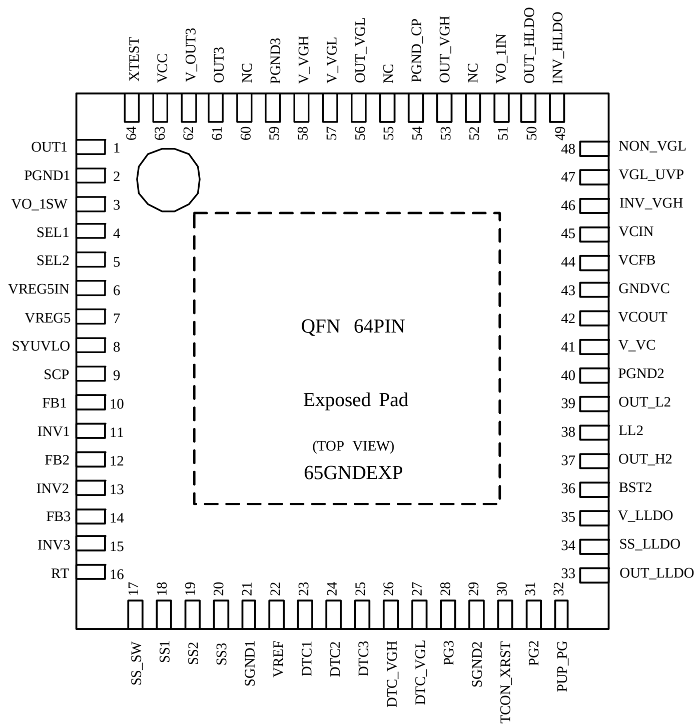
Features

- QFN 64 pin package
- Input Voltage range : 4.2~ 15V
- Push Pull output for direct Power MOS driving
- Ceramic Capacitors are available for output
- Complete PWM mode controller
- Positive/Negative charge pumps (selectable PFM mode)
- Adjustable switching frequency up to 1MHz
- Timer Latch Protection
- System UVLO function
- Adjustable Soft Start time
- Adjustable Timer Latch Delay time
- Adjustable Dead Time Control
- Thermal Shutdown
- Ch-1, Boost converter
- Ch-2, Synchronous Buck converter
- Ch-3, Boost/Buck/Inverting converter
- High voltage LDO
- LDO of 3.3V
- Vcom Buffer Amplifier

Applications

- TFT-LCD Bias power supply

Pin Assignment

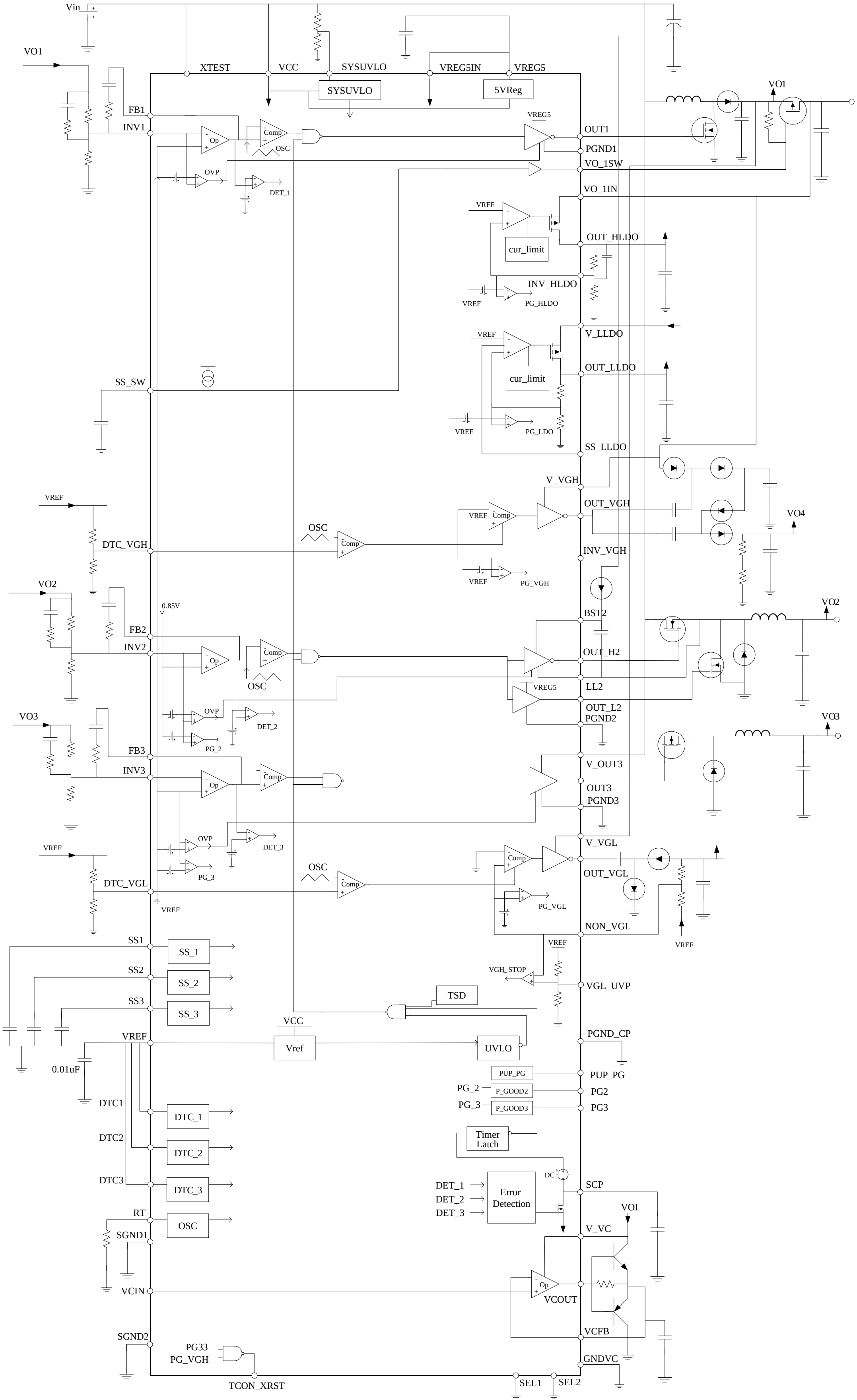


Output Channel Description

Output Channel	Description
CH-1	PWM Boost converter
CH-2	PWM Buck converter (NMOS transistor drive for synchronous rectifier / available for diode rectification)
CH-3	PWM Buck converter
VGH	Positive charge pump Selectable PFM mode
HVLDO	High voltage LDO Input voltage range : 6V to 17V
VGL	Negative charge pump Selectable PFM mode
LVLDO	LDO of 3.3V Input Voltage range : 4.2 to 5.5V
VO_1SW	Output for the external load switch. The load switch is soft-closed by setting capacitance connected to SS_SW pin.
Vcom Buffer Amplifier	Output Voltage range : 1 to VO_1IN-1V

Block Diagram

THV3056 TFT Multi Channel Controller



Pin Description

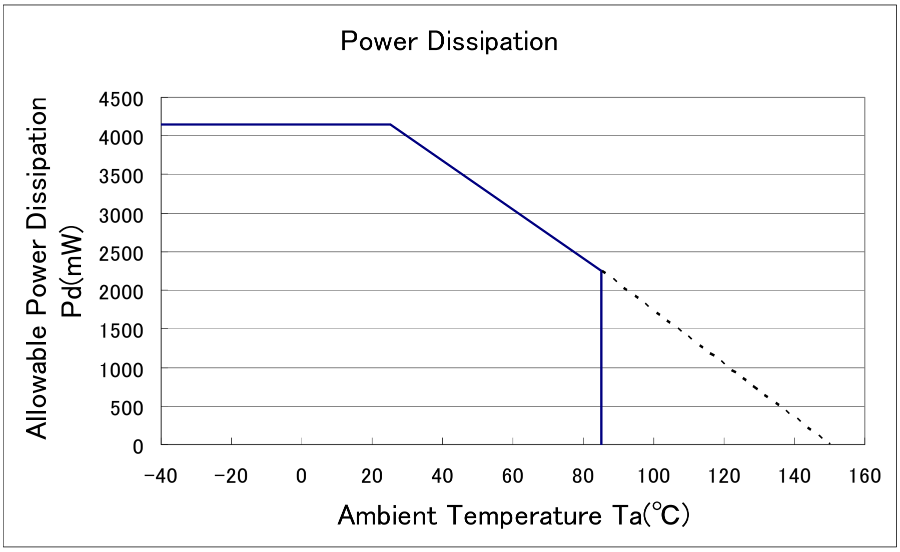
Pin#	Symbol	Function	Description
10 12 14	FB1 FB2 FB3	ch-1,ch-2,ch-3 error amplifier output	Ch-1,2,3 error amplifier outputs for phase compensation by connecting resistors and capacitors between FB_1,2,3 and INV_1,2,3.
11 13 15	INV1 INV2 INV3	ch-1,ch-2,ch3 error amplifier inverting input	Ch-1,2,3 error amp inverting inputs. The voltage on INV1 and INV3 are 1.2V, and INV2 is 0.85V, in the normal operation.
18 19 20	SS1 SS2 SS3	ch-1,ch-2,ch-3 soft start	Soft start pin for ch-1/2/3. Voltage at power-on is ground level. Constant 1mA current source charges capacitors connected to these pins. Soft start time can be adjusted by external capacitors connected these pins. On/Off control is available by connecting the external open drain ports or PG pins.
23 24 25	DTC1 DTC2 DTC3	ch-1,ch-2,ch-3 Dead Time Control	To limit the maximum duty cycle on ch-1,2,3. See Functional Description “DTC” for detail.
17	SS_SW	ch-1 soft start of external PMOS switch	Ch-1 external PMOS switch for soft start. Voltage at power-on is ground level. Constant 1mA current source charges the capacitor connected to this pin. Soft start time of PMOS transistor to VO_1SW can be adjusted by external capacitors connected this pin. On/Off control is available by connecting the external open drain ports or PG pins.
46	INV_VGH	VGH comparator inverting input	VGH comparator inverting input. The voltage on this pin is 1.2V in the normal operation.
48	NON_VGL	VGL comparator non-inverting input	VGL comparator non-inverting input. The voltage on this pin is 0V in the normal operation.
26 27	DTC_VGH DTC_VGL	VGH (charge pump +)control VGL (charge pump -)control	VGH, VHL charge pump control pins. When the input voltage is High level, these pins are On state. Low level, Off state. Using as charge pump, please set the duty cycle of 50%. In PFM mode, these pin operate as DTC. See Functional Description “DTC” for detail.
22	VREF	Reference voltage	Reference voltage of 1.2V. Connect this pin with an external capacitor of 0.01uF for stability. The maximum load current is 1mA.
4	SEL1	Startup sequence select	Two type of startup sequence are selectable by connecting SEL1 pin to GND or VREG5 pin. See Functional Description “Startup Sequence”.
5	SEL2	Charge pump UVP timer latch On/Off control	Charge pump UVP timer latch On/Off control is available by SEL2 pin. See Functional Description “SCP” for detail.
41	V_VC	Voltage supply for Vcom output	Voltage supply for Vcom output.
47	VGL_UVP	UVP voltage of VGL set pin	UVP voltage can be set optionally by connecting an external resistor to this pin. Without external resistor, UVP voltage is set at 50% of the reference voltage.

Pin#	Symbol	Function	Description
62	V_OUT3	Output power supply for OUT3	Output power supply for OUT3.
64	XTEST	Test mode select	Connect to VCC in normal operation.
16	RT	Timing resistor for oscilla-tor	Resistor connection pin to set oscillation frequency. See Functional Description “Oscillation Circuit” for detail.
21 29	SGND1 SGND2	Signal GND	GND for control circuit.
45	VCIN	Vcom buffer amplifier non-inverting input	Vcom buffer amplifier non-inverting input.
43	GNDVC	Power GND for Vcom buffer amplifier	Power GND for Vcom buffer amplifier.
44	VCFB	Vcom buffer amplifier inverting input	Vcom buffer amplifier inverting input.
42	VCOUT	Vcom buffer amplifier output	Vcom buffer amplifier output. Connecting external bipolar transistor, it can accept high output current.
9	SCP	Timer Latch short circuit protection	Setting the delay time of SCP timer latch circuit. The delay time means the period from detection of abnormal operations, to shut down of IC. See Functional Description “Short Circuit Protection” for detail.
31 28	PG2 PG3	Power good output	Open drain output. Connect an approximately 100k ohm pull-up resis-tor. During soft start, when the voltage of SS pin rise up to the predeter-mined voltage(ch-2/1V, ch-3/1.35V), PG pin output goes High level. When soft start has finished normally, the output is fixed to High level. Do not connect the pull-up resistor to higher voltage than VREG5.
32	PUP_PG	Power good resistor connection pin	Connecting PG pins with external control pins and also shorting VCC pin and VREG5 pin, the resistor connected to PG pin should be pulled up to PUP_PG pin.
2 40 54 59	PGND1 PGND2 PGND_CP PGND3	Power GND	GND for power circuit.
56	OUT_VGL	VGL (charge pump -)output	VGL drive output for negative voltage charge pump. V_VGL is used as input power supply. In PFM mode, this pin can be used as PMOS gate drive.

Pin#	Symbol	Function	Description
37	OUT_H2	ch-2 High side drive output	Ch-2 High side NMOS transistor drive for synchronous rectifier.
36	BST2	ch-2 High side capacitor connection pin	Ch-2 power supply for High side drive output.
53	OUT_VGH	VGH (charge pump +)output	VGH drive output for positive voltage charge pump. V_VGH is used as power supply. In PFM mode, this pin can be used as NMOS gate drive.
57	V_VGL	VGL output voltage supply	VGL output voltage supply.
58	V_VGH	VGH output voltage supply	VGH output voltage supply.
49	INV_HLDO	HVLDO amplifier inverting input	HVLDO inverting input. The voltage on this pin is 1.2V in the normal operation.
50	OUT_HLDO	HVLDO output	HVLDO output. Connect to an external capacitor(Typ:2.2uF).
51	VO_1IN	HVLDO voltage supply	HVLDO voltage supply.
34	SS_LLDO	LVLDO soft start	Soft start pin for LVLDO.
33	OUT_LLDO	LVLDO output	LVLDO output. Connect to an external capacitor(Typ:10uF).
35	V_LLDO	LVLDO voltage supply	LVLDO voltage supply.
3	VO_1SW	ch-1 control output for switch	Ch-1 gate control output for the external switch. The voltage is in proportion to the voltage on SS_SW pin.
1	OUT1	ch-1 output	Ch-1 drive output for the external FET of Boost. 0~5V
6	VREG5IN	Voltage supply for control	Connect to VREG5 pin.
7	VREG5	5V regulator output	Power supply for Low voltage output. Connect this pin with an external capacitor (Typ:4.7uF).
8	SYSUVLO	System UVLO input	SYSUVLO pin shuts down the IC, when the power supply voltage is lower than the predetermined voltage. Vin voltage divided by resistance is applied. The minimum operation voltage can be set optionally by changing the resistance value. If not in use, connect this pin to VREF or VREG5 pin.
63	VCC	Power supply for control	Power supply for control.
39	OUT_L2	ch-2 Low side driver output	Ch-2 Low side NMOS transistor drive for synchronous rectifier. Available even without Low side NMOS transistor. But in this case, set the load current of ch-2 at more than 10mA.
38	LL2	ch-2 inductor node connection pin	Ch-2 inductor node connection pin.
61	OUT3	ch-3 output	Ch-3 drive output for an external FET of Buck(push-pull). 0 ～ V_OUT3
52 55 60	NC	NC	No connection. Leave open.
65	GNDEXP	back side	GNDEXP should be soldered to GND to improve the thermal characteristics.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input power supply voltage	Vcc	18	V
INV1/2/3, INV_VGH/INV_VGL, FB1/2/3, NON_VGL, DTC1/2/3, DTC_VGH/DTC_VGL, SS1/2/3, SS_SW, PG2/3, SYSUVLO, SCP, SEL1/2, VREG5IN, VGL_UVP	VL_in1	6.5	V
BST2-LL2, OUT_H2-LL2	VL_in2	6.5	V
XTEST	VH_in1	18	V
VCIN, VCFB	VH_in2	20	V
OUT1, VREF, RT, OUT_L2, VREG5, PUP_PG, TCON_XRST	VL_out	6.5	V
VCOUT, OUT_HLDO, OUT_VGL, OUT_VGH, VO_1SW	VH_out1	20	V
LL2, OUT3	VH_out2	18	V
V_VGL, V_VGH, V_OUT3, V_VC	VH_cc	20	V
BST2, OUT_H2	VH_out3	24	V
Output Current OUT1, OUT_L2, OUT_H2, OUT3, OUT_VGH, OUT_VGL	Iomax	1	A
Output Current OUT_HLDO	Iomax2	80	mA
Power dissipation	Pd	4125 (Ta<25°C)	mW
Junction temperature	Tj	150	°C
Operating temperature	Ta	-40 °C +85	°C
Storage temperature	Tstg	-55 °C +150	°C
Lead temperature for soldering	Tlead	255 / +5 / -0 / 10sec	°C



Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
VCC voltage(Input Power Supply Voltage)	4.2		15	V
VREG5,VREG5IN voltage	4.2		5.5	V
LL2, V_OUT3 voltage	4.2		17	V
V_VGH, V_VGL voltage	4.2		17	V
VO_1IN, V_VC voltage	5.5		17	V
V_LLDO	4.2		5.5	V
BST2, OUT_H2 voltage	-0.1		20	V
OUT3 voltage	-0.1		17	V
VO1_SW, VCFB, VCOUT, VCIN, OUT_HLDO, OUT_VGH, OUT_VGL	-0.1		17	V
OUT1, SYSUVLO, INV1/2/3, INV_VGH, INV_HLDO, DTC1/2/3, DTC_VGH, DTC_VGL, PG2,3 OUT_L2, VREG5, PUP_PG, VGL_UVP, SEL1,2 voltage	-0.1		5.5	V
FB1/2/3, SS1/2/3, SS_LLDO, VREF, RT voltage	-0.1		3	V
OUT_LLDO, TCON_XRST voltage		3.3		V
External capacitance for VREF pin		0.01		uF
External capacitance for VREG5 pin	2.2	4.7		uF
External capacitance for OUT_HLDO pin	1	2.2		uF
OUT_HLDO output current		10		mA
External capacitance for OUT_LLDO pin		10		uF
OUT_LLDO output current			300	mA
Oscillation frequency	200		1000	kHz
X_TEST voltage		VCC		V

Electrical Characteristics

(at Vcc = 12V, RT= 47kohm, Ta = 25°C , unless otherwise noted)

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage Block						
Reference voltage	Vref	Cvref = 0.01uF	1.188	1.2	1.212	V
Reference voltage(ch-2)	Vref(ch2)	Vref x 0.85/1.2	0.841	0.85	0.859	%
Temperature coefficient	Vref(tc)	Iref = -100uA, Ta = -40 ~ 85°C		± 0.5		%
Line regulation	Vref(line)	Iref = -100uA, Vcc = 4.2 ~ 15V		2	5	mV
Load regulation	Vref(load)	Iref = -100uA ~ -1mA		2	5	mV
Oscillator Circuit Block						
Oscillation frequency	Fosc	RT = 47kΩ	460	500	540	kHz
Temperature coefficient	Fosc(tc)	Ta = -40 ~ +85°C		± 5		%
DTC Circuit Block						
Maximum duty cycle (ch-1,3)	Dmax (ch-1,3)			89		%
Maximum duty cycle(ch-2)	Dmax(ch-2)			85		%
Maximum duty cycle (VGH)	Dmax (VGH)			93		%
Maximum duty cycle (VGL)	Dmax (VGL)			87		%
Error Amplifier Block						
Offset voltage	Vio1,Vio3	Based on VREF pin voltage	-10		10	mV
	Vio2	Buffer connection Based on the value : VREF x 0.85/1.2				
Open loop gain	Vav			70		dB
Unity gain bandwidth	Bw			1.5		MHz
Output sink current	Isnk	Vfb = 1.0V	40	100		uA
Output source current	Isrc	Vfb = 1.0V	1	3		mA
SS offset voltage	Vsso			0.2		V
Charge Pump Block						
Threshold voltage (VGH)	Vthc(VGH)			1.2		V
Threshold voltage (VGL)	Vthc(VGL)			0		V
Offset voltage(VGH/VGL)	Vioc (VGH/VGL)		-20		20	mV

Parameters	Symbol	Condition	Min	Typ	Max	Unit
High Voltage LDO Block						
Offset voltage	Vhvldo(off)	Ildo = -1mA	-20		20	mV
Load regulation	Vhvldo(load)	VO_1IN = 16V, OUT_HLDO = 15V Ildo = -0.1m ~ -2mA		15	40	mV
High side output voltage range	Vhldo(hrange)	Ildo = -10mA	VO_1IN -0.5	VO_1IN -0.2		V
Low side output voltage range	Vhldo(lrange)	Ildo = -10mA	5.5			V
Dropout voltage	Vdrop(hldo)	Ildo = -10mA,VO_1IN = 16V, INV_HLDO = 0V		0.18	0.35	V
Low Voltage LDO Block						
Output voltage	Vout(lldo)	Iout_lldo = 200mA	3.2	3.3	3.4	V
Load regulation	Vlldo(load)	1mA < Iout_lldo < 300mA		33		mV
Line regulation	Vlldo(line)	4.2V < V_LLDO < 5.5V Iout_lldo = 200mA		10		mV
Dropout voltage	Vdrop(lldo)	V_LLDOpin Iout_lldo = 200mA, Vout = 3.2V		3.3		V
Vcom Buffer Amplifier Block						
Offset voltage	Vvcom(off)	VO_1IN = 15V, VCIN = 5V	-10		10	mV
Load regulation	Vvcom(load)	Io = 0 ~ ± 5mA	-50		50	mV
Line regulation	Vvcom(line)	VO_1IN = 6V ~ 17V		2	10	mV
Input common mode voltage range	Vvcom(range)	R_L = 10k Ω	1		VO_1IN -2	V
Output source maximum load current	Ivcomh(max)		30	70		mA
Output sink maximum load current	Ivcoml(max)		30	70		mA
Input bias current	Iib(vcom)			0.5	2.5	uA
5V Regulator Block						
Output voltage	Vreg5(range)	Io = -1mA		5.0		V
Load regulation	Vreg5(load)	Io = -0.1mA ~ -5mA			100	mV
Line regulation	Vreg5(line)	Io = -1mA, VCC = 5.5V ~ 15V			20	mV
Soft Start Block						
SS1,2,3 charge current	Iss	Vss = 0.5V	0.6	1.0	1.4	uA
SS_SW charge current	Isssw	Vss_sw = 0.5V		1		uA
SS_LLDO charge current	Isslldo	Vss_lldo = 0.5V		1		uA

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Switch Control Block						
Output voltage for load switch	Vo(vo_1in)	Vss_sw = 1.2V, V_VGL = 18V		15		V
Output resistance for VO_1SW	Ro(vo_1sw)	Io = 1mA, SS_SW = 2.5V		1.2		kΩ
Power Good Block						
Output resistance	Ropg	PG = Low Io = 1mA		0.9	1.6	kΩ
PUP_PG output resistance	Rpup_pg	Io = -1mA		0.4		kΩ
SS2 threshold voltage	Vpgss2			1		V
SS3 threshold voltage	Vpgss3			1.35		V
INV_VGH, INV_HLDO threshold voltage	Vpg_vgh,hldo			1.02		V
NON_VGL threshold voltage	Vpg_vgl			0.18		V
OUT_LLDO threshold voltage	Vpg_lldo	OUT_LLDO pin		2.64		V
VGL_UVP Block						
VGL_UVP threshold voltage	Vuvp_vgl			0.6		V
VGL_UVP pin input resistance	Ri(vgl_uvp)			500		k Ω
Output Block						
OUT1 H level output resistance	Roh(ch-1)	Ioh = -50mA		17		Ω
OUT1 L level output resistance	Rol(ch-1)	Iol = 50mA		11		Ω
OUT_H2 H level output resistance	Roh(ch-2h)	Ioh = -50mA		17		Ω
OUT_H2 L level output resistance	Rol(ch-2h)	Iol = 50mA		13		Ω
OUT_L2 H level output resistance	Roh(ch-2l)	Ioh = -50mA		17		Ω
OUT_L2 L level output resistance	Rol(ch-2l)	Iol = 50mA		6		Ω
OUT3 H level output resistance	Roh(ch-3)	Ioh = -50mA		13		Ω
OUT3 L level output resistance	Rol(ch-3)	Iol = 50mA		7		Ω
OUT_VGH H level output resistance	Roh(vgh)	V_VGH = 15V, Ioh = -50mA		10		Ω
OUT_VGH L level output resistance	Rol(vgh)	V_VGH = 15V, Iol = 50mA		9		Ω
OUT_VGL H level output resistance	Roh(vgl)	V_VGL = 15V, Ioh = -50mA		26		Ω
OUT_VGL L level output resistance	Rol(vgl)	V_VGL = 15V, Iol = 50mA		16		Ω
TCON_XRST H level output resistance	Roh(xrst)	OUT_LLDO = 3.3V, Iol = -50mA		14		Ω
TCON_XRST L level output resistance	Rol(xrst)	OUT_LLDO = 3.3V, Iol = 50mA		24		Ω

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Over Voltage Protection Block						
Threshold voltage (ch-1, ch-3)	Vovp (ch-1,ch-3)	INV1/INV3 pin		1.5		V
Threshold voltage (ch-2)	Vovp(ch-2)	INV2 pin		1.063		V
UVLO Block						
On threshold voltage(VCC)	Vuvlo	VCC pin(H>L), Ivreg5 = -1mA		2.54		V
Hysteresis voltage(VCC)	Vuvlo(hys)	VCC pin, Ivreg5 = -1mA		200		mV
On threshold voltage (VREG5IN)	Vuvlo	VREG5IN pin (H>L)		2.55		V
Hysteresis voltage (VREG5IN)	Vuvlo_vreg5 (hys)	VREG5IN pin		239		mV
System UVLO Block						
On threshold voltage	Vsysuvlo	SYSUVLO pin(H>L)	0.97	1.00	1.03	V
Hysteresis voltage	Vsysuvlo(hys)	SYSUVLO pin	0.13	0.22	0.31	V
Timer Latch Block						
Threshold voltage	Vlat	SCP pin	1.15	1.20	1.25	V
Charge current (UVP)	Iscp(uvp)	Vscp = 0.1V	0.6	1.0	1.4	uA
Charge current (OVP)	Iscp(ovp)	Vscp = 0.1V	3.0	5.0	7.0	uA
SCP reset voltage	Vscp(rst)	VCC pin		1.6		V
Control Block						
SEL1/SEL2 H level threshold voltage	Vsel1(h) Vsel2(h)		VREG5IN -0.5V		VREG5IN	V
SEL1/SEL2 L level threshold voltage	Vsel1(l) Vsel2(l)		0		0.5	V
Overall						
Average Current Consumption	Icc(op)	Output swing On (VCC)		4.5	9.0	mA
	Icc	Output swing Off, SS_1/2/3 = 0V, DTC_1/2/3,DTC_VGH, DTC_VGL = 0V (VCC)		3.5	7.0	mA

Functional Description

● **System UVLO**

System UVLO stops IC operation when the input voltage decreases less than the user defined voltage.

UVLO(Undervoltage Lockout) prevents the device from the malfunction under the lower VCC voltage at which IC can not operate normally. However in the actual system board, it is often required not to operate DC/DC controller IC under the voltage which is defined by the individual system, even if the voltage is enough high for normal operation of the IC. Utilizing System UVLO function, it is able to control the IC operation only with two external resistors. The below Figure 1 shows the example set at more than 4.0V(Vin), and Figure 2 shows the operation example of System UVLO.

After Input Power Supply Voltage(Vin) rises up to the release voltage of UVLO(4.27V in this example), the Soft Start operation starts and the voltage on SS pin rises gradually. When the voltage reaches to 1.2V, Soft Start operation is finished and the output voltage reaches to the user defined voltage.

When input power supply voltage(Vin) drops to the system UVLO detection voltage (under 3.5V in this example), System UVLO stops all switching operations instantly and the voltage on SS pin will be pulled down to Gnd level. As switching operation stops, the output voltage decreases. The shut off mode by the detection of system UVLO will be released, when Vin exceeds the system UVLO release voltage. (See Figure 2)

$$\text{Release Voltage of System UVLO} = 1.22 \times \frac{R1 + R2}{R2}$$

$$\text{Detection Voltage of System UVLO} = 1.0 \times \frac{R1 + R2}{R2}$$

Generally input power supply voltage(Vin) decreases when the output short circuit or over load.are detected. The decrease of input power supply voltage resets the SCP. Please pay attention of setting the System UVLO voltage and the SCP timer latch delay time.

Note1)

Please set the System UVLO voltage and SCP delay time in order that the shut off by SCP works earlier than System UVLO operation. Otherwise, the following operation will be repeated:

Output short-circuit → Power-supply voltage decrease (UVLO operation) → Shut off by System UVLO → Short-circuit current decrease → Power-supply voltage rise (UVLO release) → Out put short circuit remaining → Power-supply voltage decrease → Shut off by System UVLO

If System UVLO is not required, connect SYSUVLO pin with VREF or VREG5 pin.
In that case, only internal UVLO circuit will operates.

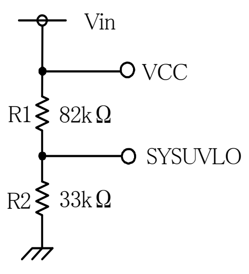


Figure 1. System UVLO Setting Example

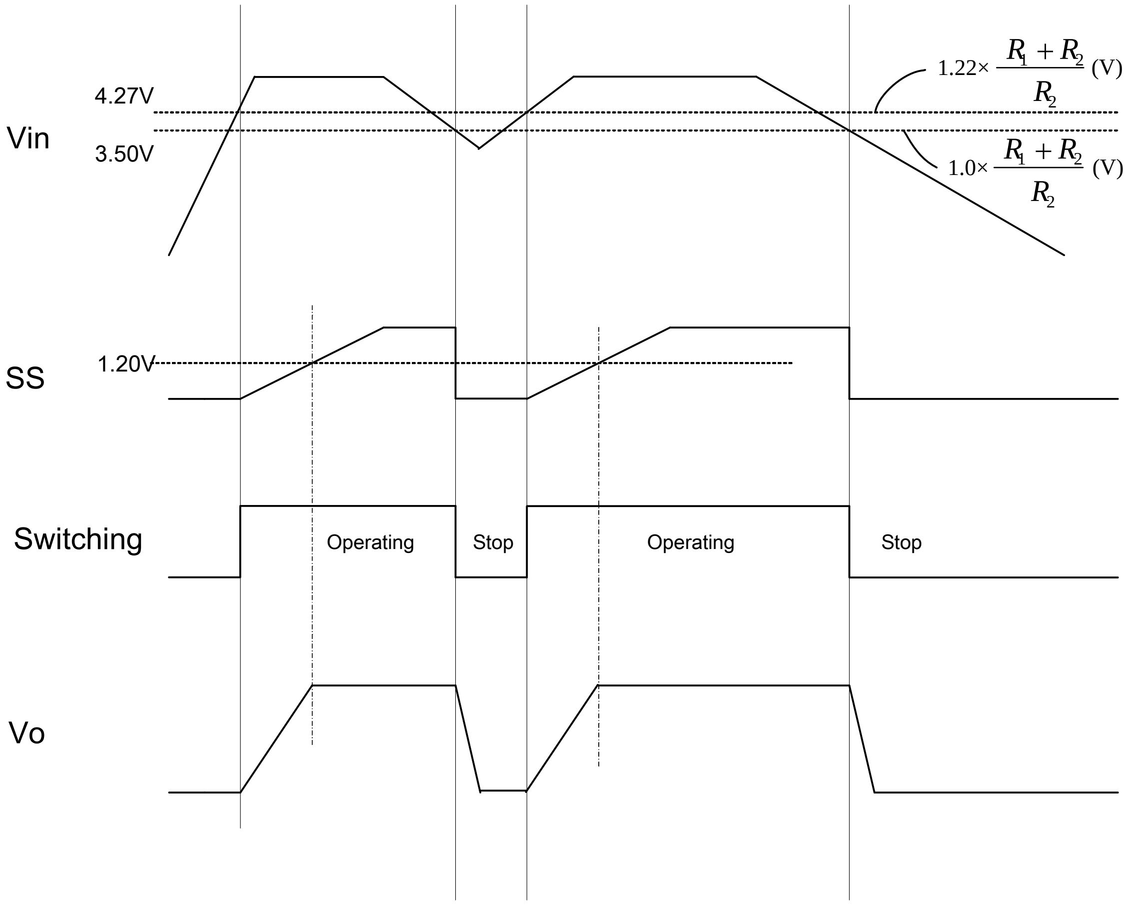


Figure 2. System UVLO Operation Example

● UVLO

If System UVLO is not in use, the internal UVLO circuit will operates. The detection voltage is set at 2.54V, and the release voltage is set at 2.74V.

Note 2) When not in use, connect SYSUVLO pin to VREF pin or VREG5 pin.

● **Soft Start**

THV3056 has Soft Start circuit to prevent high inrush current of the DC/DC converter during start up. SS pins are internally connected to 1uA constant current source and NMOS pull-down transistor. Soft Start time is set by the external capacitor connected between each SS pins and GND.
Pull-down transistor is in the On state and the voltage on SS pins are set at Gnd level, until System UVLO or UVLO is released. On/Off control on each channels are available by connecting SS pins to the external open-drain driver. (See Figure 3)

Error amplifier has three inputs of PMOS transistor, one inverting and the others non-inverting. One of non-inverting inputs is connected to SS pin and the other is connected to internal reference voltage. The reference voltage is 1.2V for ch-1 and ch-3, 0.85V for ch-2. The voltage on SS pin gradually rises up from Gnd level and then exceeds the reference voltage. The lower voltage one is active between two non-inverting inputs using PMOS transistors. Thus the input from SS pin is active if the voltage is under 1.2V for ch-1 and ch-3, 0.85V for ch-2. Also the input from internal reference voltage is active if the voltage on SS pin exceeds 1.2V for ch-1 and ch-3, 0.85 for ch-2.
During Soft Start operation, SS pin is active and the DC/DC converter operates at the voltage on SS pin as the reference voltage. The gradual voltage increase on SS pin is equivalent to the gradual increase on the reference voltage and output voltage. Soft Start operation is completed when the voltage on SS pin reaches to the internal reference voltage.
Soft start time, Tss, is calculated as following :
When Css ≒ 0.01uF , Tss ≒ 12ms for ch-1 and ch-3/ Tss ≒ 8.5ms for ch-2.

$$\mathrm{Tss1,3} \fallingdotseq \frac{1.2}{1\times10^{-6}}\times = 1.2\times10^{6}\times\mathrm{Css}\ (\mathrm{sec})$$

$$\mathrm{Tss2} \fallingdotseq \frac{0.85}{1\times10^{-6}}\times = 0.85\times10^{6}\times\mathrm{Css}\ (\mathrm{sec})$$

Different from DTC type, this type of soft start provides a natural rising-up waveform without overshooting. Soft Start time is defined only by the external capacitor and output voltage rises up in proportion to the gradual voltage rising up on SS pin. Also the sequence setting is easy because it doesn't depend on the load current fluctuation at the power on, and that facilitate the setting of sequences. Please note that the power on during output short circuit causes instant maximum duty operation, because the control circuit recognize that the output voltage doesn't reach to the user defined set voltage.
(See Functional Description "DTC" for detail)

● **PG**

PG pins are open-drain outputs of NMOS pull-down transistor. When the power supply is turned On, NMOS transistor is On and the voltage on PG pin is Gnd level. When the voltage on SS2 pin reaches to approximately 1V for ch-2, SS3 pin reaches 1.35V for ch-3, NMOS transistor is turned Off. When PG pins are connected to external control pins, resistor connection pins must be set according to the power supply voltage.

Table 1 PG Resistor Connection

Power Supply Voltage	Resistor Connection pin
under 5.5V	PUP_PG
higher than 5.5V	VREG5

Connecting PG pins to VCC through approximately 100kohm pull-up resistor, the output voltage on PG pins rises up to High level when output voltage reaches more than 90% of user defined voltage. Those output signals can be utilized for other external circuits, but do not connect to the pull-up resistor to the higher voltage than VREG5.

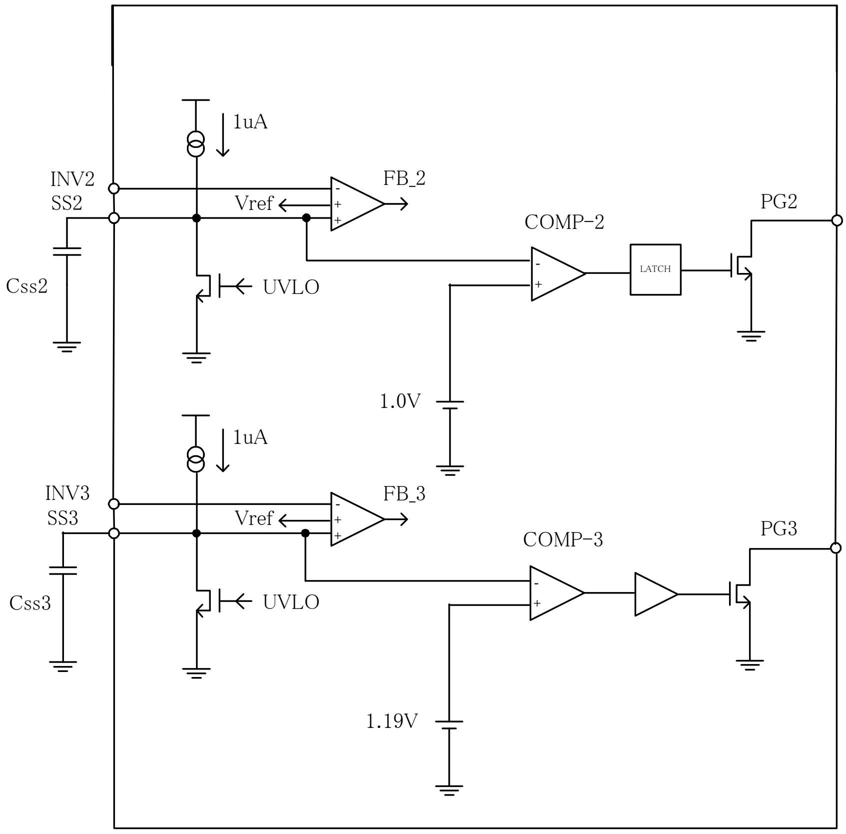


Figure 3. Block Diagram for Sequence using SS and PG

● Low Voltage LDO(of 3.3V output)

Figure 4 shows the circuit diagram of Low voltage LDO. Applies the voltage of 5V to V_LLDO pin and outputs 3.3V. When using the external 3.3V without LDO, short-circuit V_LLDO pin and OUT_LLDO pin and apply 3.3V.

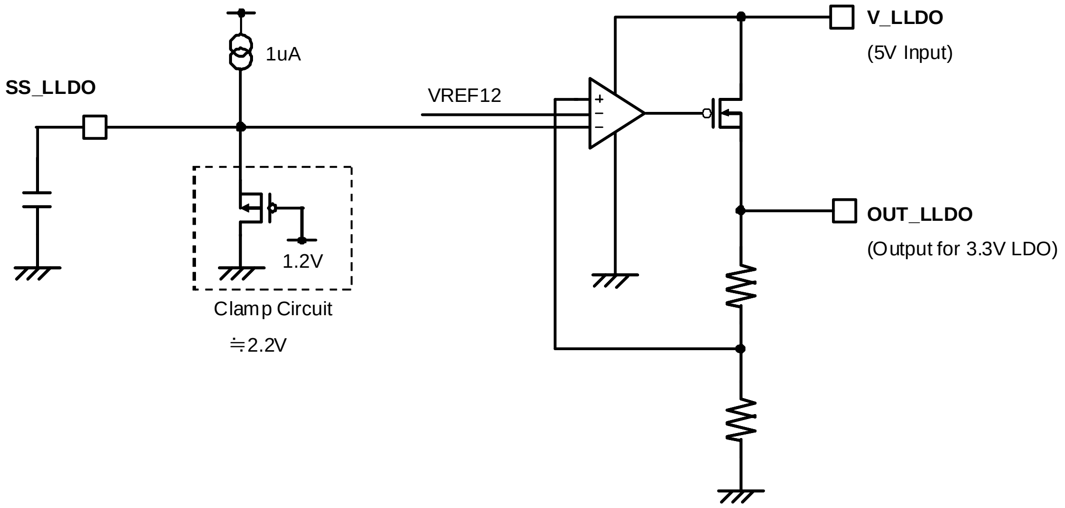


Figure 4. Low voltage LDO Circuit

● TCON Reset Circuit

TCON reset circuit generates a signal of High level, when the startup of OUT_LLDO and VGH are completed normally. (See Figure 5, Figure 6.)

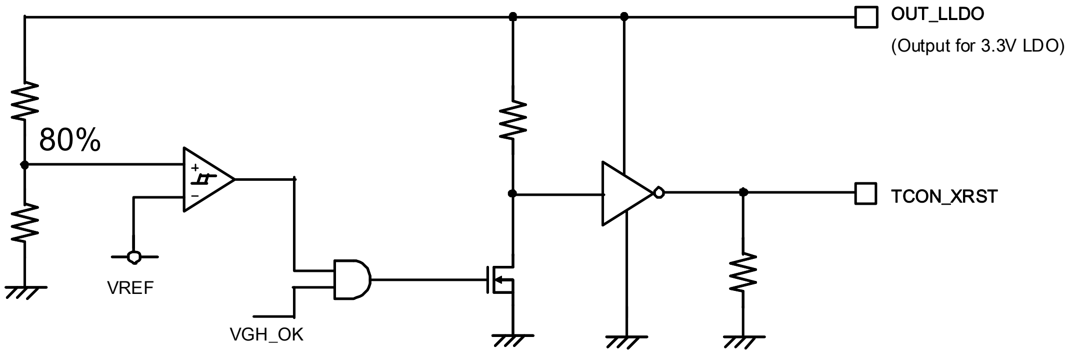
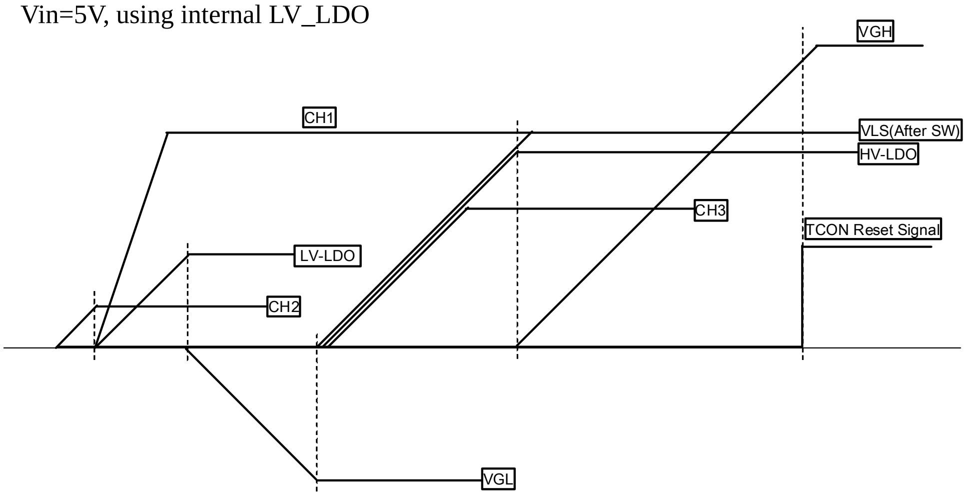


Figure 5. TCON Reset Circuit

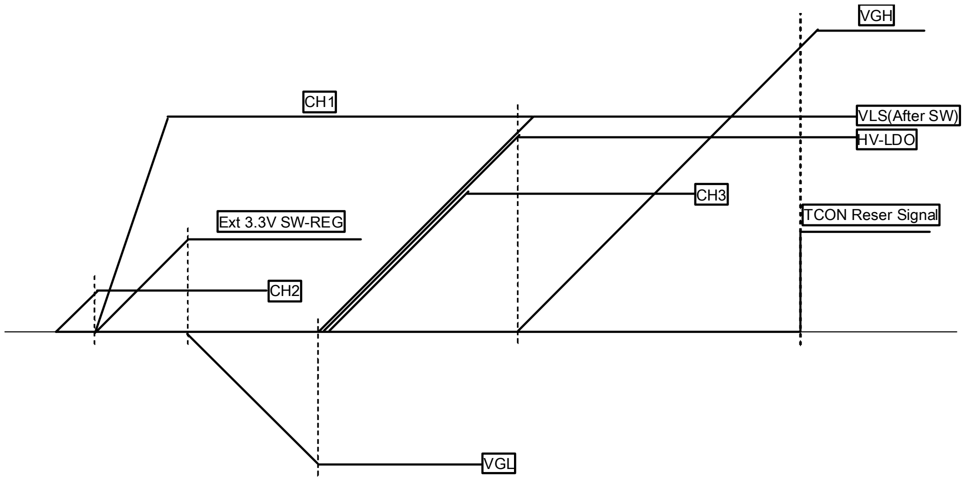
● **Startup Sequence Setting**

SEl1 pin facilitate the startup sequence setting.(See Table 2, Figure 6.)

Setting - 1
Vin=5V, using internal LV_LDO



Setting - 1
Vin=12V, using internal SW_REG of 3.3V.



Setting - 2
Vin=125V, using 3.3V generated from ch-3.

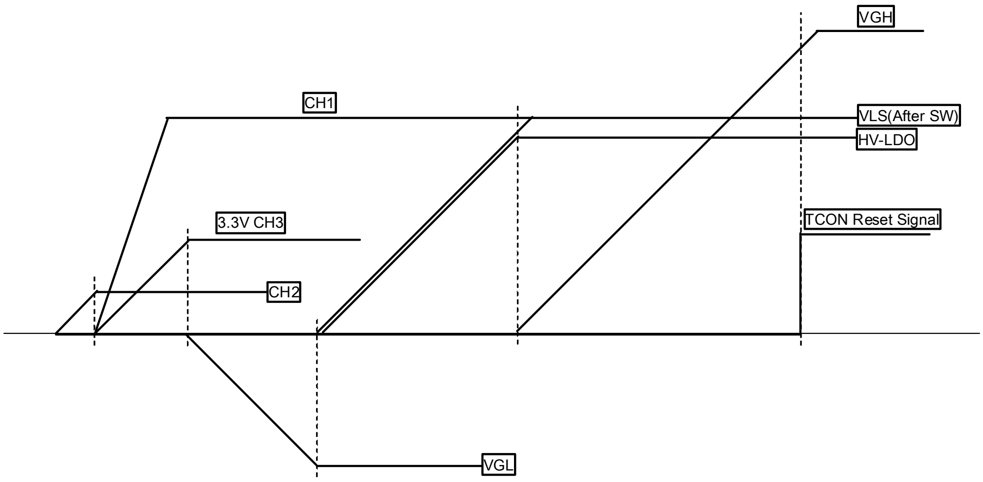


Figure 6. Startup Sequence Waveform

Table 2 SEL1 pin Setting

SEL1 Connection	Startup Sequence
GND	Setting - 1
VREG5	Setting - 2

● **DTC(Dead Time Control)**

Dead Time is set by applying voltage to DTC pins. It prevents the IC from getting into 100% on duty cycle and can set preferable maximum duty cycle for individual system requirement. About relationship between the dead time and the voltage on DTC pin, refer to typical characteristics described later. If not in use, connect DTC pin directly with VREF pin or VREG5 pin. (See Figure 7 (a)(b))

When ch-4,6 are used as charge pumps, set those outputs at 50% duty cycle (approximately 750mV). When used as PFM regulator, soft start can be set by connecting capacitors between DTC pins and GND. (See Figure 7(c)) The maximum duty cycle of ch-1,3 are internally set at 89%, ch-2 85%, VGH 93%, VGL 87%.

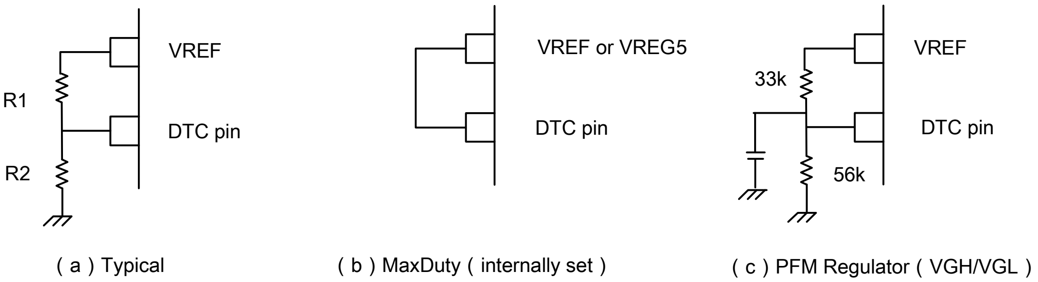


Figure 7. Voltage Apply Example for DTC pin

● **VGL-UVP Circuit**

VGL-UVP circuit detects abnormal drops of output voltage caused by short circuits or over load. The internal VGL-UVP comparator monitors the output voltage of NON_VGL and compare with the value of VREF which is divided in half by resistor. The division value of VREF can be set even by the external resistor.(See Figure 8.) Connect a capacitor of 0.01uF to VGL_UVP pin without using external resistor. If the output voltage drops below the user defined voltage, the system goes into Max Duty cycle and UVP comparator stops VGH and reports the abnormal output of charge pump to SCP circuit.

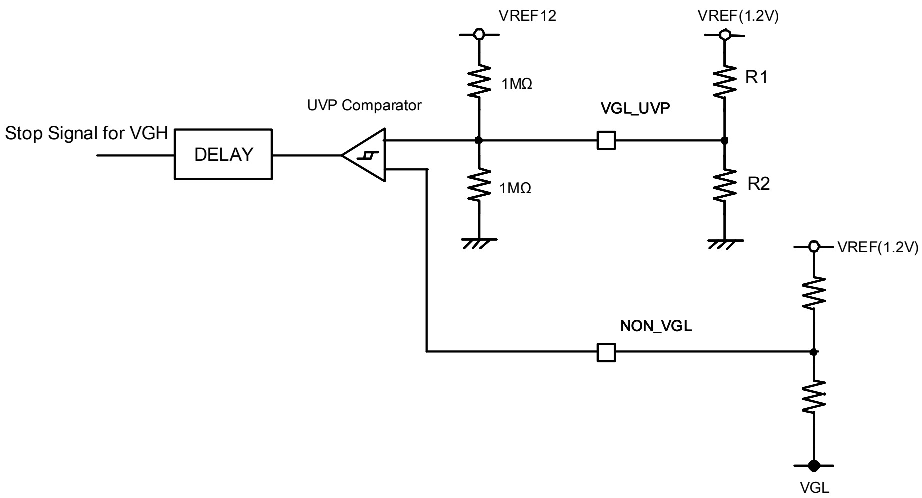


Figure 8. VGL_UVP Circuit

● UVP(Under Voltage Protection)

UVP circuit detects abnormal drops of output voltage caused by short circuits or over load.

The internal UVP comparator monitors the output voltage of error amplifiers(FB1,2,3). In the normal operation the inverting input voltage is approximately 1.2V, same as the non-inverting input connected internally to VREF. The inverting input voltage decreases in proportion to the output voltage drop. If the output voltage drops below the user defined voltage, the system goes into Max Duty cycle and UVP comparator reports the abnormal operation of DC/DC converter to SCP circuit. (See Figure 9)

● Short Circuit Protection（SCP Timer Circuit）

SCP shut down the IC operation when the Max Duty operation/OVP operation /abnormal temperature continue for a longer time than the user defined time. SCP timer circuit has the internal constant source current circuit, a pull-down transistor and an external capacitor connected between SCP pin and GND. In the normal operation the internal pull-down transistor is in On state, and SCP pin is held Gnd level. (See Figure 9.)

When UVP comparator detects the output voltage drop, the pull-down transistor connected with SCP pin is turned to Off and the external capacitor is charged with 1uA constant current. While OVP comparator detects the output voltage rise or the abnormal temperature is detected continuously, the voltage on SCP pin keep on rising in proportion to the time constant defined by 5uA constant current and the external capacitor. When the voltage on SCP pin reaches to 1.2V, the latch operates and then all channels stops and goes into shut down mode. (See Figure 10.) The latch state will not be released until power supply is restarted. The delay time to the latch state can be set by the external capacitance. Also, users can select SCP timer mode(On/Off) of charge pump by SEL2 pin.(See Table 3.)

The delay time Tscp is given by following :

When Cscp=0.01uF and UVP is activated, the SCP delay time (Tscp) is around 12msec. Also, when OVP or TSD is activated, Tovp is around 2.4msec.

In the case of UVP,

$$Tscp = \frac{1.2}{1\times10^{-6}} \times Cscp = 1.2\times10^{6} \times Cscp(sec)$$

In the case of OVP or TSD,

$$Tovp = \frac{1.2}{5\times10^{-6}} \times Cscp = 2.4\times10^{5} \times Cscp(sec)$$

Note 1) When output short circuit or over load occur, the input power supply voltage (Vin) may decrease according to the circumstances. UVLO resets SCP timer latch state, so please set the delay time in order that timer latch works earlier than UVLO operation. Otherwise, the following operation will be repeated:

Output short-circuit → Power-supply voltage decrease (UVLO operation) → Short-circuit current decrease → Power-supply voltage rise (UVLO release) → Power-supply voltage decrease

Note 2) When UVP timer latch function of charge pump is set to be enable, please be careful to determine the delay time considering the startup time of charge pumps. (See Figure 11.)

Table 3 SEL2 pin Setting

SEL2 Connection	Startup Sequence
GND	C.P Timer Latch/Active
VREG5	C.P Timer Latch/Inactive

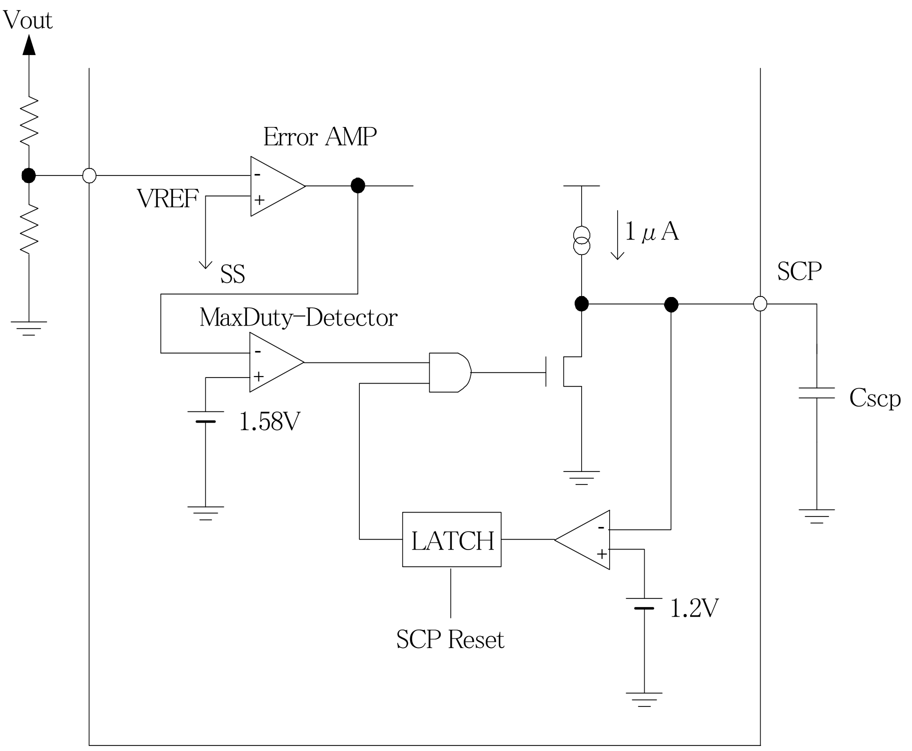


Figure 9. SCP Circuit

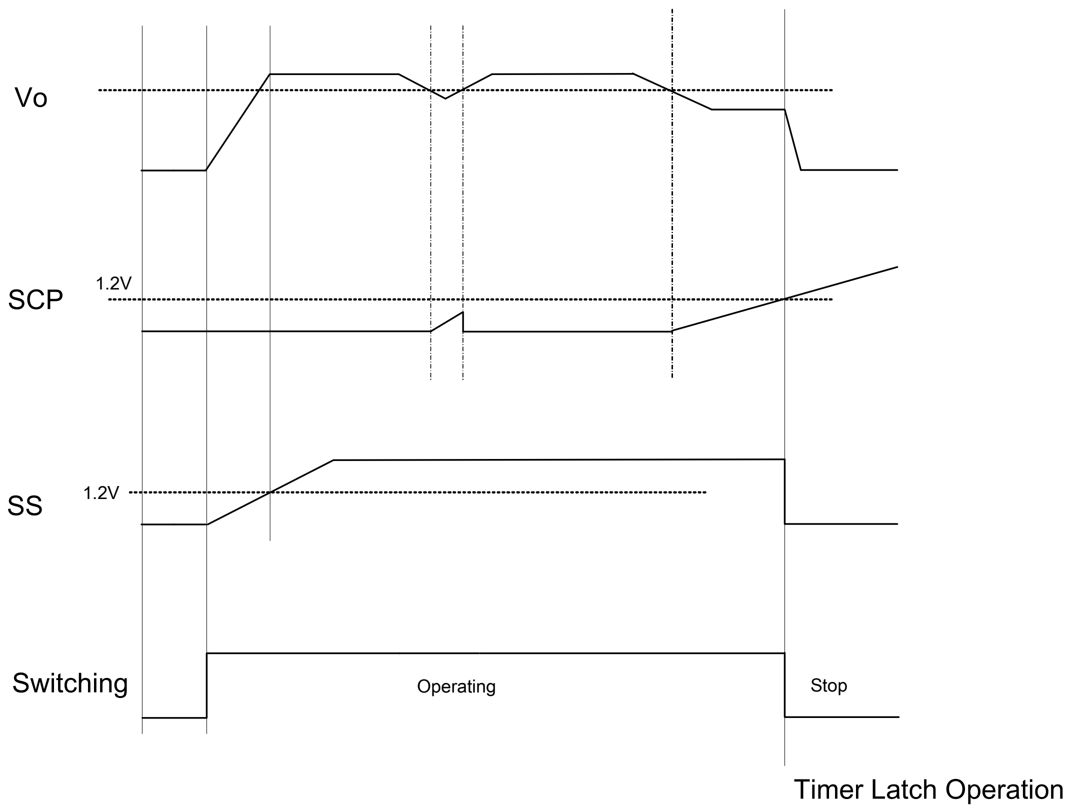
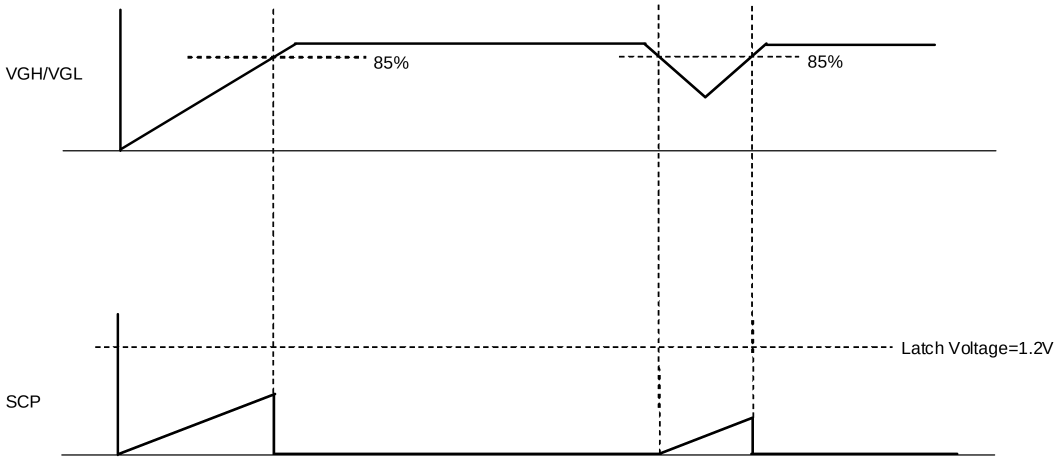


Figure 10. SCP Operation Waveform



SCP Latch Time >> VGH/VGL Startup Time

Figure 11. Charge Pump SCP Operation Waveform

● **Over Voltage Protection(OVP)**

OVP circuit stops the output, if the output voltage on ch-1/2/3 exceed the predetermined voltage. The internal OVP comparator (with reference voltage of 1.5V for ch-1 and ch-3, 1.06V for ch-3) monitors the voltage on INV pins. The output of OVP comparator is connected to OUT pin. When the voltage on INV pin exceeds 1.5V for ch-1 and ch-3, 1.06V for ch-2, OUT pin turns external MOS transistor Off and stops switching operation to prevent the output voltage excessing the predetermined voltage.(See Figure 12.) Also, OVP comparator of ch-2 and ch-3 report the abnormal operation to SCP circuit.

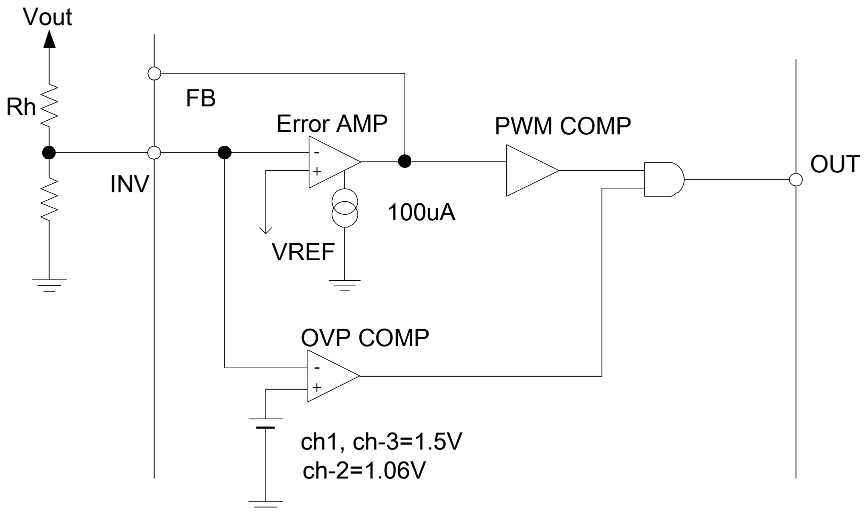


Figure 12. OVP Circuit

Note) Operation at FB - INV short circuit

When FB pin and INV pin are short circuited, the internal constant current circuit (100uA) affects the output voltage. An approximate output voltage is given by the following formula.

The output voltage at FB-INV short circuited(Vout) = the normal output voltage x 1.25 + Rh x 100uA

Also, OVP comparator has Delay circuit of 0.5us to prevent the malfunction, so the actual output voltage will be higher than the result of calculation.

● **Output Voltage Setting**

Figure 13 shows ch-1 output voltage setting model. The voltage on INV1 pin is equal to the voltage on VREF pin due to the effect of feed-back. The voltage on INV_1 pin is the divided voltage of Vout by R1 and R2.

So,

$$\mathrm{Vout1} \times \frac{\mathrm{R2}}{\mathrm{R1}+\mathrm{R2}} = \mathrm{VREF}$$

Therefore,

$$\mathrm{Vout1} = \mathrm{VREF} \times \left(1 + \frac{\mathrm{R1}}{\mathrm{R2}}\right)$$

Since VREF =1.2V, then

$$\mathrm{Vout1} = 1.2 \times \left(1 + \frac{\mathrm{R1}}{\mathrm{R2}}\right)$$

Similarly the output voltage of ch-2 and ch-3 is described as follows.

$$\mathrm{Vout2} = 0.85 \times \left(1 + \frac{\mathrm{R4}}{\mathrm{R5}}\right)$$

$$\mathrm{Vout3} = 1.2 \times \left(1 + \frac{\mathrm{R7}}{\mathrm{R8}}\right)$$

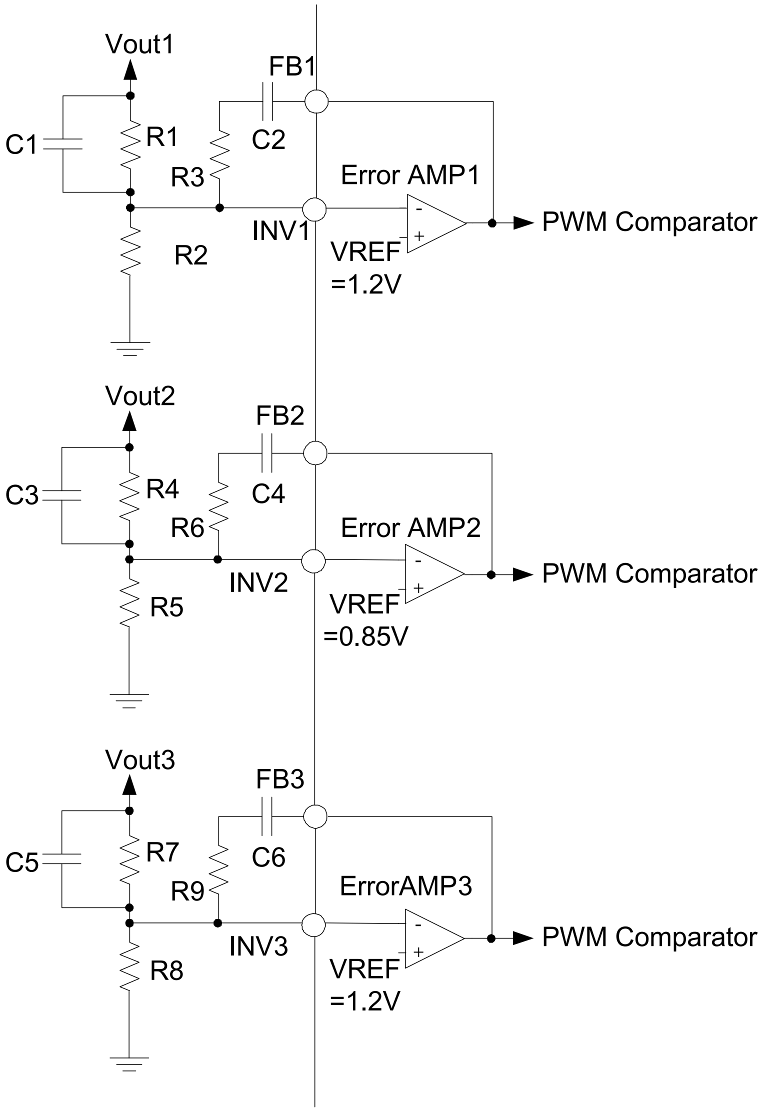


Figure 13. Output Voltage Setting

Description of charge pumps. As to VGH, the voltage on INV_VGH pin is controlled to be equal to the voltage of VREF. (See Figure 14.) The voltage on INV_VGH pin is the divided voltage of VGH by R9 and R10.
So

$$VGH = VREF \times \left(1 + \frac{R9}{R10}\right) = 1.2 \times \left(1 + \frac{R9}{R10}\right)$$

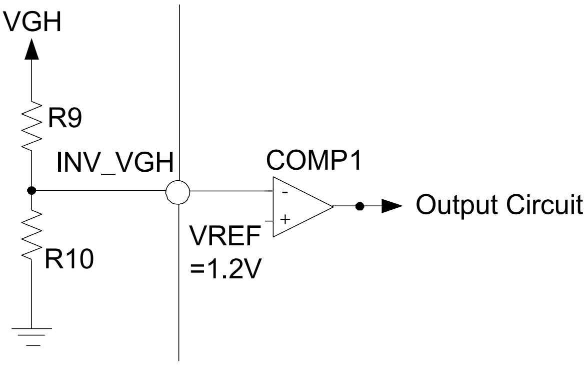


Figure 14. Output Setting for VGH

As to VGL, the voltage on NON_VGL pin is controlled to be zero. (See Figure 15, Figure 16.) The current through NON_VGL is negligible.
Therefore

$$VGL = -(VREF) \times \frac{R11}{R12} = -1.2 \times \frac{R11}{R12}$$

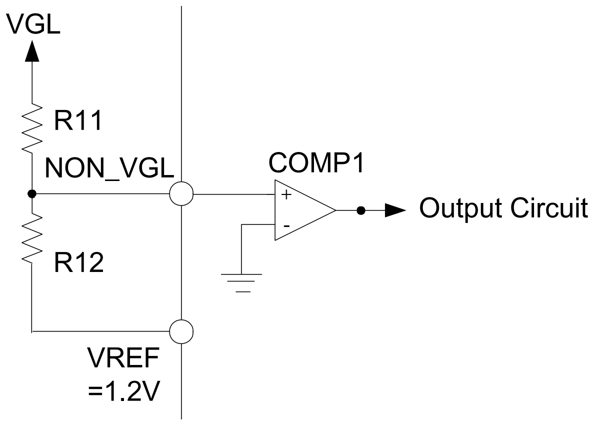


Figure 15. Output Setting for VGL

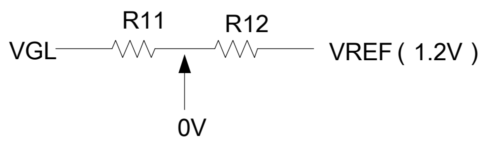


Figure 16. Output Setting for Inverting Mode

● Thermal Shut Down(TSD)

TSD detects abnormal heat and reports it to SCP circuit. The detecting temperature is 175°C, release temperature is 160°C.

● Current Limit Circuit(LDO)

High voltage LDO and Low voltage LDO(of 3.3V output) have built-in auto-recovery current limit function. The threshold current is 250mA for High voltage LDO, 700mA for Low voltage LDO.

● Voltage Reference Circuit

Voltage reference circuit generates temperature-compensated voltage(=1.2V) for the use as the internal reference voltage. Also, an external load current can be obtained from the power supply at VREF pin, up to 1mA maximum. Please connect a capacitor of 0.01uF between VREF pin and SGND for stability.

● Error Amplifier

Error Amplifier detects the output voltage of switching regulator and outputs the PWM control signal. Programmable by connecting feedback resistor and capacitor between the output of Error Amp(FB_1/2/3) and Inverting input(INV_1,2), it can provide stable phase compensation.

● Oscillation Circuit

The oscillation frequency can be defined by the external resistor connected between RT pin and GND. (See Typical Characteristics "the graph of oscillation frequency vs RT resistance".)

The relation between the oscillation frequency and the resistance of RT is approximately as follows.

$$\text{Oscillation Frequency (kHz)} \fallingdotseq \frac{2.35 \times 10^{4}}{RT(k\Omega)}$$

● VREG5, VREG5IN

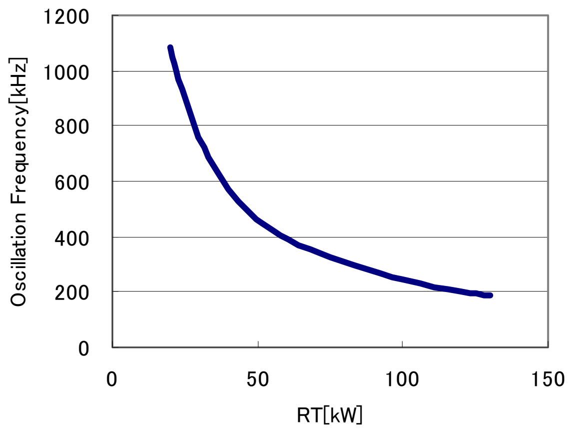
Built-in 5V local regulator for power supply of ch-1 and ch-2 output and for internal power supply. If the input voltage is lower than 5.5V, short-circuit the input voltage and VREG5 pin. If the input voltage is higher than 5.5V, leave the input voltage and VREG5 pin open.

● Amplifier for Vcom

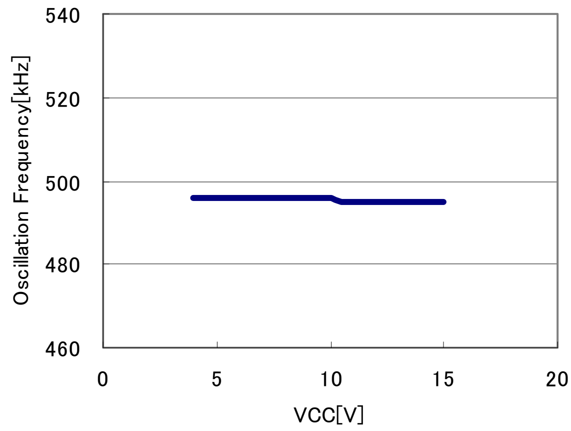
A buffer amplifier attained 4V/us slew rate. If output current is required, use the external bipolar transistor.

Typical Characteristics

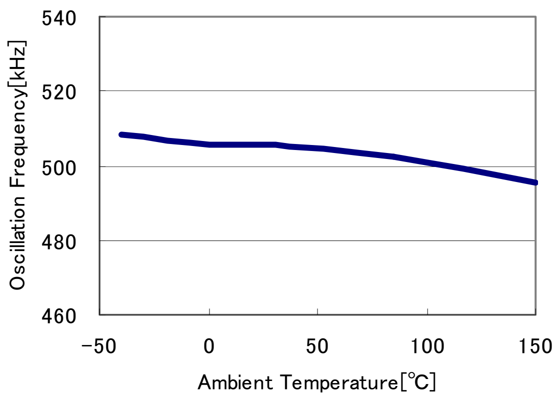
Oscillation Frequency vs RT Resistance



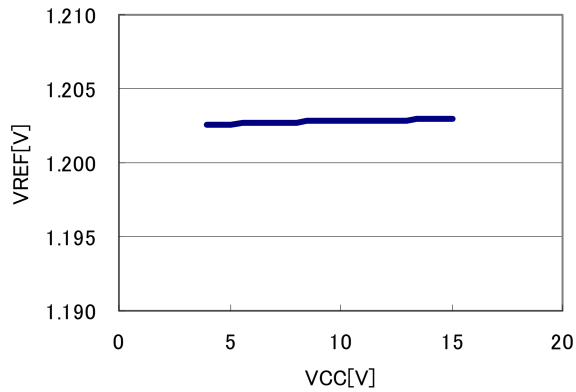
Oscillation Frequency vs VCC Voltage



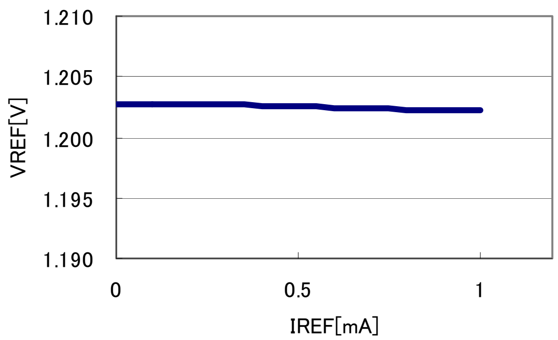
Oscillation Frequency vs Ambient Temperature



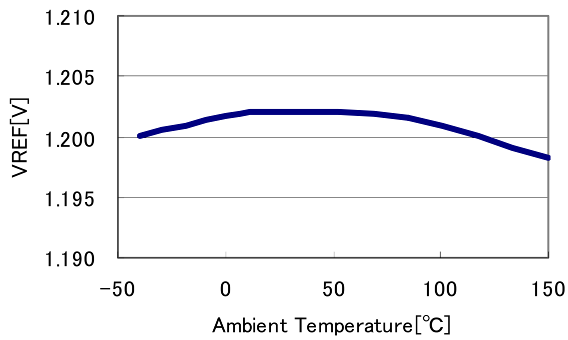
VREF vs VCC Voltage(Line Regulation)



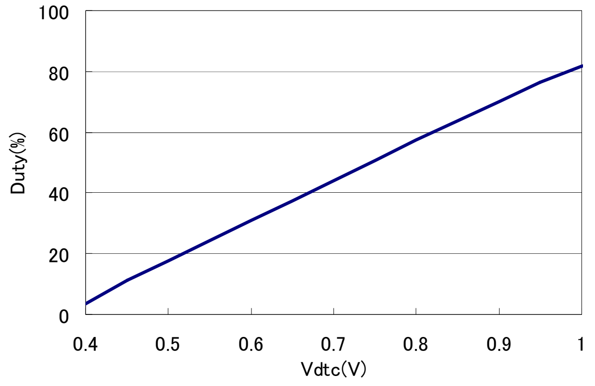
VREF vs IREF (Load Regulation)



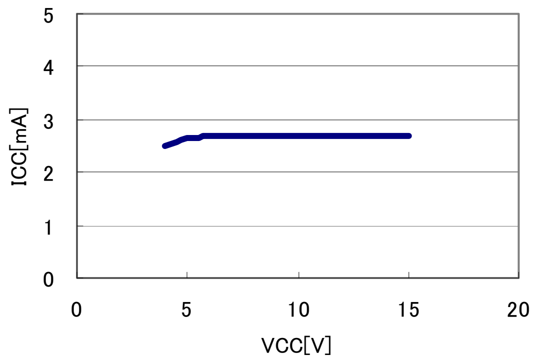
VREF vs Ambient Temperature



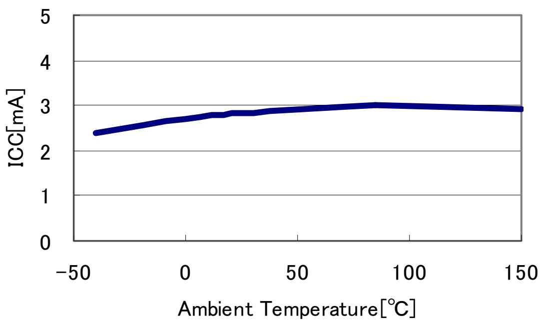
Maximum Duty Ratio vs DTC Voltage



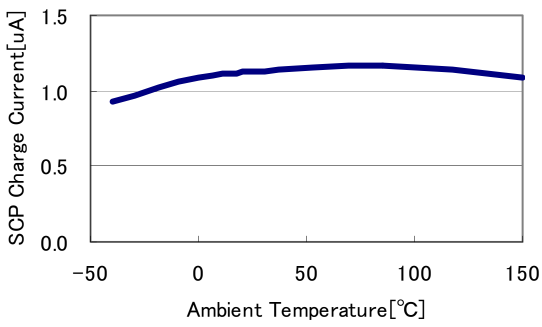
ICC(output swing Off) vs VCC



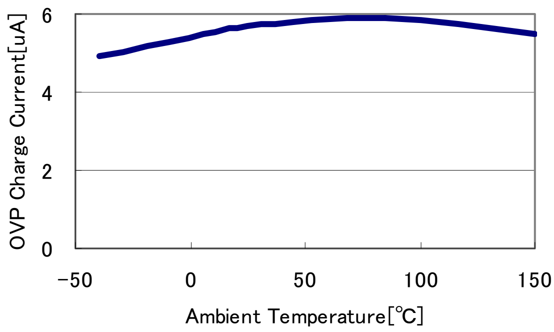
ICC(output swing Off) vs Ambient Temperature



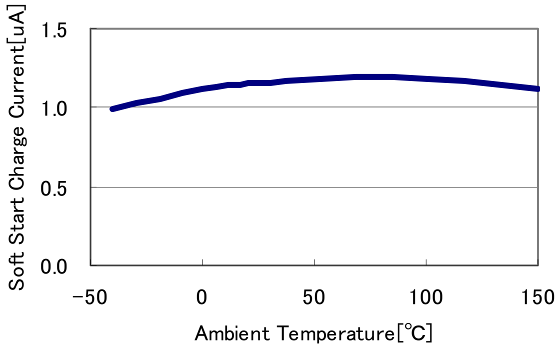
SCP Charge Current(UVP) vs Ambient Temperature



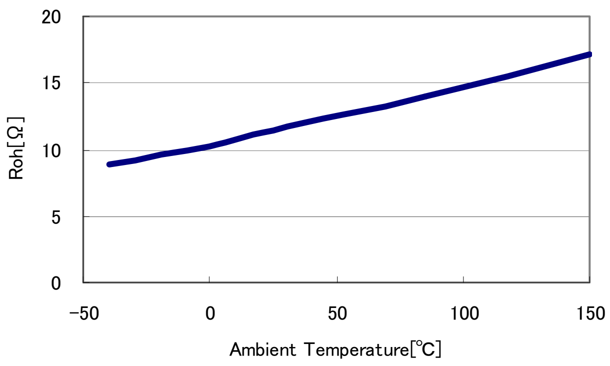
OVP Charge Current vs Ambient Temperature



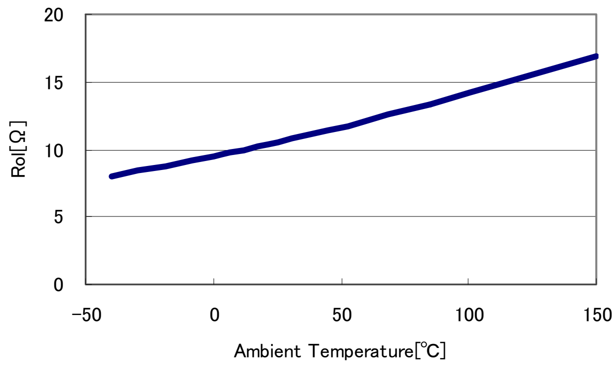
Soft Start Charge Current vs Ambient Temperature



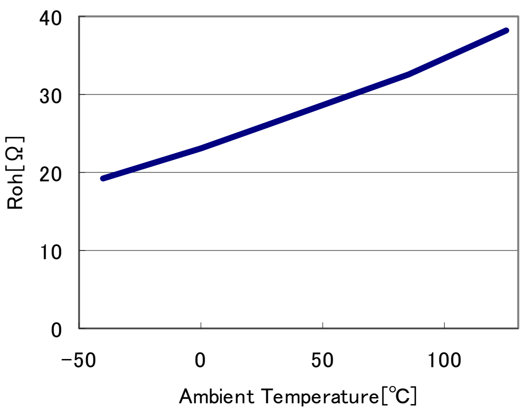
Output H level Output Resistance(Roh)
vs Ambient Temperature(VGH)



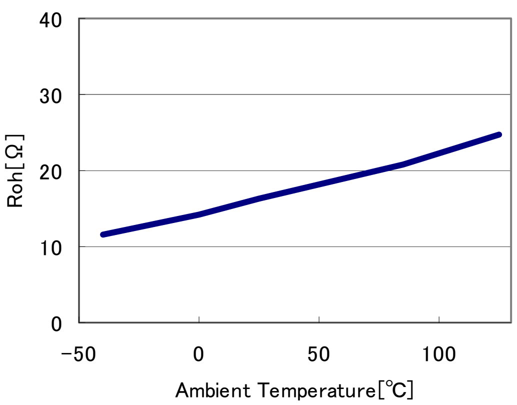
Output L level Output Resistance(Rol)
vs Ambient Temperature(VGH)



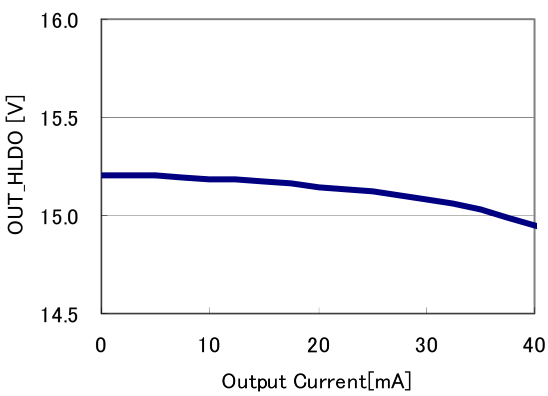
Output H level Output Resistance(Roh)
vs Ambient Temperature(VGJL)



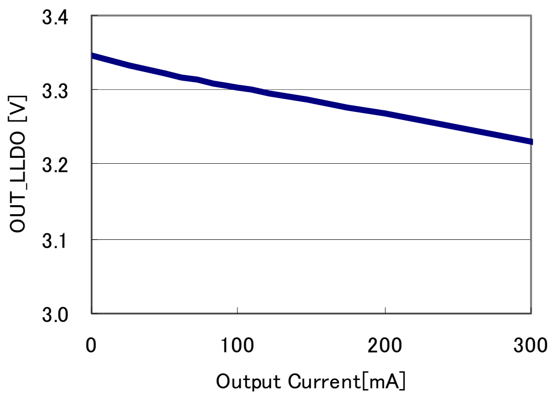
Output L level Output Resistance(Rol)
vs Ambient Temperature(VGL)



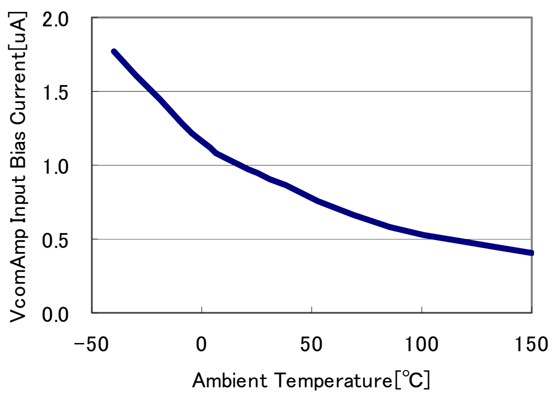
VO5 Load Regulation
(Input-Output Potential Difference : 0.4V)



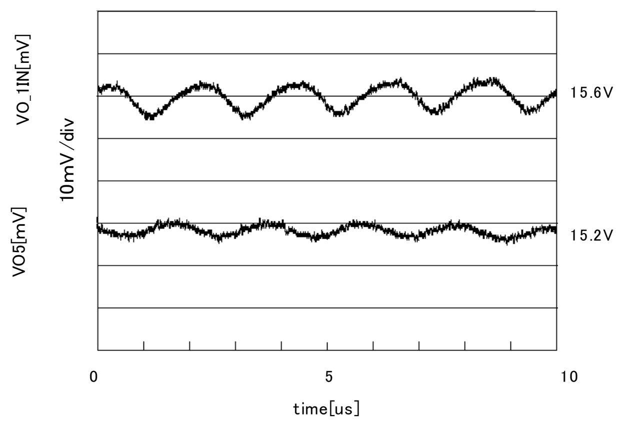
OUT_LLDO Load Regulation



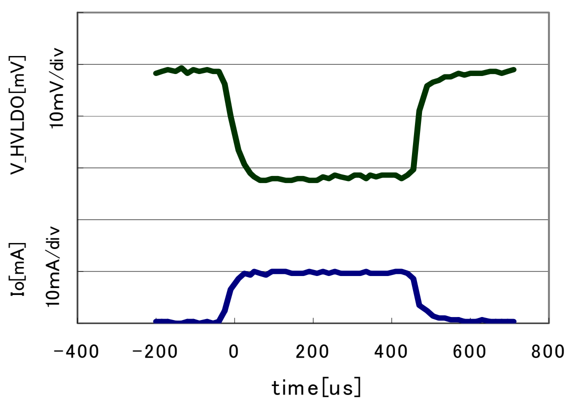
Vcom Amp Input Bias Current



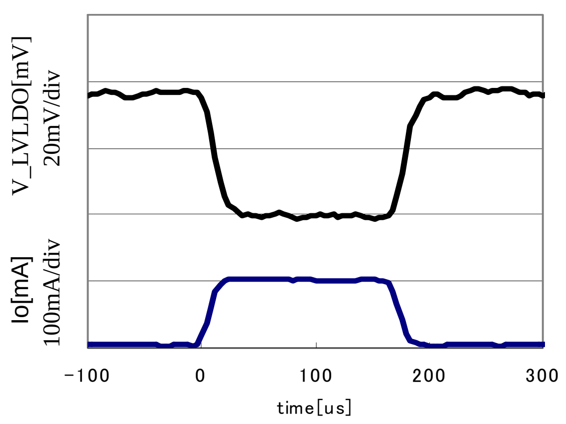
VO_1IN & OUT_HLDO Waveform



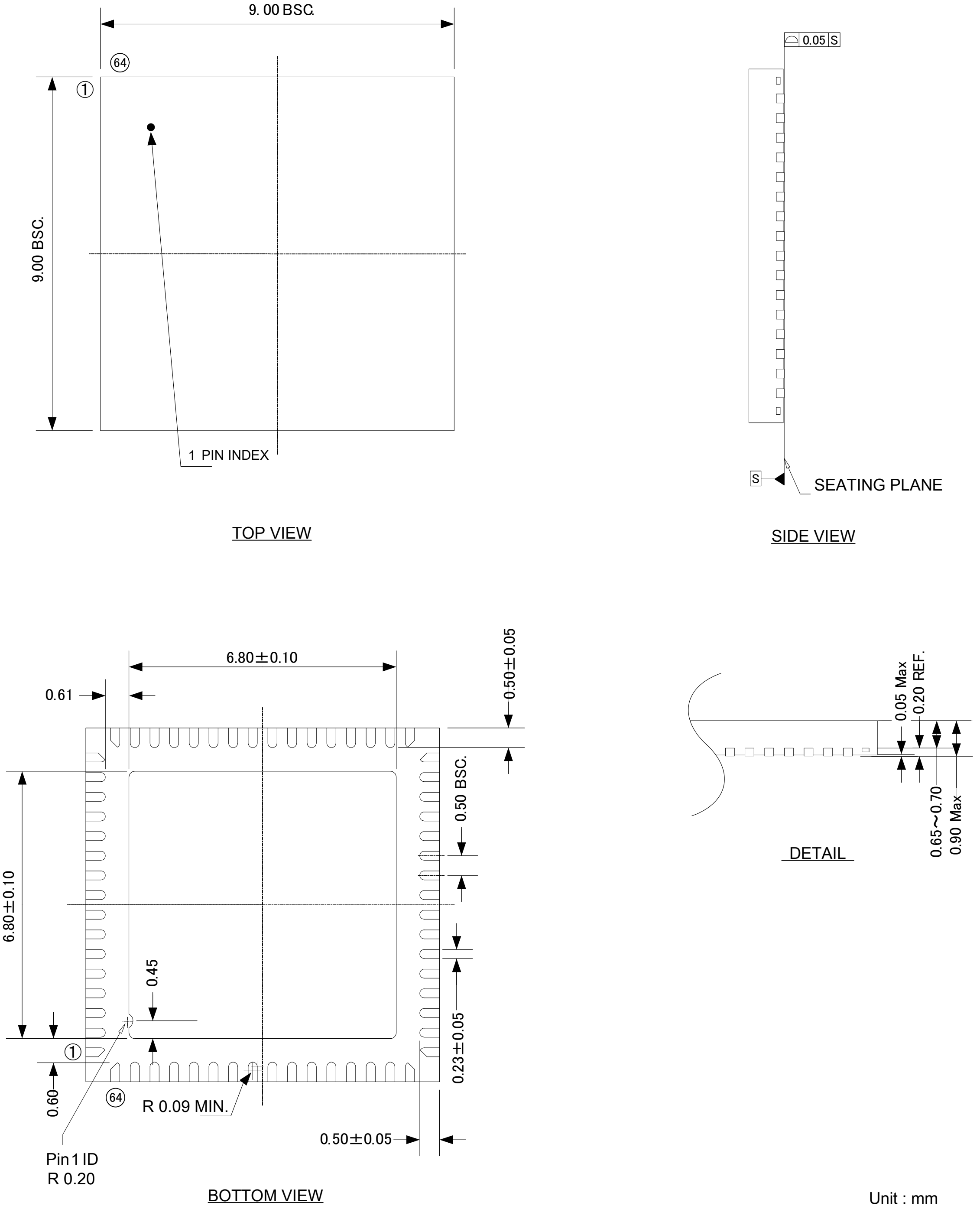
HV-Ido Response



LV-Ido Response

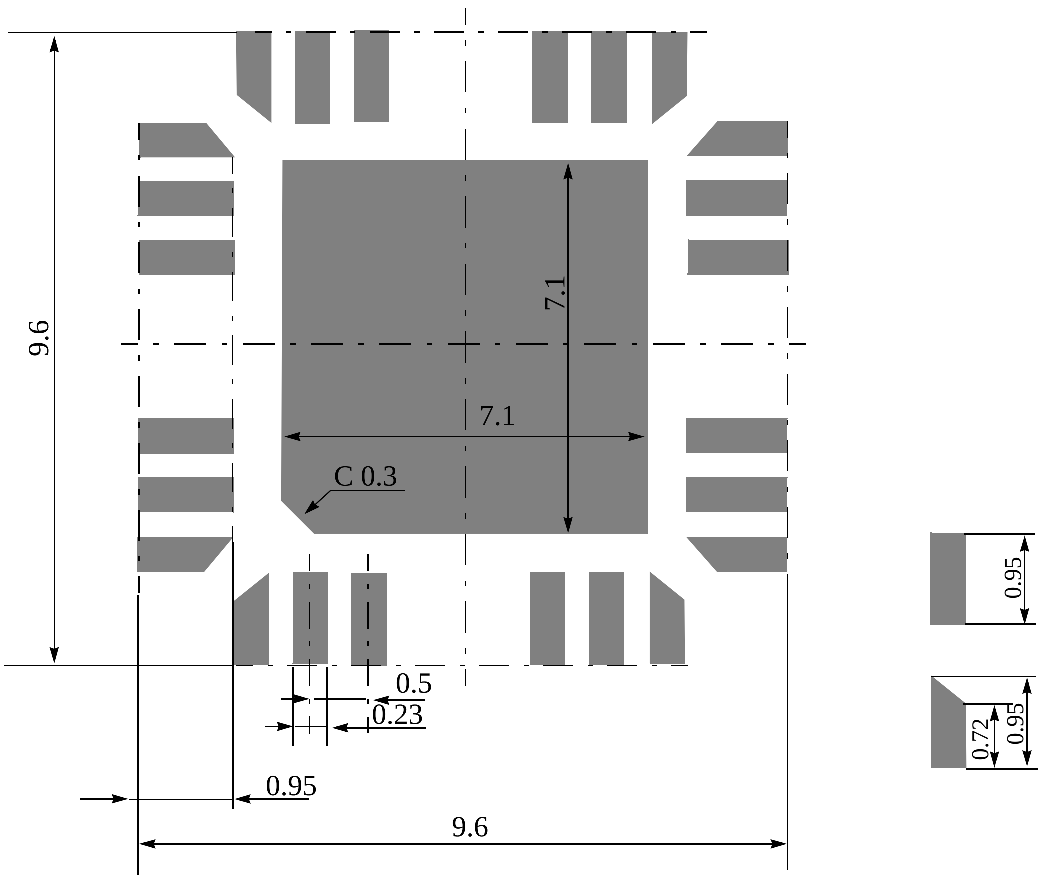


Package Outline



Recommended Land Pattern Design

Following shows the recommended land pattern design for QFN64PKG.
*This land pattern is for reference purpose only. Please examine carefully at deigning the board.



unit : mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
9. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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