THCV2911A

V-by-One® HS Redriver with Linear Equalization

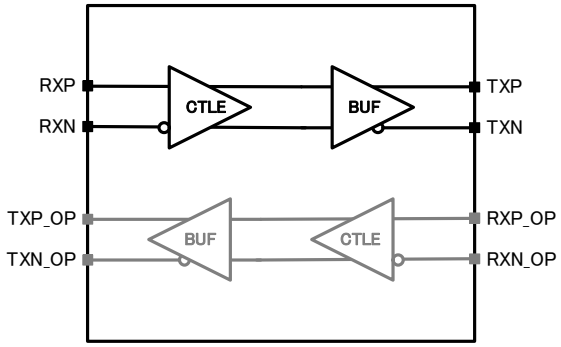
General Description

The THCV2911A is low power, high performance active redriver for V-by-One® HS with data rates up to 4Gbps. The THCV2911A pinout is configured as a forward and sub channels.

The THCV2911A features a powerful 15-stages continuous time linear equalizer (CTLE) to provide a boost of up to +9.3dB at 2GHz and open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the inter-connect mediums such as cable or FR-4.

The programmable settings can be applied via pin configurations which eliminates the needs for an external microprocessor and software driver.

Block Diagram



Features

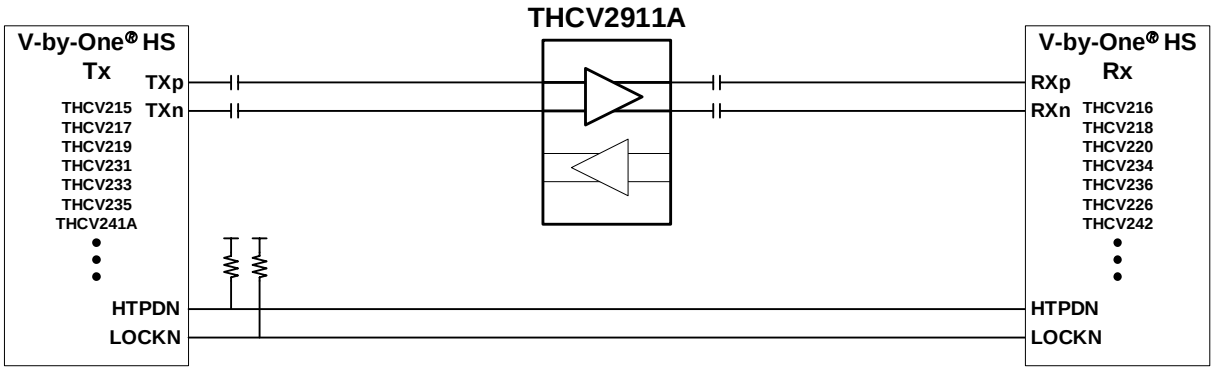
- Signal Conditioning with Linear Equalizer
- A forward and optional lane Redriver for up to 4 Gbps
- Linear Equalization up to +9.3dB@2GHz
- Adjustable Receiver Equalization and DC Gain
- Programmable via Pin Selection
- Flow-Thru Pinout
- Single Supply Voltage (3.3V)
- ESD HBM < ±4kV
- Package : QFN30 (2.5mm x 4.5mm)
- -40 to 105°C Operating Temperature

Applications

All V-by-One® HS applications for reach extension such as

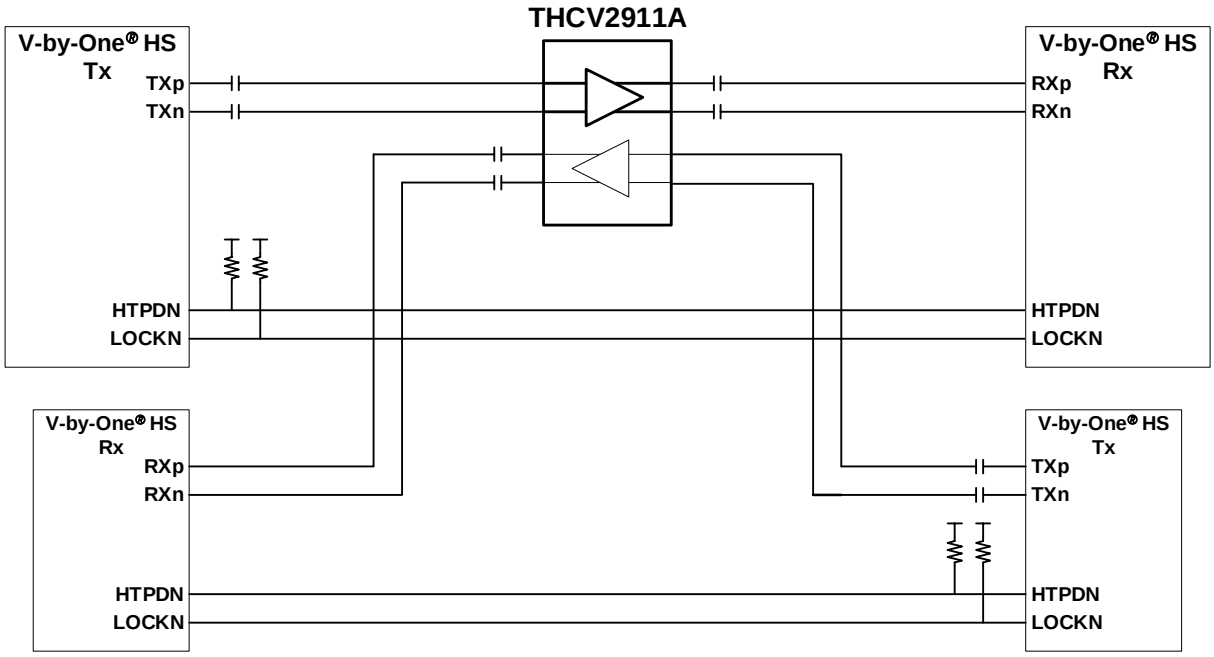
- Digital Signage
- Digital blackboard
- Multi-Function Printer
- Production Printer
- Medical imaging
- Machine vision
- Image Sensor
- Camera
- Active Cable

Typical Application

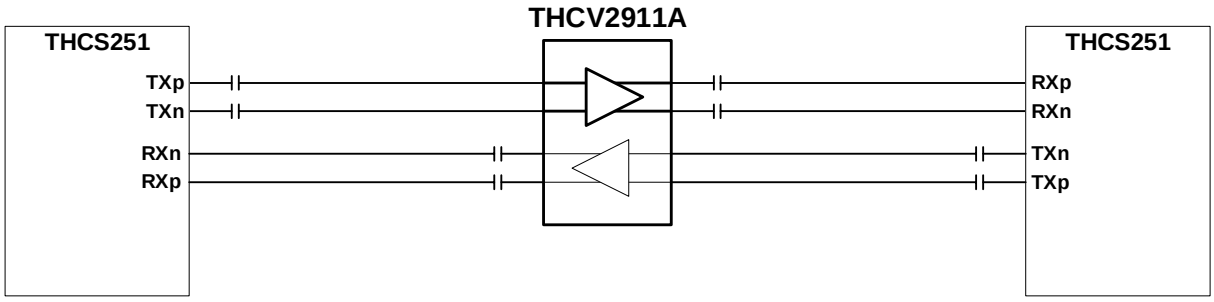


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Optional Application

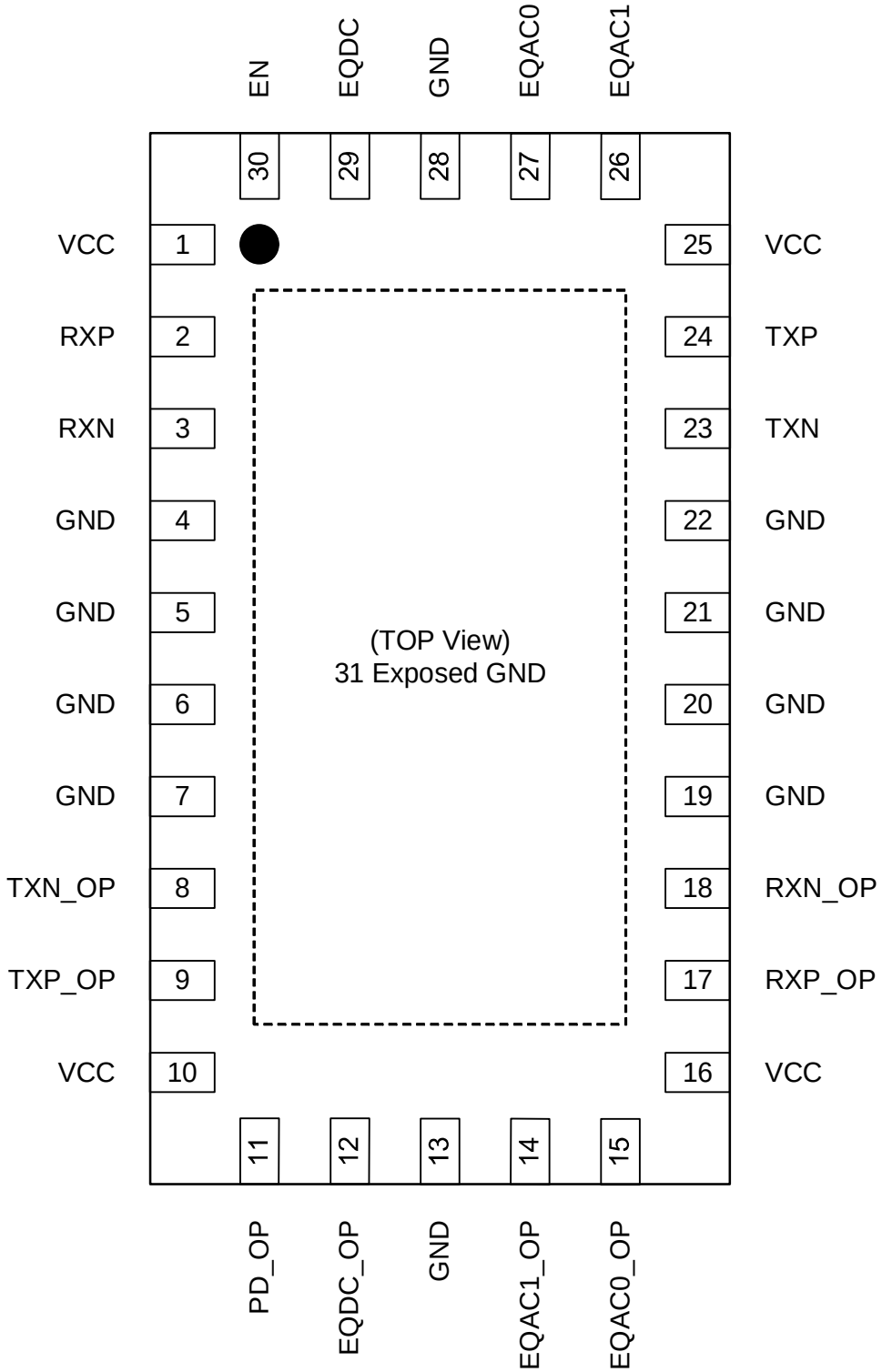


Optional Application with THCS251



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Pin Configuration



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Pin Description

Pin Name	Pin No	Type	Description
RXP	2	CI	High-Speed CML Signal Input of Main-Lane
RXN	3	CI	High-Speed CML Signal Input of Main-Lane
TXP	24	CO	High-Speed CML Signal Output of Main-Lane
TXN	23	CO	High-Speed CML Signal Output of Main-Lane
RXP_OP	17	CI	High-Speed CML Signal Input of Optional-Lane(OP)
RXN_OP	18	CI	High-Speed CML Signal Input of OP
TXP_OP	9	CO	High-Speed CML Signal Output of OP
TXN_OP	8	CO	High-Speed CML Signal Output of OP
EN	30	I	Channel Enable. With Internal 300kΩ Pull-up Resistor. 0 : Power Down 1 : Normal Operation
EQAC1	26	3LI (*1)	Main Rx Equalizer Peak Gain Setting This pin along with EQAC0 allows for up to 5 settings.
EQAC0	27	3LI (*1)	Main Rx Equalizer Peak Gain Setting This pin along with EQAC1 allows for up to 5 settings.
EQAC1_OP	14	3LI (*1)	OP Rx Equalizer Peak Gain Setting This pin along with EQAC0_OP allows for up to 5 settings.
EQAC0_OP	15	3LI (*1)	OP Rx Equalizer Peak Gain Setting This pin along with EQAC1_OP allows for up to 5 settings.
EQDC	29	3LI (*1)	Main Equalizer DC Gain Setting
EQDC_OP	12	3LI (*1)	OP Equalizer DC Gain Setting
PD_OP	11	3LI (*1)	Chip Operation Mode Select, if EN=1 F : OP Enable, 1 : OP Disable,
VCC	1, 10, 16, 25	PWR	Power Supply Pin for On-chip Regulator.
GND	4,5,6,7,13, 19,20,21, 22,28,31	GND	Ground. Must be tied to the PCB ground plane through an array of vias. Pin#31 is exposed pad ground.

CI: CML Input Buffer, CO: CML Output Buffer
I: LVCMOS Input Buffer, 3LI: 3-Level LVCMOS Input Buffer,
PWR: Power Supply, GND: Ground

*1 : 3-Level Input Buffer. With internal 180kΩ pull-up resistor and 300kΩ pull-down resistor.

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Operation Mode Settings

Table 1. Operation Mode Settings

Pin Settings		Operation Mode
EN	PD_OP	
1	0(*1)	Reserved
	F(*2)	OP Enable
	1(*3)	OP Disable
0	Ignore	Chip Power Down.

*1 Tie 0Ω to GND
*2 Leave pin Open
*3 Tie 0Ω to VCC

Linear Equalizer Settings

Table 2. Linear Equalizer Settings

EQAC1(_OP)	EQAC0(_OP)	EQDC(_OP)	Equalizer Settings (dB)				
			Up to 0.2GHz	@0.5GHz (1Gbps)	@1.0GHz (2Gbps)	@1.5GHz (3Gbps)	@2.0GHz (4Gbps)
0	*	*	Reserved				
F	0	0	-1.5	-0.8	0.5	1.9	3.0
F	F			-0.7	1.0	2.7	4.1
F	1			Reserved			
1	0			-0.6	1.4	3.3	5.0
1	F			-0.4	1.9	4.2	6.1
1	1			-0.2	2.3	4.7	6.7
F	0	F	1.2	1.7	2.7	3.6	4.3
F	F			1.8	3.2	4.2	5.1
F	1			Reserved			
1	0			1.9	3.3	4.6	5.8
1	F			2.0	3.6	5.3	6.7
1	1			2.1	3.9	5.7	7.2
F	0	1	4.5	5.2	6.3	7.0	7.4
F	F			5.2	6.5	7.4	7.9
F	1			Reserved			
1	0			5.3	6.6	7.6	8.3
1	F			5.3	6.8	8.0	8.9
1	1			5.3	7.0	8.3	9.3

Average of all channels in typical condition

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Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter		Min	Typ	Max	Unit
Supply Voltage(VCC)		-0.3	-	4.0	V
LVCMOS Input/Output Voltage		-0.3	-	VCC+0.3	V
3-Level LVCMOS Input Voltage		-0.3	-	VCC+0.3	V
CML Receiver Input Voltage		-0.3	-	VCC+0.3	V
CML Transmitter Output Voltage		-0.3	-	VCC+0.3	V
ESD Rating	HBM	-	-	±4	kV
	CDM	-	-	±1000	V
Storage Temperature		-55	-	125	°C
Junction Temperature		-	-	125	°C
Reflow Peak Temperature/Time		-	-	260/10	°C/sec

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	3.0	3.3	3.6	V
Supply Ramp Requirement	0.1	-	50	ms
Operating Temperature	-40	-	105 85(*1)	°C

(*1) PD_OP=F

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Equivalent CML Input Schematic Diagram

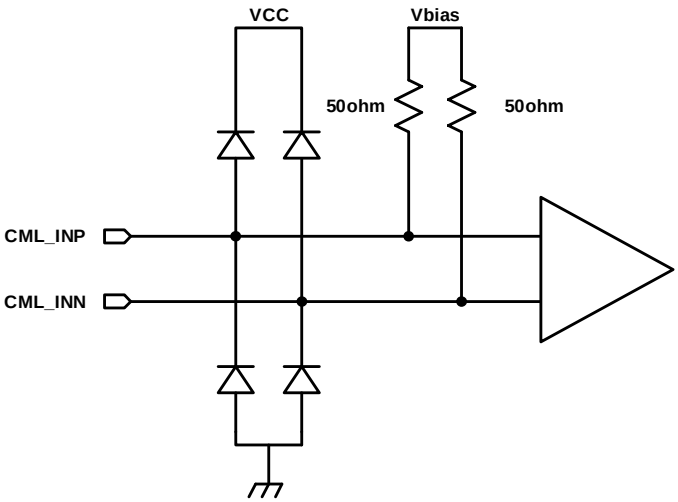


Figure 1. CML Input Schematic Diagram

Equivalent CML Output Schematic Diagram

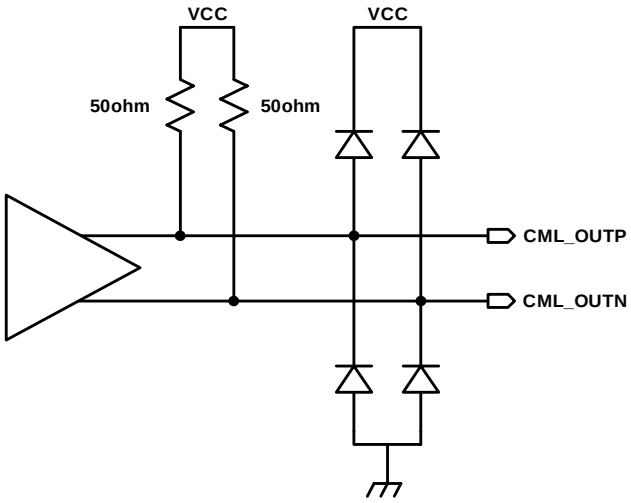


Figure 2. CML Output Schematic Diagram

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Equivalent LVCMOS Input Schematic Diagram

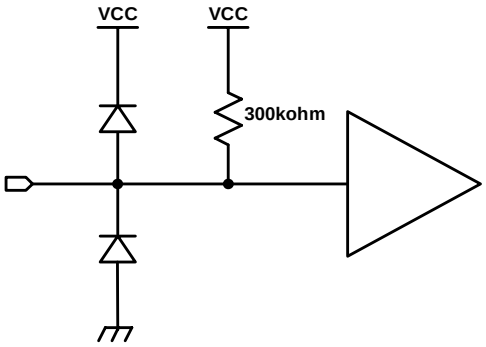


Figure 3. LVCMOS Input Schematics Diagram

Equivalent 3-Level LVCMOS Input Schematic Diagram

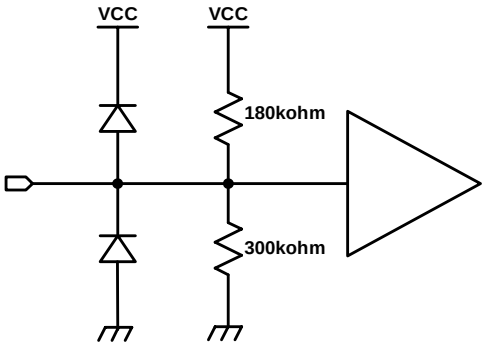


Figure 4. 3-Level Input Schematics Diagram

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Electrical Specification

Supply Current

Table 5. Supply Current

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCW	Active Mode Supply Current	PD_OP=1	-	58	84	mA
		PD_OP=F	-	84	106	mA
ICCS	Power Down Supply Current	-	-	120	180	uA

LVCMOS DC Specification

Table 6. LVCMOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	-	2.0	-	VCC	V
VIL	Low Level Input Voltage	-	0	-	0.7	V

3-Level LVCMOS DC Specification

Table 7. 3-Level LVCMOS DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{THL}	Low Level Input Voltage	0(*1)	0	-	VCC*0.25 - 0.3	V
V_{THF}	F-Level Input Voltage	F(*2)	VCC*0.5 + 0.3	-	VCC*0.75 - 0.3	V
V_{THH}	High Level Input Voltage	1(*3)	VCC*0.75 + 0.3	-	VCC	V
I_{IH_3L}	High level Input Leak Current	VIN=VCC	-100	-	100	uA
I_{IL_3L}	Low Level Input Leak Current	VIN=GND	-100	-	100	uA

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Receiver DC Specification

Table 8. Receiver DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	EN=0,RXP/N=VCC	-10	-	10	uA
IRIL	CML Input Leak Current Low	EN=0,RXP/N=GND	-10	-	10	uA
RRIN	CML Differential Input Resistance	-	-	100	-	Ω

Transmitter DC Specifications

Table 9. Transmitter DC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VTOC	CML Common mode Output Voltage	-	-	VCC-0.75	-	V
ITOH	CML Output Leak Current High	EN=0	-	-	50	uA

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AC Specifications

Table 10. AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{EN}	Power On to EN High Delay	-	0	-	-	ns
T_{ACTIVE}	EN High to Active Delay	-	-	-	200	us
$T_{PROPAGATION}$	Differential Propagation Delay	-	-	150	-	ps
$\Delta T_{PROPAGATION}$	Delta Propagation Delay	-	-	-	40	ps

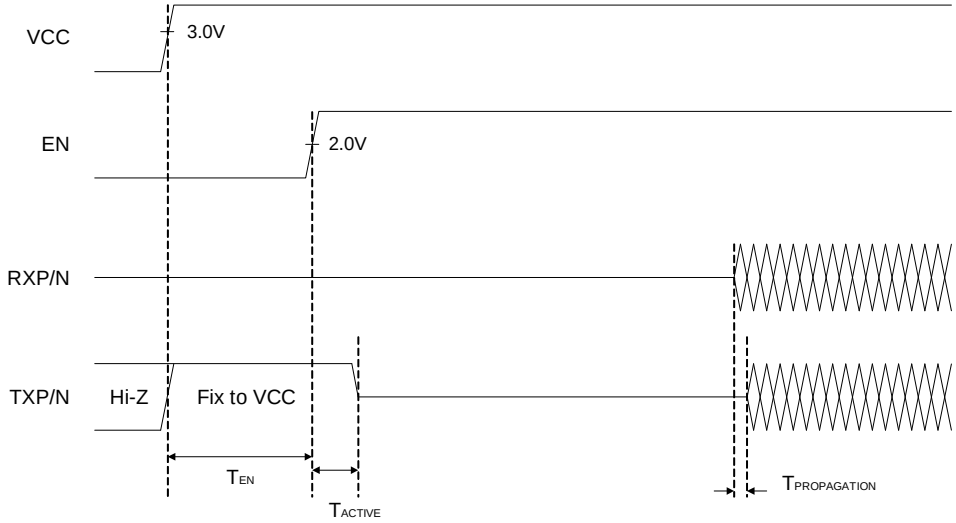
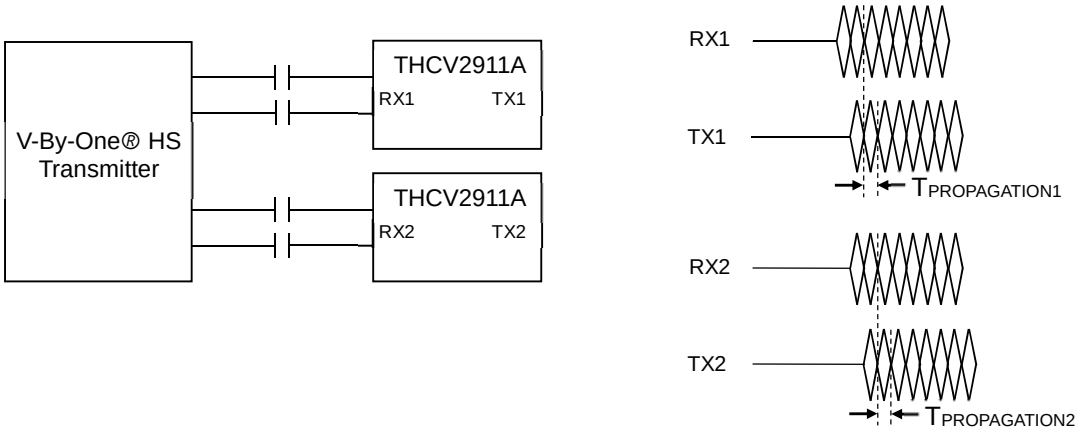


Figure 5. Power on Sequence



$\Delta T_{PROPAGATION} = | T_{PROPAGATION1} - T_{PROPAGATION2} |$

Figure 6. CML Propagation Delay Timing

Table 11. Transmitter AC Specification

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tTRF	Tx Rise/Fall Time	20% to 80 %	50	-	150	ps

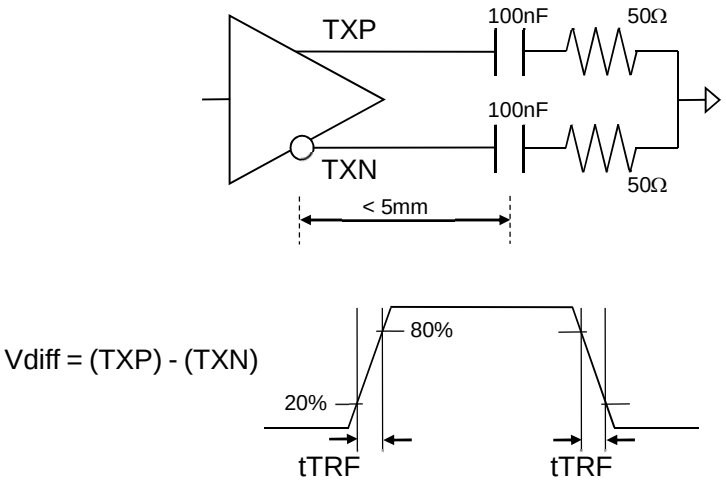
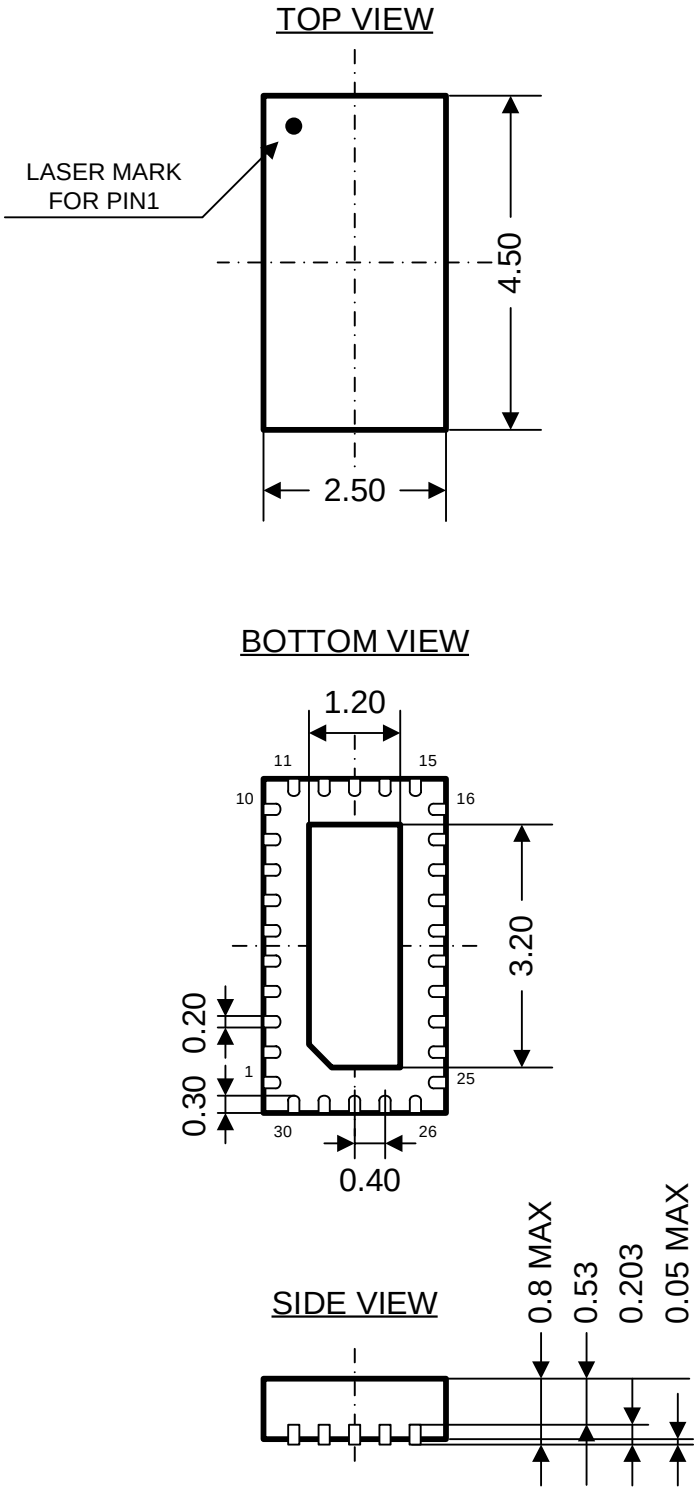


Figure 7. CML Output Switching Timing and Test Circuit

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Package



Unit: mm

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