THCV226

V-by-One® HS High-speed Video Data Receiver

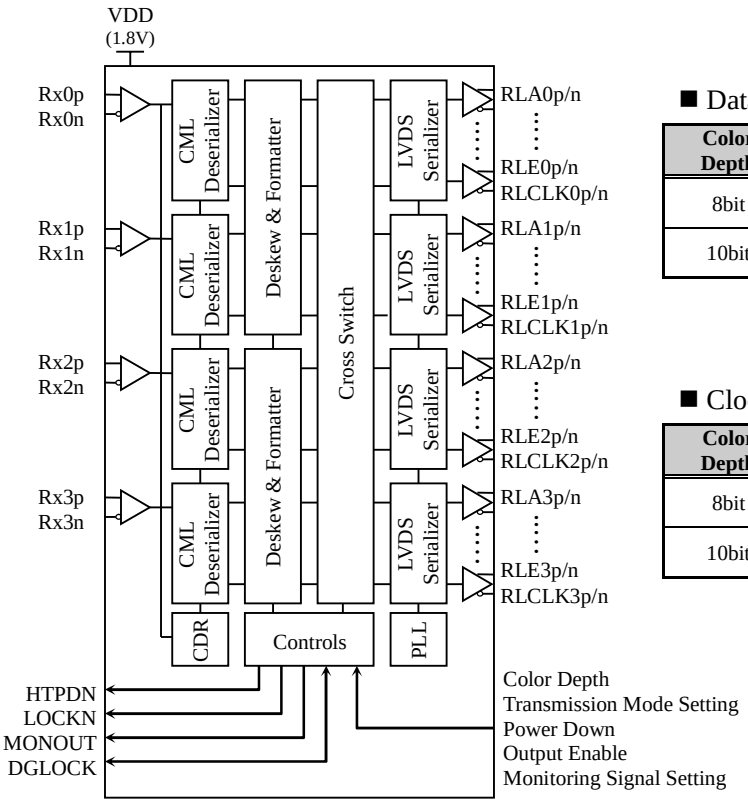
General Description

THCV226 is designed to support video data transmission between the host and display. This chip can receive 32bit video data and 3bit control data via four differential pairs of V-by-One® HS lanes. This chip in TQFP package supports the video data transmission up to 1080p/10b/120Hz. The maximum serial data rate is 3.4Gbps/lane.

Features

- Normal / High-speed LVDS output selectable
- 1.8V single power supply
- Color depth selectable: 8/10 bits per colors
- Crossing / Distribution mode selectable
- Monitoring signal function
- 1.8V LVCMOS I/O interface
- Package: 128pin 0.4mm-pitch TQFP (16mm x 16mm)
- AC coupling for CML inputs
- CDR requires no external frequency reference
- Supports Spread Spectrum Clocking tolerance with up to 30kHz/±0.5%(center spread)
- V-by-One® HS standard compliant
- PLL requires no external components
- Power down / Output enable mode
- Compliant with RoHS and REACH

Block Diagram



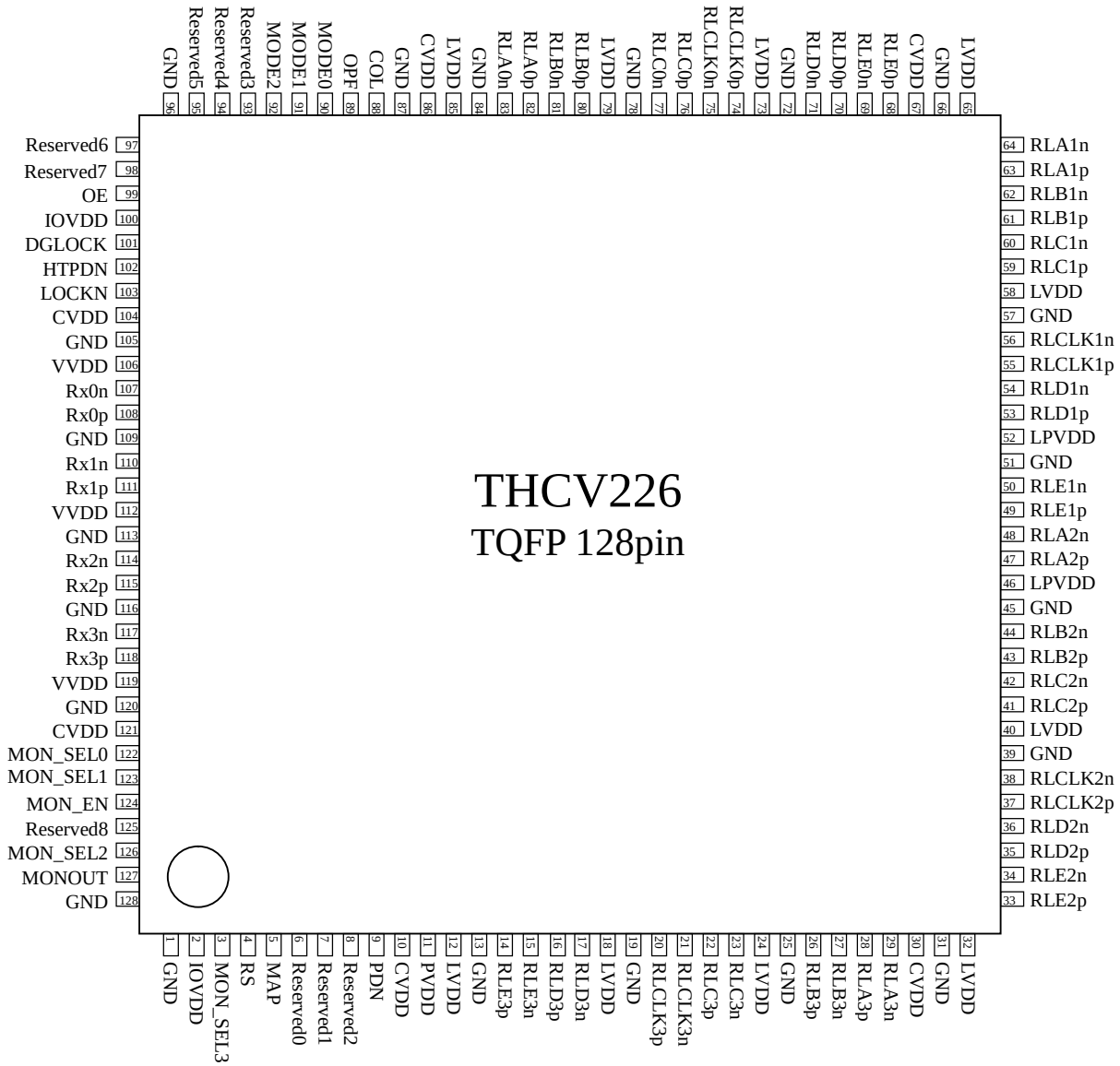
■ Data Transmission Rate of CML Input

Color Depth	Normal Speed LVDS Mode	High-Speed LVDS Mode
8bit	1.2 to 2.7Gbps	1.2 to 2.36Gbps
10bit	1.6 to 3.4Gbps	1.6 to 3.14Gbps

■ Clock Frequency of LVDS Output

Color Depth	Normal Speed LVDS Mode	High-Speed LVDS Mode
8bit	40 to 90MHz	80 to 157MHz
10bit	40 to 85MHz	80 to 157MHz

PIN Configuration



PIN Description

PIN Name	PIN No	Type	Description
Rx0n , Rx0p	107, 108	CI	CML Data Input
Rx1n , Rx1p	110, 111	CI	CML Data Input
Rx2n , Rx2p	114, 115	CI	CML Data Input
Rx3n , Rx3p	117, 118	CI	CML Data Input
RLA0n , RLA0p	83, 82	LO	LVDS Data Output
RLB0n , RLB0p	81, 80	LO	LVDS Data Output
RLC0n , RLC0p	77, 76	LO	LVDS Data Output
RLCLK0n , RLCLK0p	75, 74	LO	LVDS Data Output
RLD0n , RLD0p	71, 70	LO	LVDS Data Output
RLE0n , RLE0p	69, 68	LO	LVDS Data Output
RLA1n , RLA1p	64, 63	LO	LVDS Data Output
RLB1n , RLB1p	62, 61	LO	LVDS Data Output
RLC1n , RLC1p	60, 59	LO	LVDS Data Output
RLCLK1n , RLCLK1p	56, 55	LO	LVDS Data Output
RLD1n , RLD1p	54, 53	LO	LVDS Data Output
RLE1n , RLE1p	50, 49	LO	LVDS Data Output
RLA2n , RLA2p	48, 47	LO	LVDS Data Output
RLB2n , RLB2p	44, 43	LO	LVDS Data Output
RLC2n , RLC2p	42, 41	LO	LVDS Data Output
RLCLK2n , RLCLK2p	38, 37	LO	LVDS Data Output
RLD2n , RLD2p	36, 35	LO	LVDS Data Output
RLE2n , RLE2p	34, 33	LO	LVDS Data Output
RLA3n , RLA3p	29, 28	LO	LVDS Data Output
RLB3n , RLB3p	27, 26	LO	LVDS Data Output
RLC3n , RLC3p	23, 22	LO	LVDS Data Output
RLCLK3n , RLCLK3p	21, 20	LO	LVDS Data Output
RLD3n , RLD3p	17, 16	LO	LVDS Data Output
RLE3n , RLE3p	15, 14	LO	LVDS Data Output
DGLOCK	101	BI	Connect all DGLOCK pins in multiple-chip configuration. Must be left OPEN for single-chip configuration
HTPDN	102	OD	Hot plug detect output Must be connected to Tx HTPDN with a 10KΩ pull-up resistor
LOCKN	103	OD	Lock detect output Must be connected to Tx LOCKN with a 10KΩ pull-up resistor
COL	88	I	Color depth select H : 10bit mode L : 8bit mode
OPF	89	I	Output Pattern at CDR Fail Condition (LOCKN=L) H : LVDS output Low data L : LVDS output Hi-Z data
MODE2,1,0	92,91,90	I	Input / Output mode select
OE	99	I	LVDS Output Enable H : Normal Operation L : Output Disable

PIN Description (Continued)

PIN Name	PIN No	Type	Description
MON_SEL1,0	123, 122	I	Monitoring Input Lane select (See Table 8)
MON_SEL3,2	3, 126	I	Monitoring Input Signal select (See Table 8)
MON_EN	124	I	Monitoring mode enable H : Enable L : Disable
RS	4	I	LVDS swing level select H : Normal swing (350mV) L : Reduced swing (200mV)
MAP	5	I	LVDS output format select H : JEIDA format L : VESA format
PDN	9	I	Power down H : Normal operation L : Power down operation
MONOUT	127	O	Monitoring signal output
Reserved 0,1,2,3,4,5,8	6, 7, 8, 93, 94, 95, 125	I	Must be tied to GND
Reserved 6,7	97, 98	O	Must be open
CVDD	10, 30, 67, 86, 104, 121	PWR	1.8V power supply for Logic block
VVDD	106, 112, 119	PWR	1.8V power supply for V-by-One® HS block
LVDD	12, 18, 24, 32, 40, 58, 65, 73, 79, 85	PWR	1.8V power supply for LVDS block
PVDD	11	PWR	1.8V power supply for PLL block
LPVDD	46, 52	PWR	1.8V power supply for LVDS analog block
IOVDD	2, 100,	PWR	1.8V power supply for LVCMOS I/O buffer
GND	1, 13, 19, 25, 31, 39, 45, 51, 57, 66, 72, 78, 84, 87, 96, 105, 109, 113, 116, 120, 128	GND	Ground

CI : CML Input buffer , LO : LVDS Output buffer , BI : LVCMOS Bi-directional buffer
I : LVCMOS Input buffer , O : LVCMOS Output buffer , OD : Open Drain buffer
PWR : 1.8V Power supply , GND : Ground

Functional Description

Functional Overview

With V-by-One® HS's proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV226 enables the transmission of 8 or 10-bit video data, 2-bit synchronizing control data of HSYNC, VSYNC, and Data Enable (DE), by a pair cable with minimal external components.

THCV226 automatically extracts the clock from the incoming data streams and converts the serial data into video data with DE being high or synchronizing control data with DE being low, recognizing which type of serial data is being sent by the transmitter. Also, THCV226 outputs the recovered data in the LVDS data format.

THCV226 can operate for a wide range of a serial bit rate from 1.2Gbps to 3.4Gbps. It is unnecessary to use any external frequency reference, such as a crystal oscillator.

Data Enable Requirement (DE)

There are some requirements for DE signal as described in Figure1 and Figure2.
If DE=Low and MODE0=0, control data of same cycle and particular assigned data bit 'CTL' except the first and last pixel are transmitted. If DE=Low and MODE0=1, control data of same cycle and particular assigned data bit 'CTL' except the first 2cycle and last 2pixel are transmitted. Otherwise video data is transmitted during DE=High. The length of DE being low and high must be at least 8 clock cycles long, as described in Figure15 and Switching Characteristics. DE must be toggled as High -> Low -> High at regular interval. The length of particular DE cycle must be same at all lane.

CTL Bit Transmission

There is particular assigned data bit 'CTL' which can be transmitted at blanking period except the first and the last pixel on DE=Low.

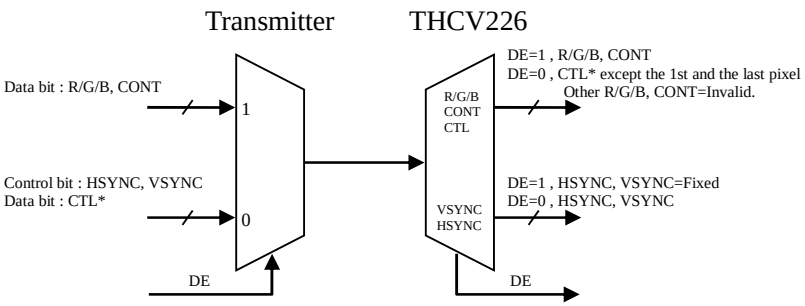


Figure 1. Conceptual Diagram of Basic Operation of Chipset

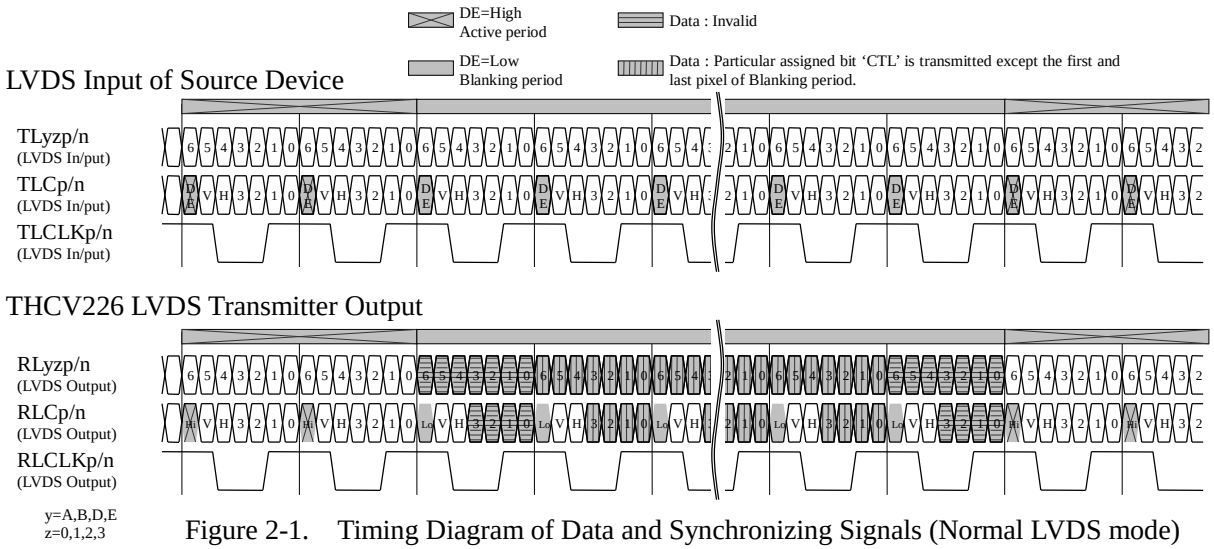


Figure 2-1. Timing Diagram of Data and Synchronizing Signals (Normal LVDS mode)

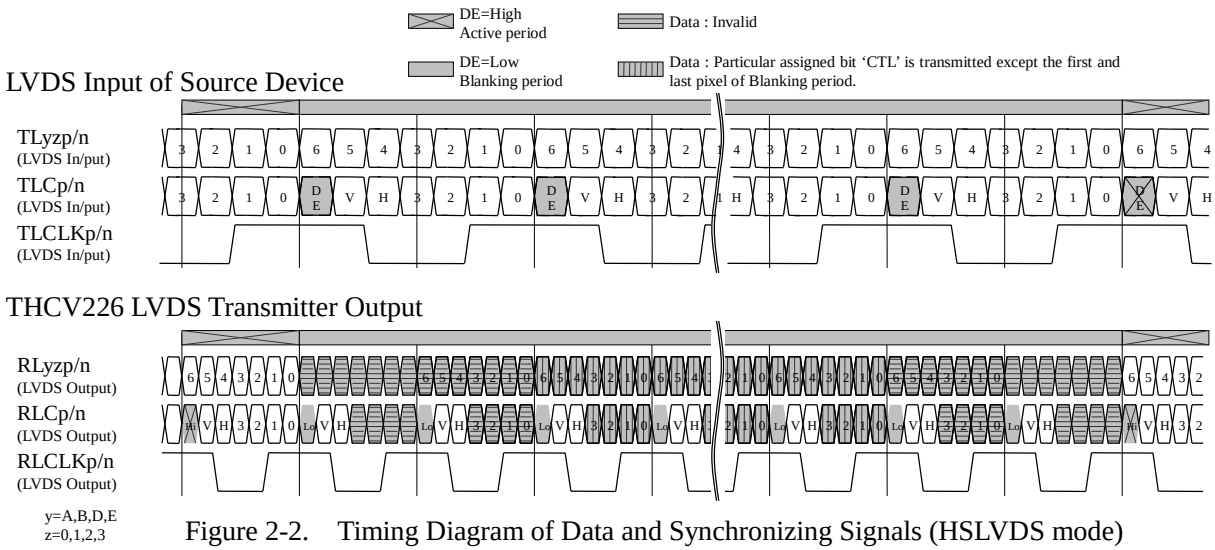


Figure 2-2. Timing Diagram of Data and Synchronizing Signals (HSLVDS mode)

Color Depth Mode Function

Table 1. Color Depth Mode Select

COL	Operation Mode
1	10-bit R/G/B data (4byte mode for V-by-One® HS Standard)
0	8-bit R/G/B data (3byte mode for V-by-One® HS Standard)

Transmission Mode Select

Table 2. Transmission Mode Select

MODE 2, 1, 0	COL	V-by-One HS	LVDS	Operation Mode
111	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Distribution mode2
	0	40 – 78.5MHz	80 – 157MHz	
110	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Distribution mode2
	0	40 – 90MHz	40 – 90MHz	
101	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Distribution mode1
	0	40 – 78.5MHz	80 – 157MHz	
100	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Distribution mode1
	0	40 – 90MHz	40 – 90MHz	
011	1	40 – 78.5MHz	80 – 157MHz	HSLVDS / Crossing Mode
	0	40 – 78.5MHz	80 – 157MHz	
010	1	40 – 85MHz	40 – 85MHz	Normal LVDS / Crossing mode
	0	40 – 90MHz	40 – 90MHz	
001	1	40 – 78.5MHz	80 – 157MHz	HSLVDS mode
	0	40 – 78.5MHz	80 – 157MHz	
000	1	40 – 85MHz	40 – 85MHz	Normal LVDS mode
	0	40 – 90MHz	40 – 90MHz	

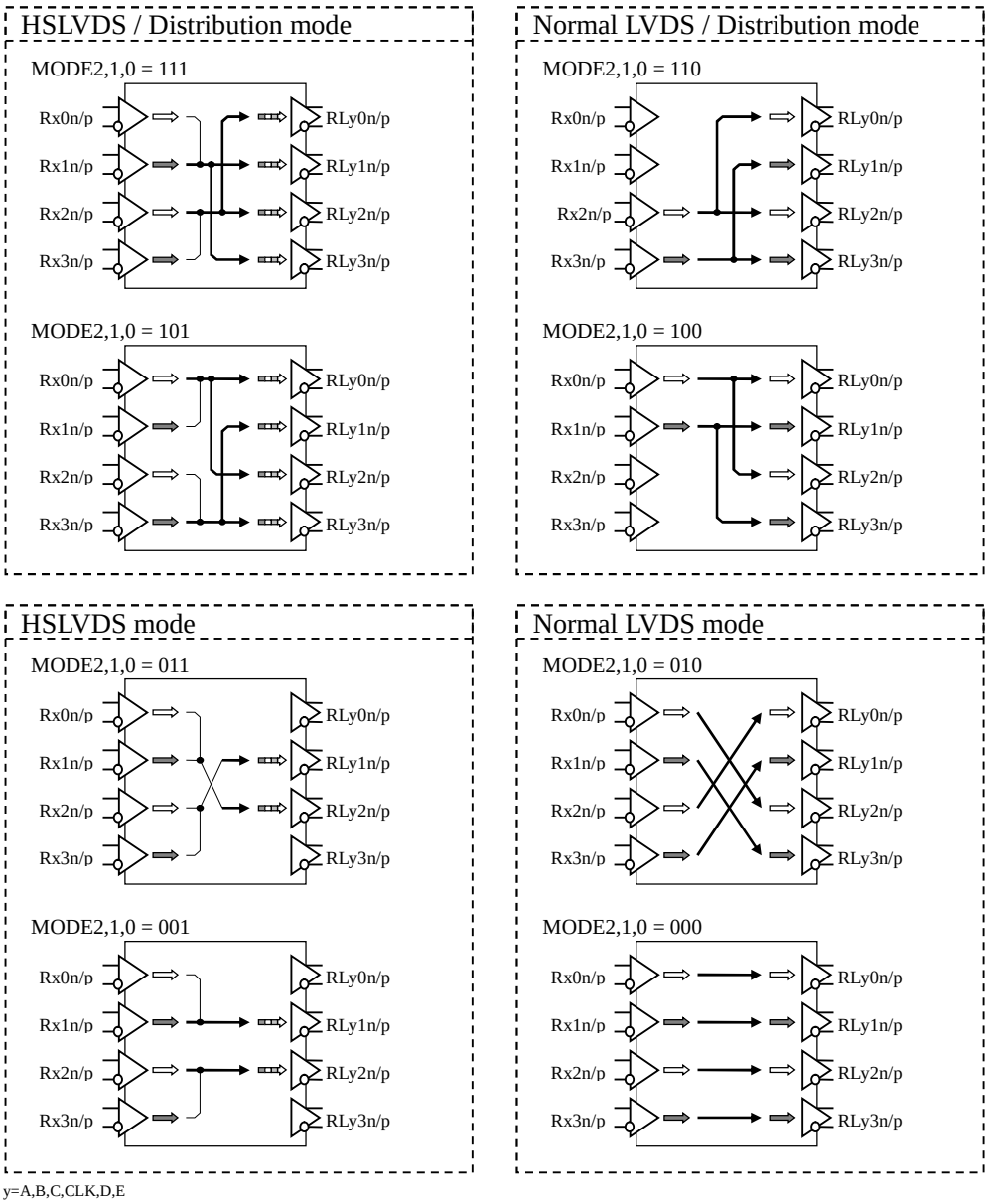


Figure 3. Transmission Mode Select Diagram

Power Down Mode

Table 3. Power Down Mode

PDN	Operation
1	Normal operation
0	Power down operation

Hot-plug and Lock Detect Function

HTPDN and LOCKN are both open drain outputs from THCV226. Pull-up resistors must be placed at V-by-One® HS transmitter side. See Figure.4 and 5.

If THCV226 is not active (power down mode (PDN=0) or powered off), HTPDN is open. Otherwise, HTPDN is pulled down by THCV226.

HTPDN at V-by-One® HS transmitter side is High when THCV226 is not active or the receiver board is not connected. Then V-by-One® HS transmitter side enters into the power down mode. When HTPDN transits from High to Low, V-by-One® HS transmitter starts up and transmits training pattern for link training.

LOCKN indicates whether THCV226 is in CDR state or not. If THCV226 is in the CDR unlock state, LOCKN is open. Otherwise (in the CDR lock state), it is pulled down by THCV226.

V-by-One® HS transmitter side keeps transmitting training pattern until LOCKN transition to Low. After training is done, THCV226 sinks current, and LOCKN turns to Low. Then V-by-One® HS transmitter side starts transmitting normal video pattern.

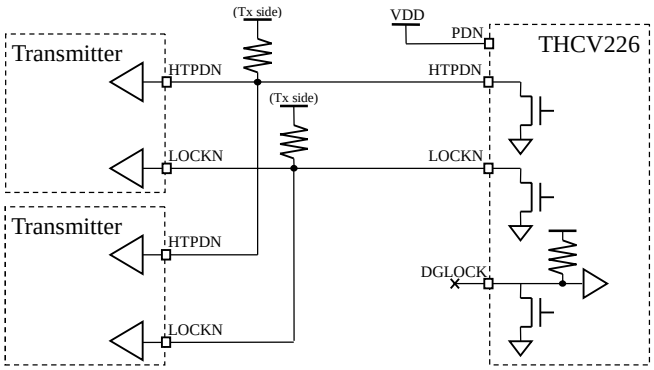


Figure 4. HTPDN and LOCKN Scheme

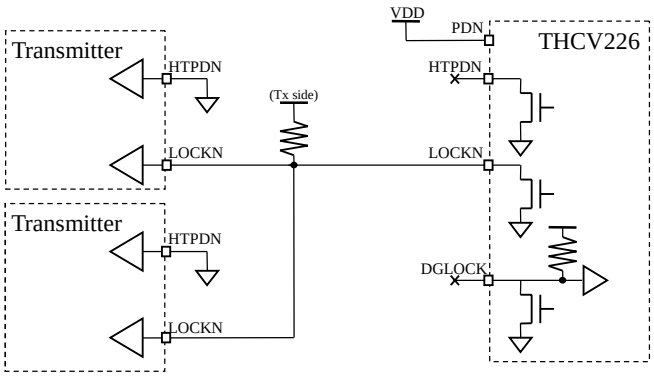


Figure 5. HTPDN and LOCKN Scheme without HTPDN Connection

Multiple-chip Configuration

In order to reduce the number of cables needed for HTPDN and LOCKN in multiple-chip configuration, THCV226 is equipped with the DGLOCK pin. When all the DGLOCK pins are connected as in Figure 6 , the connected Rx chips can share the CDR lock status via DGLOCK, making all the Rx chips in the same operation status.

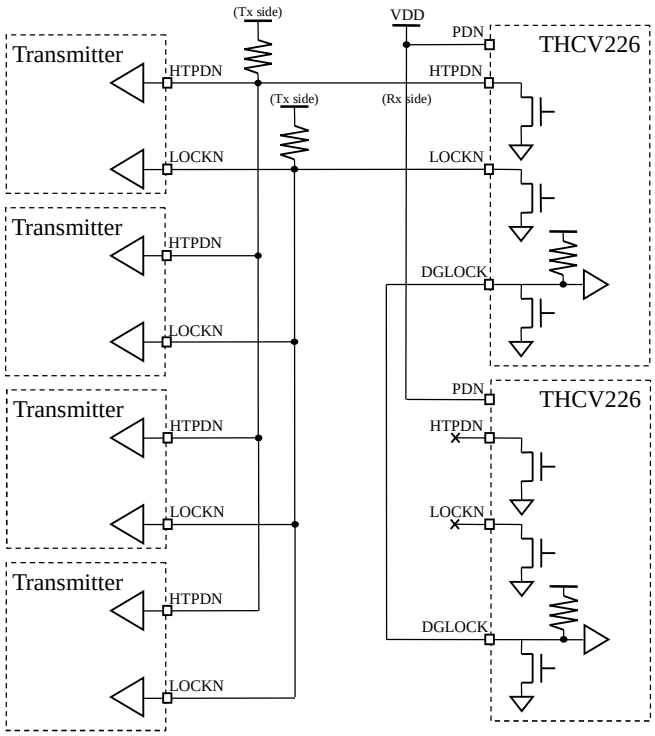


Figure 6. Usage of DGLOCK in Multiple-Rx Configuration

LVDS Reduced Swing Output Function

RS pin controls LVDS output swing level.

Table 4. LVDS Output Level Select

RS	Output Swing Level
0	Reduced Swing Level (200mV typical)
1	Normal Swing Level (350mV typical)

LVDS Output Enable Function

By setting the OE and OPF pins, the following output enable function can be selected.

In output disable condition, all the outputs take low fixed data or High-Z except for HTPDN, LOCKN and DGLOCK.

Table 5. LVDS Output Enable Function

LOCKN	OE	OPF	LVDS Outputs	
			Status	Output Condition
1	1	1	Enable	Low Fixed Data
		0		Hi-Z
	0	1	Disable	Low Fixed Data
		0		Hi-Z
0	1	1	Enable	Normal Data
		0		
	0	1	Disable	Low Fixed Data
		0		Hi-Z

LVDS Data Mapping

LVDS data (video data, control data, DE) are mapped as Figure 7. RLC[6] is special bit for DE (data enable). RLC[5:4] are for control data bits, and the other bits are for video data. Also there are special assigned bits, 'CTL' transmitted under DE=0 condition.

The number of LVDS channels depends on color depth mode, COL.

RLD[6] is not available at COL=0, 8-bit color depth mode.

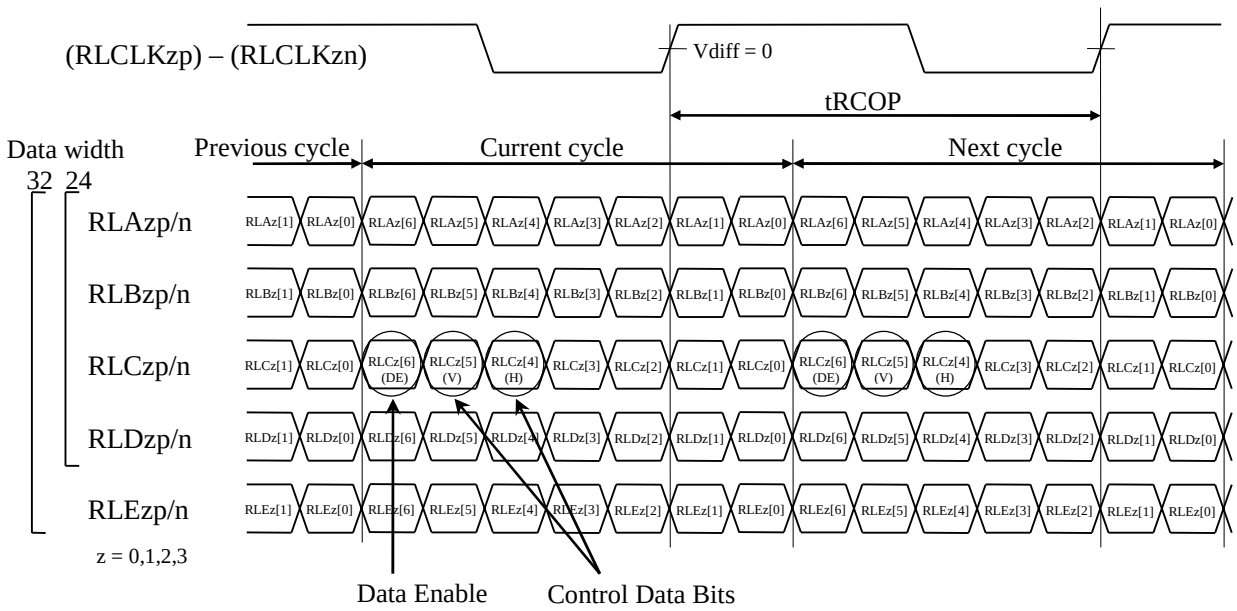


Figure 7. LVDS Output Switching Timing Diagram

Table 6. LVDS Data Mapping Table for JEIDA Format (MAP=1)

THCV226 Output	COL		Comment
	0 (8bit)	1 (10bit)	
RLAz[0]	R[2]	R[4]	Data bit
RLAz[1]	R[3]	R[5]	Data bit
RLAz[2]	R[4]	R[6]	Data bit
RLAz[3]	R[5]	R[7]	Data bit
RLAz[4]	R[6]	R[8]	Data bit
RLAz[5]	R[7]	R[9]	Data bit
RLAz[6]	G[2]	G[4]	Data bit
RLBz[0]	G[3]	G[5]	Data bit
RLBz[1]	G[4]	G[6]	Data bit
RLBz[2]	G[5]	G[7]	Data bit
RLBz[3]	G[6]	G[8]	Data bit
RLBz[4]	G[7]	G[9]	Data bit
RLBz[5]	B[2]*2	B[4]*2	Data bit
RLBz[6]	B[3]*2	B[5]*2	Data bit
RLCz[0]	B[4]*2	B[6]*2	Data bit
RLCz[1]	B[5]*2	B[7]*2	Data bit
RLCz[2]	B[6]*2	B[8]*2	Data bit
RLCz[3]	B[7]*2	B[9]*2	Data bit
RLCz[4]	HSYNC	HSYNC	Control bit
RLCz[5]	VSYNC	VSYNC	Control bit
RLCz[6]	DE	DE	Data Enable*2
RLDz[0]	R[0]	R[2]	Data bit
RLDz[1]	R[1]	R[3]	Data bit
RLDz[2]	G[0]	G[2]	Data bit
RLDz[3]	G[1]	G[3]	Data bit
RLDz[4]	B[0]*2	B[2]*2	Data bit
RLDz[5]	B[1]*2	B[3]*2	Data bit
RLDz[6]	N/A*1	CONT[1]*2*3	Data bit
RLEz[0]	Channel Power Down	R[0]*2	Data bit
RLEz[1]		R[1]*2	Data bit
RLEz[2]		G[0]*2	Data bit
RLEz[3]		G[1]*2	Data bit
RLEz[4]		B[0]*2	Data bit
RLEz[5]		B[1]*2	Data bit
RLEz[6]		CONT[2]*2*3	Data bit

Table 1.

*1 N/A : Not available. THCV226 outputs RLDz[6]=0
*2 CTL bits, which are carried during DE=0 expect the 1st and the last pixel.(If MODE0=0)
Which are carried during DE=0 except the 1st, 2nd and last 2pixel.(IF MODE0=1)
*3 3D flags defined in the V-by-One® HS Standard are assigned to the following bits.
V-by-One® HS Standard Packer/Unpacker D[24](3DLR) ⇔ LVDS RLEz[6].
V-by-One® HS Standard Packer/Unpacker D[25](3DEN) ⇔ LVDS RLDz[6].
(z=0,1,2,3)

Table 7. LVDS Data Mapping Table for VESA Format (MAP=0)

THCV226 Output	COL		Comment
	0 (8bit)	1 (10bit)	
RLAz[0]	R[0]	R[0]*2	Data bit
RLAz[1]	R[1]	R[1]*2	Data bit
RLAz[2]	R[2]	R[2]	Data bit
RLAz[3]	R[3]	R[3]	Data bit
RLAz[4]	R[4]	R[4]	Data bit
RLAz[5]	R[5]	R[5]	Data bit
RLAz[6]	G[0]	G[0]*2	Data bit
RLBz[0]	G[1]	G[1]*2	Data bit
RLBz[1]	G[2]	G[2]	Data bit
RLBz[2]	G[3]	G[3]	Data bit
RLBz[3]	G[4]	G[4]	Data bit
RLBz[4]	G[5]	G[5]	Data bit
RLBz[5]	B[0]*2	B[0]*2	Data bit
RLBz[6]	B[1]*2	B[1]*2	Data bit
RLCz[0]	B[2]*2	B[2]*2	Data bit
RLCz[1]	B[3]*2	B[3]*2	Data bit
RLCz[2]	B[4]*2	B[4]*2	Data bit
RLCz[3]	B[5]*2	B[5]*2	Data bit
RLCz[4]	HSYNC	HSYNC	Control bit
RLCz[5]	VSYNC	VSYNC	Control bit
RLCz[6]	DE	DE	Data Enable*2
RLDz[0]	R[6]	R[6]	Data bit
RLDz[1]	R[7]	R[7]	Data bit
RLDz[2]	G[6]	G[6]	Data bit
RLDz[3]	G[7]	G[7]	Data bit
RLDz[4]	B[6]*2	B[6]*2	Data bit
RLDz[5]	B[7]*2	B[7]*2	Data bit
RLDz[6]	N/A*1	CONT[1]*2*3	Data bit
RLEz[0]	Channel Power Down	R[8]	Data bit
RLEz[1]		R[9]	Data bit
RLEz[2]		G[8]	Data bit
RLEz[3]		G[9]	Data bit
RLEz[4]		B[8]*2	Data bit
RLEz[5]		B[9]*2	Data bit
RLEz[6]		CONT[2]*2*3	Data bit

*1 N/A : Not available. THCV226 outputs RLDz[6]=0

*2 CTL bits, which are carried during DE=0 expect the 1st and the last pixel.(If MODE0=0)
Which are carried during DE=0 except the 1st, 2nd and last 2pixel.(IF MODE0=1)

*3 3D flags defined in the V-by-One® HS Standard are assigned to the following bits.
V-by-One® HS Standard Packer/Unpacker D[24](3DLR) ⇔ LVDS RLEz[6].
V-by-One® HS Standard Packer/Unpacker D[25](3DEN) ⇔ LVDS RLDz[6].
(z=0,1,2,3)

Monitoring Signal Function

The recovered HSYNC, VSYNC, DE or CLK from V-by-One® HS signals can be monitored by "Monitoring Signal Function". The monitoring lane out of four high-speed data lane is selectable. This function is used for debugging purpose and set by five pins, MON_EN, MON SEL0/1/2/3.

The monitoring signal is outputted from MONOUT pin as 1.8V LVCMOS signal.

All signals operate as normal mode except these setting pins and monitoring output pin when "Monitoring Signal Function" is enabled. See the table below.

Table 8. Monitoring Signal Function

Pin Option					Monitoring Output	Description
Function	Lane Selection		Signal Selection			
MON_EN	MON_SEL0	MON_SEL1	MON_SEL2	MON_SEL3	MONOUT	
0	0	0	0	0	(Invalid)	Normal mode
1	0	0	0	0	DE	Monitoring Signal Mode to Check Lane0
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	1	0	0	0	DE	Monitoring Signal Mode to Check Lane1
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	0	1	0	0	DE	Monitoring Signal Mode to Check Lane2
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	
	1	1	0	0	DE	Monitoring Signal Mode to Check Lane3
			0	1	HSYNC	
			1	0	VSYNC	
			1	1	CLK	

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage (VVDD,LVDD,LPVDD,PVDD,CVDD,IOVDD)	-0.3	-	2.1	V
CMOS Input Voltage	-0.3	-	IOVDD+0.3	V
CMOS Output Voltage	-0.3	-	IOVDD+0.3	V
Open Drain Output Voltage	-0.3	-	3.6	V
CML Receiver Input Voltage	-0.3	-	VVDD+0.3	V
LVDS Transmitter Output Voltage	-0.3	-	LVDD+0.3	V
Output Current	-50	-	50	mA
Storage temperature	-55	-	125	˚C
Junction temperature	-	-	125	˚C
Reflow Peak Temperature/Time	-	-	260/10	˚C/sec
Maximum Power Dissipation @+25deg	-	-	2.5	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage (VVDD,LVDD,LPVDD,PVDD,CVDD,IOVDD)	1.62	1.80	1.98	V
Ta	Operating Temperature	-40	-	85	˚C

Supply Current

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
IRCCW	Power Supply Current (Worst case pattern) 10bit mode	MODE2,1,0=111	-	450	515	mA
		MODE2,1,0=001	-	360	415	
		MODE2,1,0=000	-	420	475	
		MODE2,1,0=100	-	295	335	
	Power Supply Current (Gray scale pattern) 10bit mode	MODE2,1,0=111	-	370	440	
		MODE2,1,0=001	-	300	355	
		MODE2,1,0=000	-	345	405	
		MODE2,1,0=100	-	245	285	
IRCCS	Power Down Supply Current	PDN = 0	-	-	1	mA

* VDD=1.8V, Room temperature

Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LVCMOS DC Specifications						
VIH	High Level Input Voltage	-	0.65VDD	-	VDD+0.3	V
VIL	Low Level Input Voltage	-	-0.3	-	0.35VDD	V
VOH	High Level Output Voltage (IO Type : O)	IOH = -2mA	VDD-0.2	-	VDD	V
VOL	Low Level Output Voltage (IO Type : O,OD)	IOL = 2mA	GND	-	0.2	V
	Low Level Output Voltage (IO Type : BI)	IOL = 160uA	GND	-	0.2	V
IOZH	Output Leak Current High in Hi-Z State	-	-10	-	10	uA
IOZL	Output Leak Current Low in Hi-Z State	-	-10	-	10	uA
IIH	High Level Input Leakage Current	-	-10	-	10	uA
IIL	Low Level Input Leakage Current	-	-10	-	10	uA
CML DC Specifications						
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input High Leak Current	PDN=0, Rxzp/n=VDD	-10	-	10	uA
IRIL	CML Input Low Leak Current	PDN=0 Rxzp/n=GND	-10	-	10	uA
IRRIH	CML Input High Current	Rxzp/n=VDD	-	-	2	mA
IRRIL	CML Input Low Current	Rxzp/n=GND	-6	-	-	mA
RRIN	CML Differential Input Resistance	-	80	100	120	Ω
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
LVDS DC Specifications						
VROD	LVDS Differential Mode Output Voltage	RL = 100Ω RS = 1	250	350	450	mV
	LVDS Differential Mode Output Voltage	RL = 100Ω RS = 0	100	200	300	mV
⊿ROD	Change in VROD between Complementary Output States	RL = 100Ω	-	-	35	mV
VROC	LVDS Common Mode Output Voltage	RL = 100Ω	1.125	1.25	1.375	V
⊿ROC	Change in VROD between Complementary Output States	RL = 100Ω	-	-	35	mV
IROS	LVDS Output Short Circuit Current	RLyzp/n = GND RL = 100Ω	-	-	100	mA
IROZ	LVDS Output Tri-State Current	PDN = 0 RLyzp/n =GND～VDD	-20	-	20	uA

*y=A,B,C,CLK,D,E / z=0,1,2,3

Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CML AC Specifications						
tRBIT	Unit Interval (UI)	COL = 0	370	tRCOP/30	833	ps
		COL = 1	294	tRCOP/40	625	ps
tRISK	CML Lane0/1/2/3 Input Inter Pair Skew Margin	COL = 0	-30	-	30	UI
		COL = 1	-40	-	40	UI
tRIJT	CML Lane0/1/2/3 Input Jitter Margin	COL = 0	-	-	15	UI
		COL = 1	-	-	20	UI
LVDS AC Specifications						
tRCOP	Clock Out Period	-	6.37	-	25	ns
tRLVT	LVDS Differential Output Transition Time	-	-	0.6	1.5	ns
tROP1	LVDS Output Data Position0	HSLVDS mode (tRCOP= 6.37ns – 8.33ns)	-0.20	-	0.20	ns
tROP0	LVDS Output Data Position1		tRCOP/7 -0.20	tRCOP/7	tRCOP/7 +0.20	ns
tROP6	LVDS Output Data Position2		2tRCOP/7 -0.20	2tRCOP/7	2tRCOP/7 +0.20	ns
tROP5	LVDS Output Data Position3		3tRCOP/7 -0.20	3tRCOP/7	3tRCOP/7 +0.20	ns
tROP4	LVDS Output Data Position4		4tRCOP/7 -0.20	4tRCOP/7	4tRCOP/7 +0.20	ns
tROP3	LVDS Output Data Position5		5tRCOP/7 -0.20	5tRCOP/7	5tRCOP/7 +0.20	ns
tROP2	LVDS Output Data Position6		6tRCOP/7 -0.20	6tRCOP/7	6tRCOP/7 +0.20	ns
tROP1	LVDS Output Data Position0	Normal LVDS mode (tRCOP= 11.1ns -16.6ns)	-0.25	-	0.25	ns
tROP0	LVDS Output Data Position1		tRCOP/7 -0.25	tRCOP/7	tRCOP/7 +0.25	ns
tROP6	LVDS Output Data Position2		2tRCOP/7 -0.25	2tRCOP/7	2tRCOP/7 +0.25	ns
tROP5	LVDS Output Data Position3		3tRCOP/7 -0.25	3tRCOP/7	3tRCOP/7 +0.25	ns
tROP4	LVDS Output Data Position4		4tRCOP/7 -0.25	4tRCOP/7	4tRCOP/7 +0.25	ns
tROP3	LVDS Output Data Position5		5tRCOP/7 -0.25	5tRCOP/7	5tRCOP/7 +0.25	ns
tROP2	LVDS Output Data Position6		6tRCOP/7 -0.25	6tRCOP/7	6tRCOP/7 +0.25	ns
tROSK	Link0/1/2/3 LVDS Output Clock Skew	-	-	-	500	ps

Switching Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Delay time						
tRDC	Input Data to Output Data Delay	MODE0 = 0 COL = 0	(17+27/30) tRCOP+4.5	-	(17+27/30) tRCOP+13.5	ns
		MODE0 = 1 COL = 0	(34+24/30) tRCOP+5.0	-	(34+24/30) tRCOP+15.5	
		MODE0 = 0 COL = 1	(17+7/40) tRCOP+4.5	-	(17+7/40) tRCOP+13.5	
		MODE0 = 1 COL = 1	(33+14/40) tRCOP+5.0	-	(33+14/40) tRCOP+15.5	ns
tRPD	Power On to PDN High Delay	-	0	-	-	ns
tRHPD0	PDN High to HTPDN Low Delay	-	-	-	1	us
tRHPD1	PDN Low to HTPDN High Delay	-	-	-	1	us
tRPLL0	Training Pattern Input to LOCKN Low Delay	-	-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay	-	-	-	10	us
tRPLL2	LOCKN Low to LVDS CLK Lock Time	-	-	-	10	ms
tRLCK0	LOCKN Low to LVDS Output Delay	-	-	-	1	ms
tRLCK1	LOCKN High to LVDS Output High-Z/Low Delay	-	-	-	1	ms
tRDLH	DGLOCK High to LOCKN Low	-	0	-	-	ns
tRDLL	DGLOCK Low to LOCKN High	-	0	-	-	ns
DE Input Timing						
tRDEH	DE=1 Duration	MODE0 = 0	8tRCOP	-	-	ns
		MODE0 = 1	16tRCOP	-	-	ns
tRDEL	DE=0 Duration	MODE0 = 0	8tRCOP	-	-	ns
		MODE0 = 1	16tRCOP	-	-	ns

AC Timing Diagram and Test Circuit

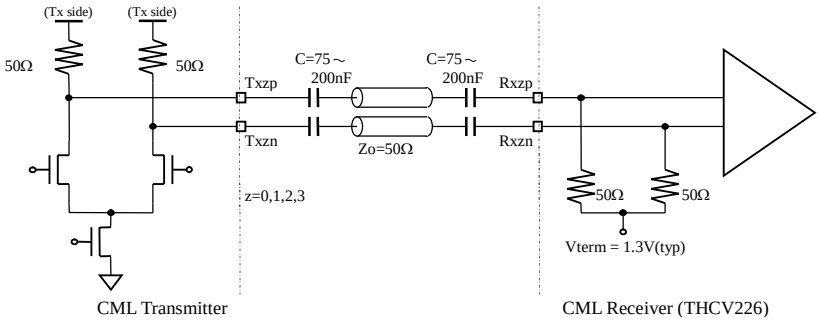


Figure 8. CML Buffer Scheme

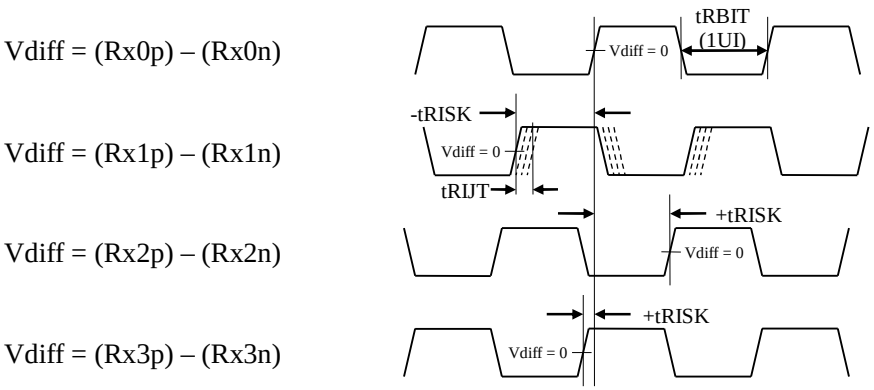


Figure 9. CML Input Timing Diagram

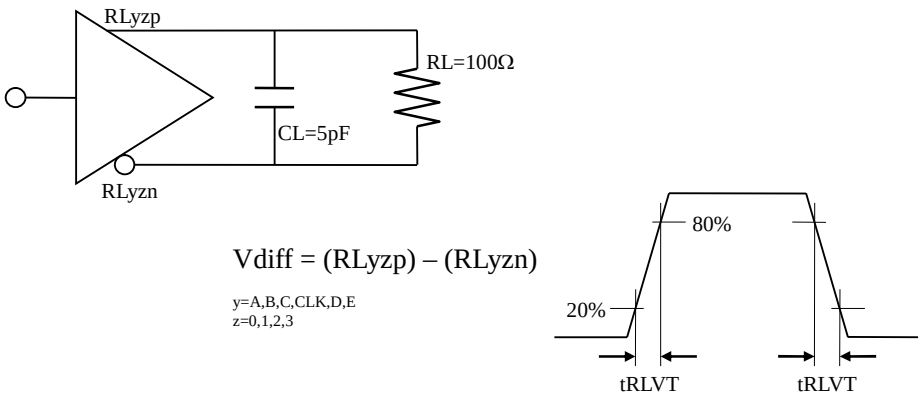


Figure 10. LVDS Output Switching Timing Diagram and Test Circuit

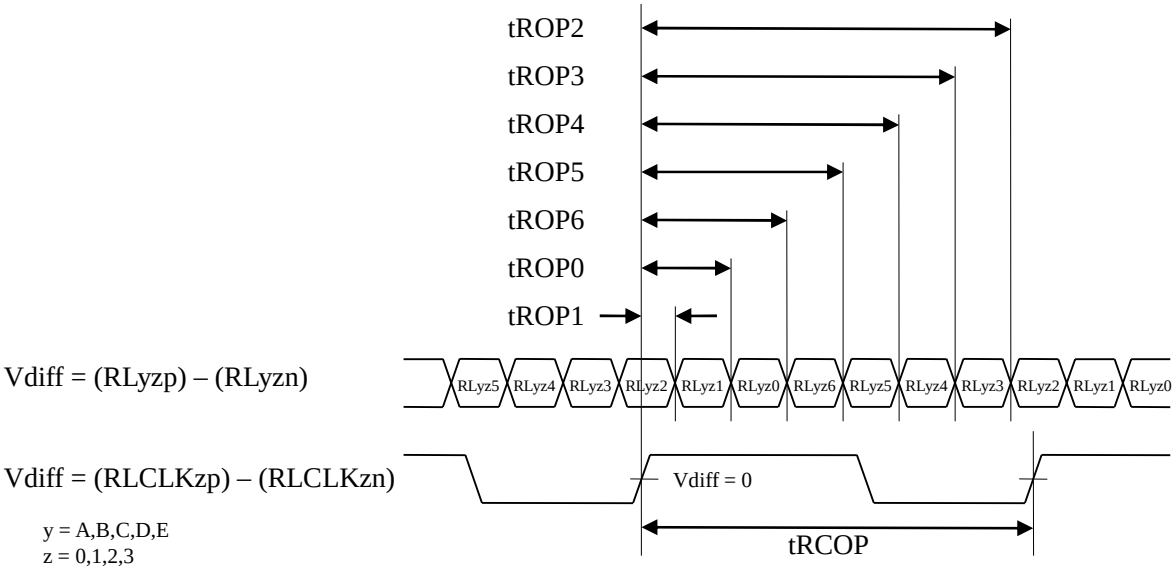


Figure 11. LVDS Output Switching Timing Diagram

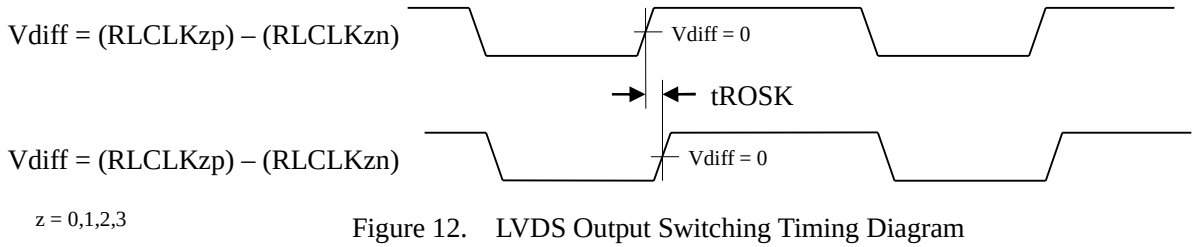


Figure 12. LVDS Output Switching Timing Diagram

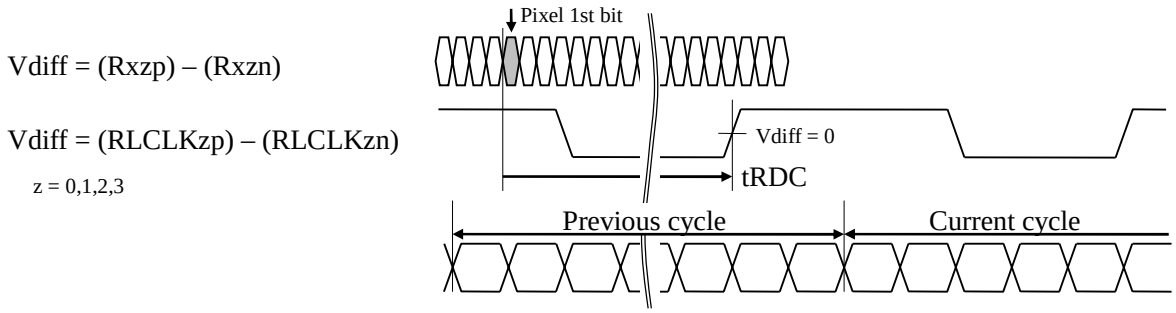


Figure 13. V-by-One® HS Input to LVDS Output Latency

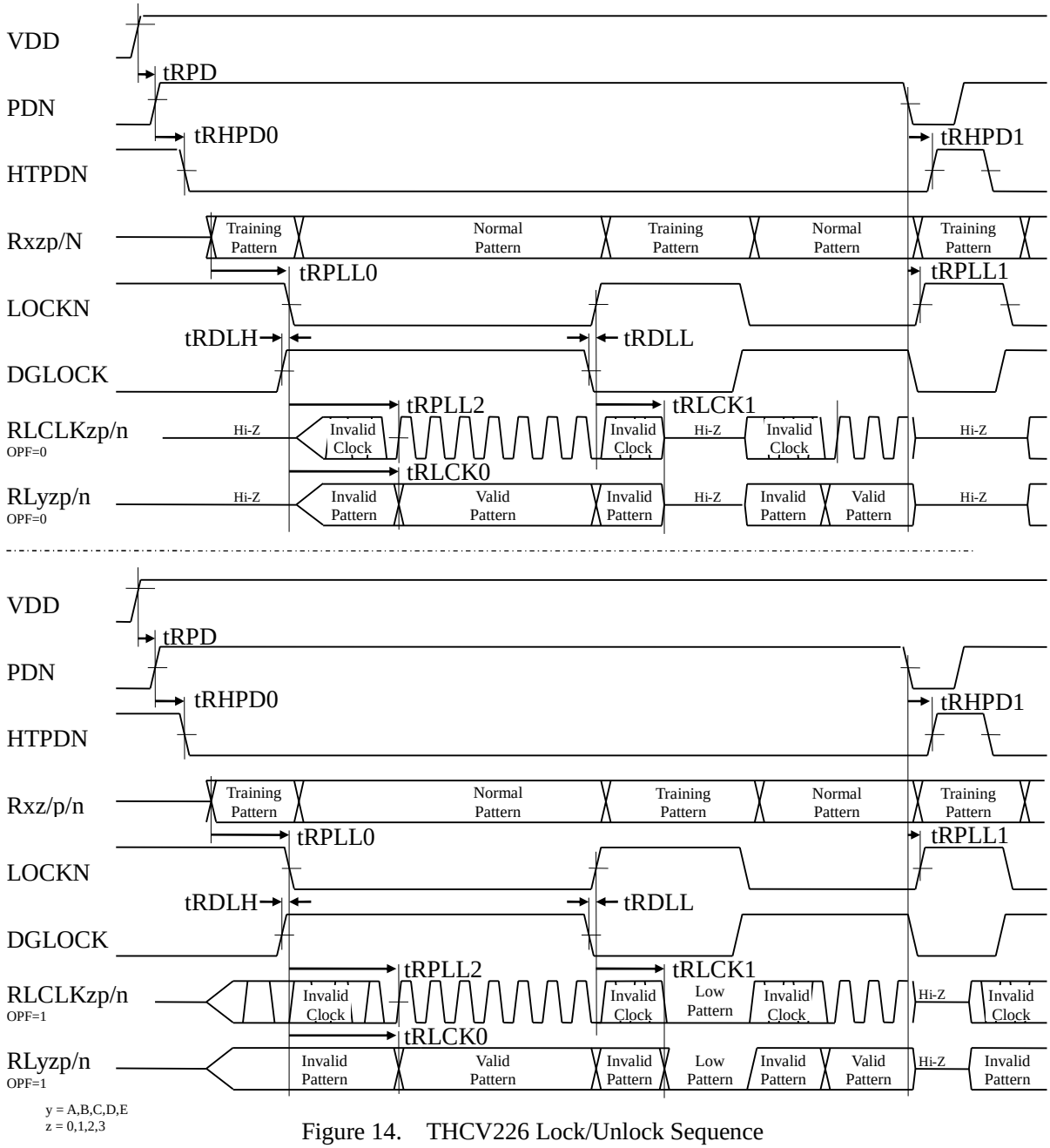


Figure 14. THCV226 Lock/Unlock Sequence

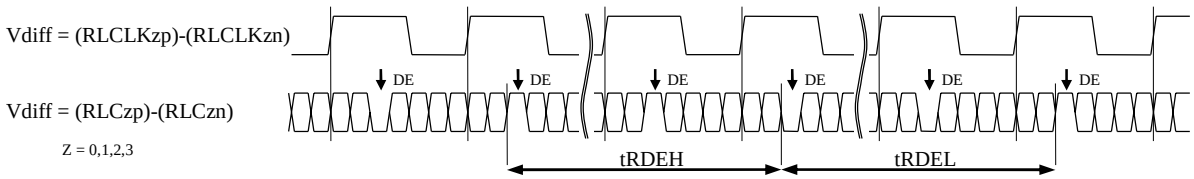


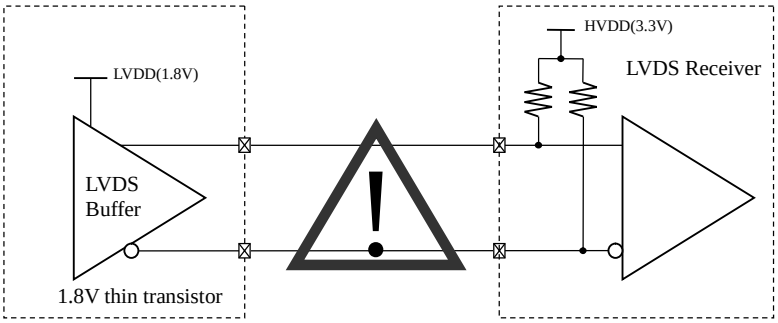
Figure 15. DE Period Requirement

Note

1) LVDS Output Pin Connection

In case that the LVDS Rx of destination device is equipped with pull-up resistors connected to higher than THCV226's VDD voltage, this can cause violation of absolute maximum ratings to THCV226. This phenomenon may be happened at power-on phase and Hi-Z state of the whole system including LVDS Rx device.

One solution for this problem is power-down control for LVDS Rx device during no LVDS input or Hi-Z state period, if its pull-up resistors can be cut off at power-down state. Another solution is to set THCV226's OPF option pin to VDD. This setting provides low fixed data output mode at PDN=1, not Hi-Z state mode.



2) Cable Connection and Disconnection

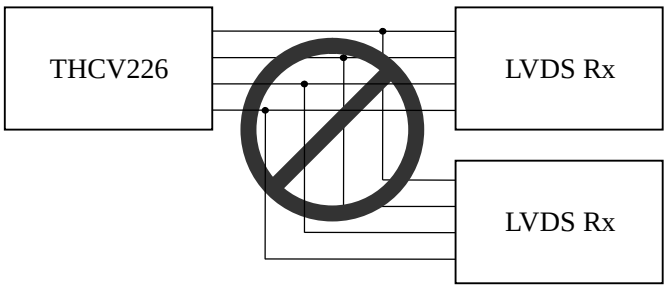
Do not connect and disconnect the LVDS and CML cables, when the power is supplied to the system.

3) GND Connection

Connect the each GND of the PCB which Transmitter and Receiver. It is better for EMI reduction to place GND cables as close to LVDS and CML cables as possible.

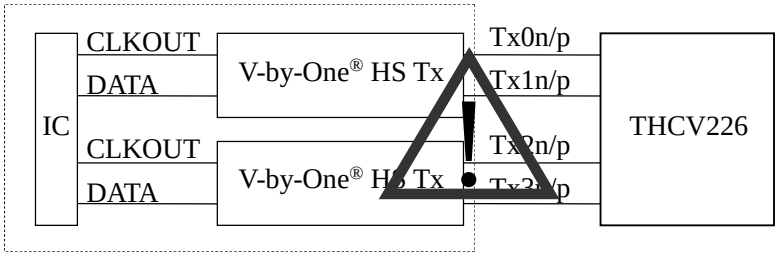
4) Multi-drop Connect

Multi-drop connect is not recommended.



5) Multiple Counterpart Use

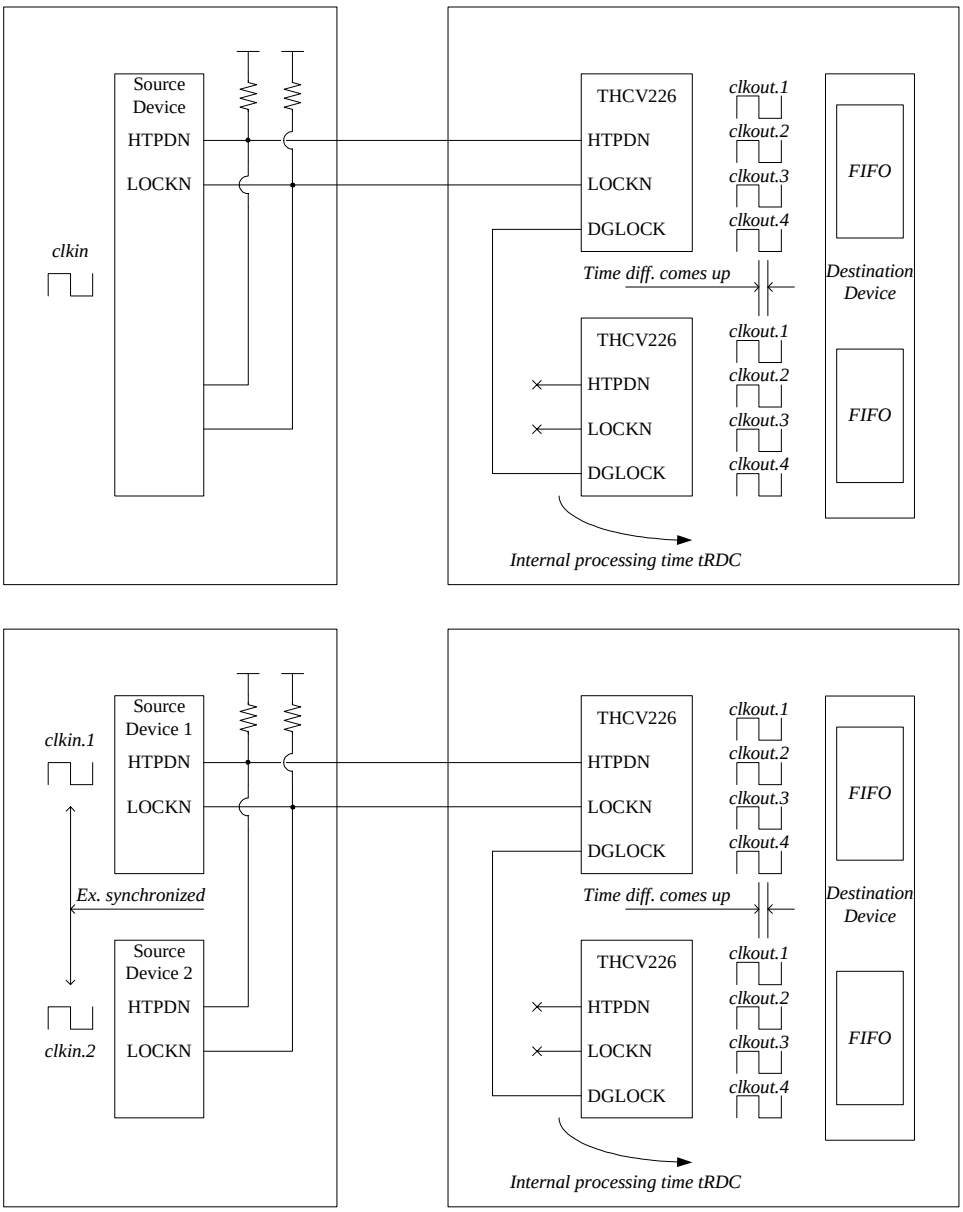
Multiple counterpart use such as the following system is not recommended. If it is not avoidable, please check whether tRISK and tRIJT spec of THCV226 can be kept or not. Furthermore, please contact to



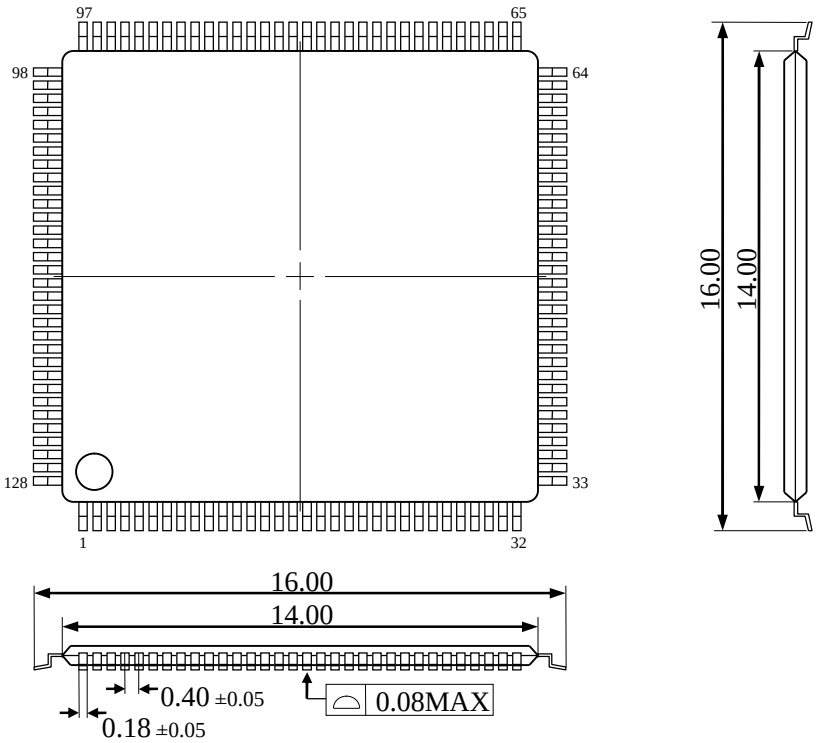
6) Multiple Device Connection

HTPDN and LOCKN signals are supposed to be connected properly for their purpose like the following figure. HTPDN should be from just one THCV226 to multiple Tx devices because its purpose is only ignition of all Tx devices. LOCKN should be connected so as to indicate that CDR status of all Rx devices becomes ready to receive normal operation data. LOCKN of Tx side can be simply split to multiple Tx devices. THCV226's DGLOCK is appropriate for multiple Rx use.

Also possible time difference of internal processing time (THCV226 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV226s, which may have internal FIFO.



Package



Detail of Lead End

Unit : mm

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