THCV220

V-by-One® HS High-speed video data receiver

General Description

THCV220 is designed to support video data transmission between the host and display.

One high-speed lane can carry up to 32bit data and 3 bits of synchronizing signals at a pixel clock frequency from 7.5MHz to 93MHz.

It has one high-speed data lane and, maximum serial data rate is 3.75Gbps/lane.

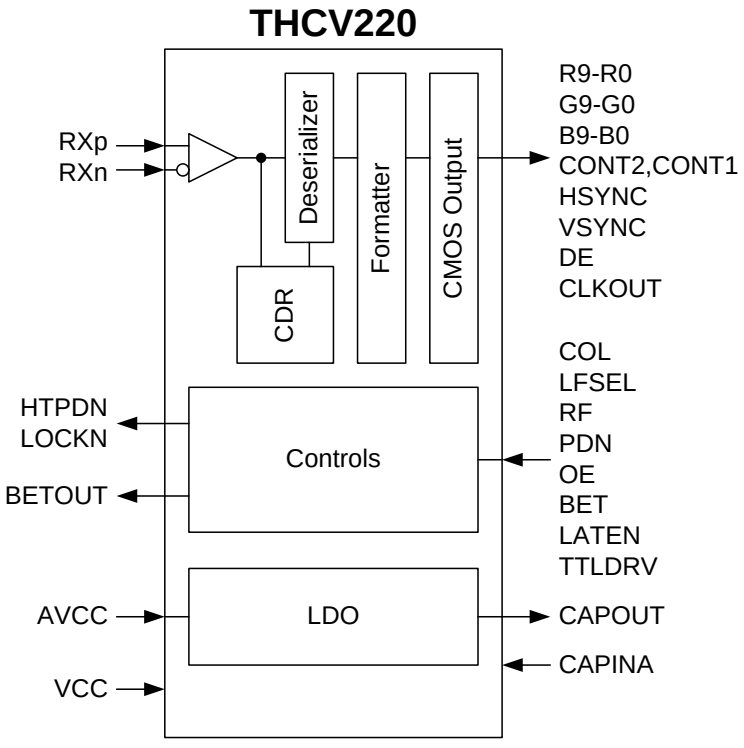
Width	Link	TTL Clock Freq.
24bit	Si/So	10MHz to 125MHz
32bit	Si/So	7.5MHz to 93MHz

Si/So : Single-in/Single-out,

Features

- Color depth selectable: 24(8*3)/32(10*3)bit
- Single Link
- AC coupling for high speed lines
- Wide Range Supply Voltage 2.3-3.6V
- Package: 64 pin QFN
- Wide frequency range
- CDR requires no external freq. reference
- Spread Spectrum Clocking tolerant
  Up to 30kHz/±0.5% (center spread)
- V-by-One® HS standard Ver.1.4 compliant
- AEC-Q100 ESD Protection

Block Diagram



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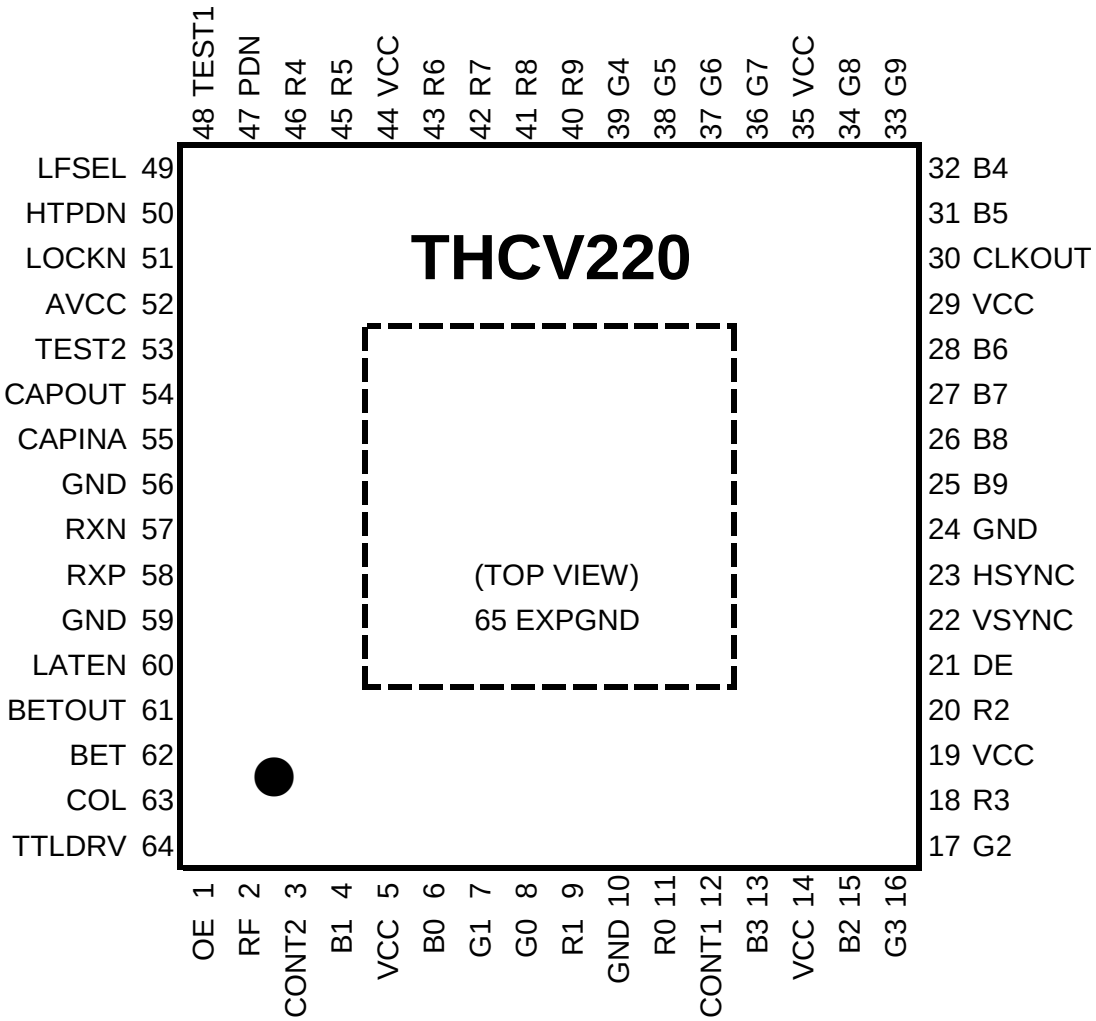
Pin configuration



Pin Description

THCV220 pin description

Pin Name	Pin #	type	Description
R9-R0	40,41,42,43,45, 46,18,20,9,11	O3	pixel data outputs
G9-G0	33,34,36,37,38, 39,16,17,7,8	O3	pixel data outputs
B9-B0	25,26,27,28,31, 32,13,15,4,6	O3	pixel data outputs
CONT1,2	12,3	O3	User defined data outputs. Active only in 32bit mode.
DE	21	O3	DE Output
VSYNC	22	O3	Vsync Output
HSYNC	23	O3	Hsync Output
CLKOUT	30	O3	Pixel clock output
RXN/P	57,58	CI	High-speed CML signal input.
LOCKN	51	OD3	Lock detect output. Must be connected to Tx LOCKN with a 10kΩ pull-up resistor.
HTPDN	50	OD3	Hot plug detect output. Must be connected to Tx HTPDN with a 10kΩ pull-up resistor.
PDN	47	I3L	Power down input. H: Normal operation L: Power down
TTLDRV	64	I3	TTL outputs drive strength select input. H : Normal drive strength L : Weak drive strength
OE	1	I3	Output enable input. H: All CMOS outputs enabled L: All CMOS outputs disabled, except for LOCKN, HTPDN
COL	63	I3	Data width setting. H : 24bit L : 32bit
LFSEL	49	I3	Frequency range setting. H: Low frequency operation L: Normal Operation
RF	2	I3	Output clock triggering edge select input H: Rising edge L: Falling edge
BET	62	I3	Field-BET entry. H : Field BET Operation L : Normal Operation
BETOUT	61	O3	Field BET result output. Must be left OPEN when NOT used.
LATEN	60	I3	Latch select input under Field-BET operation H : Latched result L : NOT Latched result
TEST1	48	-	Test pin, must be “L” for normal operation.
TEST2	53	-	Test pin, must be “L” for normal operation.
CAPOUT	54	-	Decoupling capacitor pins. This pin should be connected to external decoupling capacitors. Recommended Capacitance is 2.2uF
CAPINA	55	-	Reference Input for Analog circuit.Must be tied CAPOUT.
VCC	5,14,19,29, 35,44	PS	Digital Power supply Pins
AVCC	52	PS	Analog Power supply Pin
GND	10,24,56,59	PS	Ground Pins
EXPGND	65	PS	Exposed Pad Ground

*type symbol

I3=3.3v CMOS input, I3L=Low Speed 3.3v CMOS input, O3=3.3v CMOS output, OD3=3.3v Open drain output

CI=CML input, PS=Power Supply

Functional Description

Functional Overview

With V-by-One® HS proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV220 enable transmission of 8/10 bit RGB, 2bits of user-defined data (CONT), synchronizing signals HSYNC, VSYNC, and DE by a pair cable with minimal external components.

THCV220 automatically extracts the clock from the incoming data streams and converts the serial data into video data with DE being high or synchronizing data with DE being low, recognizing which type of serial data is being sent by the transmitter. And it outputs the recovered data in the form of CMOS/TTL data.

THCV220 can operate for a wide range of a serial bit rate from 600Mbps to 3.75Gbps.
It does not need any external frequency reference, such as a crystal oscillator.

Internal Reference Output/Input Function (CAPOUT,CAPINA)

An internal regulator produces the 1.2V (CAPOUT). This 1.2V linear regulator can not supply any other external loads. Bypass CAPOUT to GND with 2.2uF.

CAPINA supplies reference voltage for any internal analog circuit also. Bypass CAPINA to GND with 0.1uF to remove high frequency noise. CAPOUT and CAPINA must be tied together.

Analog power supply AVCC is supposed to be stabilized with de-coupling capacitor and series noise filter (for example, ferrite bead).

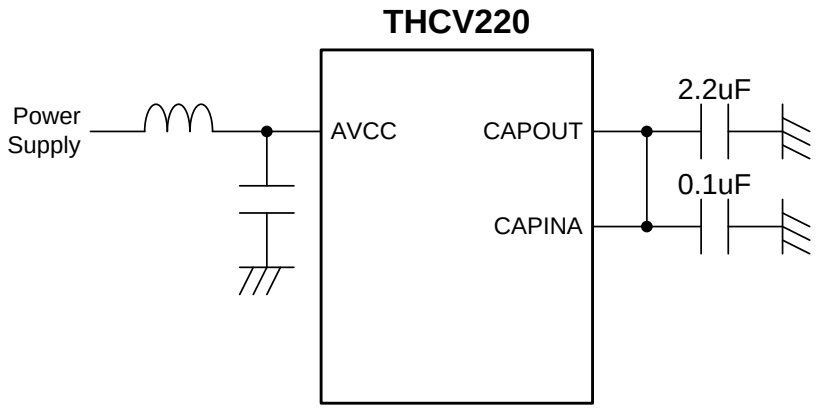


Figure 1. Connection of CAPOUT, CAPINA and Decoupling Capacitor

Data Enable

Figure 2 is the conceptual diagram of the basic operation of the chipset. THCV219 in Figure 2 is an example of V-by-One® HS Transmitter. There are some requirements for DE. Figure 3 shows the timing diagram of it.

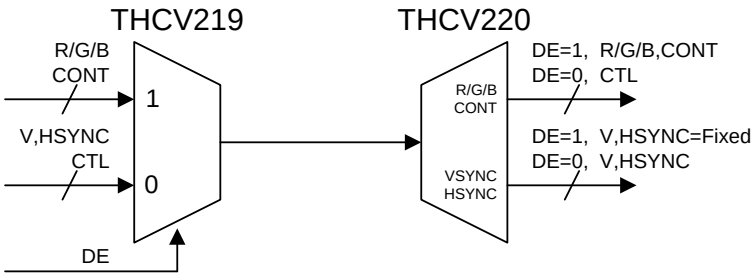


Figure 2. Conceptual diagram of the basic operation of the chipset

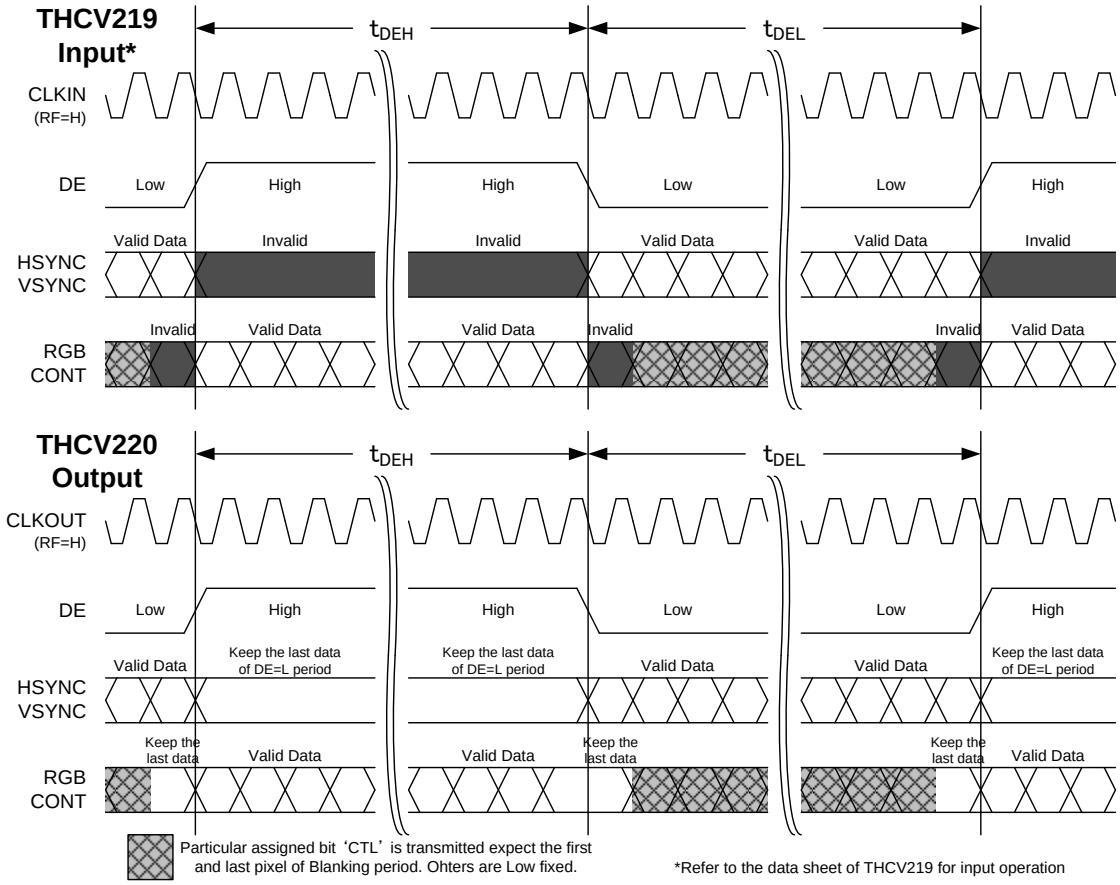


Figure 3. Data and synchronizing signals transmission timing diagram

Table 1. DE requirement

symbol	Parameter	min.	typ.	max.	Unit
tDEH	DE=High Duration	2tTCIP	-	-	sec
tDEL	DE=Low Duration	2tTCIP	-	-	sec

Color Depth and Frequency Range Select function

The mode selected by the combination of the COL and LFSEL pin settings is shown in Table 2.

The 32bit mode and 24bit mode correspond to the 4Byte mode and 3Byte mode in the V-by-One® HS standard, respectively.

Low Frequency mode is a THine proprietary feature. To use this mode, a Transmitter device with this function must be used. The Transmitter device must also be set to Low Frequency mode.

Table 2. operation mode select

COL	LFSEL	Description	Freq. Range
L	L	32bit mode	15 to 93M
	H	32bit Low frequency mode	7.5 to 30M
H	L	24bit mode	20 to 125M
	H	24bit Low frequency mode	10 to 40M

Hot-Plug Function

HTPDN indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is high when the Receiver is not active or not connected. Then Transmitter can enter into the power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the Transmitter and the Receiver can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as Low.

Lock Detect Function

LOCKN indicates whether the CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High by pull-up resistor when Receiver is not active or at the CDR PLL training state. LOCKN is set to Low by the Receiver when CDR lock is done. Then the CDR training mode finishes and Transmitter shifts to the normal mode. LOCKN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the Receiver.

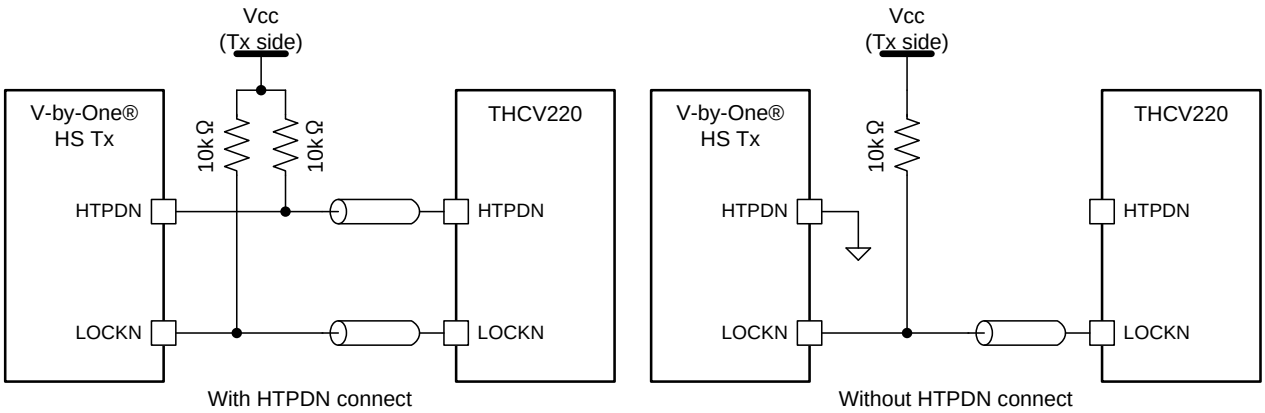


Figure 4. Hot-plug and Lock detect scheme

Drive Select Function

TTLDRV pin controls TTL output strength. See Table 3.

Table 3. Drive Select function table

TTLDRV	Description
L	Weak TTL output strength
H	Normal TTL output strength

Power Down Function

Setting the PDN pin low places THCV220 in the power-down mode. Internal circuitry turns off and the CMOS outputs drives low or Hi-Z depends on OE pin.

Table 4. Power Down function table

PDN	Description
L	Power Down
H	Normal Operation

Output Enable Function

OE pin select CMOS/TTL output states. It is enabled with OE=H. When OE=L, CMOS/TTL outputs turns high-Z. See Table 5.

Table 5. OE function table

PDN	OE	CMOS/TTL Output
-	L	Hi-Z
L	H	Low Fixed
H		Normal Operation

Field BET Operation

In order to help users to check validity of CML high-speed serial line, THCV220 has an operation mode in which they act as a bit error tester (BET). THCV219 which is an example of Tx device also has BET function mode. In this mode, THCV219 internally generates test pattern which is then serialized onto the CML high-speed line. THCV220 receives the data stream and checks bit errors.

This "Field BET" mode is activated by setting BET= H both on THCV219 and THCV220. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for THCV220, the internal test pattern check circuit gets enabled and reports result on BETOUT pin. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error. Please refer to Table 6. User can select two kinds of check result, “Latched-result” or “NOT latched result”. The latch is reset by setting LATEN=L.

Table 6. Field BET operation pin settings

THCV219	THCV220		Condition	
BET	BET	LATEN	Operation	Output Latch select
L	L	L	Normal Operation	-
		H	Forbidden	-
H	H	L	Field BET Operation	NOT latched result
H	H	H		Latched result

Table 7. THCV220 Field BET result

BETOUT	Output
L	Bit error occurred
H	No error

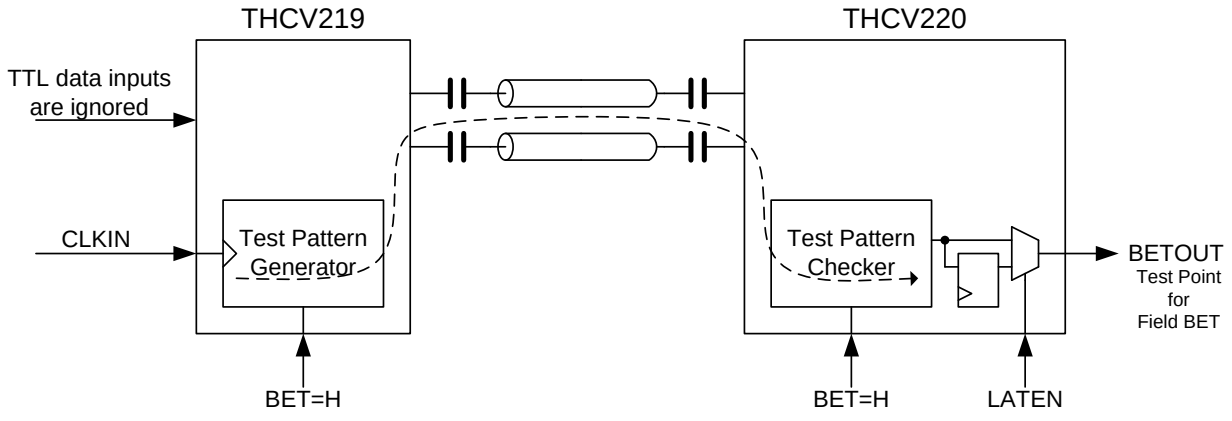


Figure 5. Field BET Configuration

Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage(VCC,AVCC)	-0.3	-	+4.0	V
CMOS Input Voltage	-0.3	-	VCC+0.3	V
CMOS Output Voltage	-0.3	-	VCC+0.3	V
CMOS Open Drain Output Voltage	-0.3	-	+4.0	V
CML Receiver Input Voltage	-0.3	-	CAPINA+0.3	V
Output Current	-30	-	30	mA
Storage Temperature	-55	-	+125	℃
Junction Temperature	-	-	+125	℃
Reflow Peak Temperature/Time	-	-	+260/10sec	℃

* "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

Parameter	min.	typ.	max.	Unit
Supply Voltage（VCC,AVCC）	2.3	2.5	2.7	V
	2.6	2.8	3.0	V
	3.0	3.3	3.6	V
CAPOUT and CAPINA Voltage	-	1.20	-	V
Operating Temperature	-40	-	85	℃

Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter	conditions	min.	typ.	max.	Unit
Supply Current	PDN=H COL=L Cload=8pF Worst Case Pattern	-	-	170	mA
	PDN=L All Inputs =Fixed LorH	-	1.2	10	mA

Electrical Specifications

CMOS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
IOZH	Output Leak Current High in Hi-Z state	OE=L	-10	-	+10	uA
IOZL	Output Leak Current Low in Hi-Z state	OE=L	-10	-	+10	uA
IIH	Input Leak Current High		-10	-	+10	uA
IIL	Input Leak Current Low		-10	-	+10	uA

VCC=3.3±0.3V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	2.0	-	VCC	V
		I3L	2.1	-	VCC	V
VIL	Low Level Input Voltage	I3	0	-	0.8	V
		I3L	0	-	0.7	V
VOH	High Level Output Voltage CMOS Output buffer	TTLDRV=L,IOH=-4mA	2.4	-	VCC	V
		TTLDRV=H,IOH=-8mA				
VOL	Low Level Output Voltage Open Drain Output buffer	IOL=2mA	-	-	0.2	V
	Low Level Output Voltage CMOS Output buffer	TTLDRV=L, IOL=4mA	-	-	0.4	
		TTLDRV=H, IOL=8mA	-	-	0.4	

VCC=2.8±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	1.8	-	VCC	V
		I3L	1.9	-	VCC	V
VIL	Low Level Input Voltage	I3	0	-	0.7	V
		I3L	0	-	0.6	V
VOH	High Level Output Voltage CMOS Output buffer	TTLDRV=L,IOH=-2mA	2.0	-	VCC	V
		TTLDRV=H,IOH=-4mA				
VOL	Low Level Output Voltage Open Drain Output buffer	IOL=2mA	-	-	0.2	V
	Low Level Output Voltage CMOS Output buffer	TTLDRV=L, IOL=2mA	-	-	0.4	
		TTLDRV=H, IOL=4mA	-	-	0.4	

VCC=2.5±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
VIH	High Level Input Voltage	I3	1.7	-	VCC	V
		I3L	1.6	-	VCC	V
VIL	Low Level Input Voltage	I3	0	-	0.7	V
		I3L	0	-	0.5	V
VOH	High Level Output Voltage CMOS Output buffer	TTLDRV=L,IOH=-2mA	2.0	-	VCC	V
		TTLDRV=H,IOH=-4mA				
VOL	Low Level Output Voltage Open Drain Output buffer	IOL=2mA	-	-	0.2	V
	Low Level Output Voltage CMOS Output buffer	TTLDRV=L, IOL=2mA	-	-	0.4	
		TTLDRV=H, IOL=4mA	-	-	0.4	

CML DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
VRTH	CML Differential Input High Threshold		-	-	50	mV
VRTL	CML Differential Input Low Threshold		-50	-	-	mV
IRIH	CML Input Leak Current High	PDN=L, RXP/N=1.2V	-	-	±15	uA
IRIL	CML Input Leak Current Low	PDN=L, RXP/N=GND	-	-	±15	uA
IRRIH	CML Input Current High	RXP/N=1.2V	-	-	1.6	mA
IRRIL	CML Input Current Low	RXP/N=GND	-4.6	-	-	mA
RRIN	CML Differential Input Resistance		80	100	120	Ω

AC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

symbol	Parameter	conditions	min.	typ.	max.	Unit
tRBIT	Unit Interval		267	-	1666	psec
tRCP	CLKOUT Period	COL=H, LFSEL=L	8	-	50	ns
		COL=H, LFSEL=H	25	-	100	ns
		COL=L, LFSEL=L	10.67	-	66.66	ns
		COL=L, LFSEL=H	33.34	-	133.33	ns
tRCH	CLKOUT High Time		-	tRCP/2	-	ns
tRCL	CLKOUT Low Time		-	tRCP/2	-	ns
tDOUT	TTL Data OUT Period		-	tRCP	-	ns
tRDC	Input Data to Output Clock Delay	COL=H	-	13.0tRCP+3.5	-	ns
		COL=L	-	12.4tRCP+3.5	-	ns
tRPD	Power On to PDN High Delay		0	-	-	ns
tRHPD0	PDN High to HTPDN Low Delay		-	-	10	ms
tRHPD1	PDN Low to HTPDN High Delay		-	-	10	us
tRPLL0	Training Pattern Input to LOCKN Low Delay		-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay		-	-	10	us
tRLCK0	LOCKN Low to TTL Output Delay		-	-	5	ms
tRLCK1	LOCKN High to TTL Low-fixed Delay		-	-	0	ns

VCC=3.3±0.3V

symbol	Parameter	conditions	min.	typ.	max.	Unit
tRS	TTL Data Setup to CLKOUT	TTLDRV=L	0.45tRCP-2.0	-	-	ns
		TTLDRV=H	0.45tRCP-1.5	-	-	ns
tRH	TTL Data Hold to CLKOUT	TTLDRV=L	0.45tRCP-2.0	-	-	ns
		TTLDRV=H	0.45tRCP-1.5	-	-	ns
tTLH	TTL Low to High Transition Time	Clock TTLDRV=L	-	1.0	2.0	ns
		Data TTLDRV=L	-	2.0	3.6	ns
		Clock TTLDRV=H	-	0.8	1.6	ns
		Data TTLDRV=H	-	1.6	2.4	ns
tTHL	TTL High to Low Transition Time	Clock TTLDRV=L	-	1.0	2.0	ns
		Data TTLDRV=L	-	2.0	3.6	ns
		Clock TTLDRV=H	-	0.8	1.6	ns
		Data TTLDRV=H	-	1.6	2.4	ns

VCC=2.8±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
tRS	TTL Data Setup to CLKOUT	TTLDRV=L	0.45tRCP-2.5	-	-	ns
		TTLDRV=H	0.45tRCP-2.0	-	-	ns
tRH	TTL Data Hold to CLKOUT	TTLDRV=L	0.45tRCP-2.5	-	-	ns
		TTLDRV=H	0.45tRCP-2.0	-	-	ns
tTLH	TTL Low to High Transition Time	Clock TTLDRV=L	-	1.2	2.4	ns
		Data TTLDRV=L	-	2.4	4.2	ns
		Clock TTLDRV=H	-	0.8	2.2	ns
		Data TTLDRV=H	-	1.6	2.8	ns
tTHL	TTL High to Low Transition Time	Clock TTLDRV=L	-	1.2	2.4	ns
		Data TTLDRV=L	-	2.4	4.2	ns
		Clock TTLDRV=H	-	0.8	2.2	ns
		Data TTLDRV=H	-	1.6	2.8	ns

VCC=2.5±0.2V

symbol	Parameter	conditions	min.	typ.	max.	Unit
tRS	TTL Data Setup to CLKOUT	TTLDRV=L	0.45tRCP-2.5	-	-	ns
		TTLDRV=H	0.45tRCP-2.0	-	-	ns
tRH	TTL Data Hold to CLKOUT	TTLDRV=L	0.45tRCP-2.5	-	-	ns
		TTLDRV=H	0.45tRCP-2.0	-	-	ns
tTLH	TTL Low to High Transition Time	Clock TTLDRV=L	-	1.2	2.4	ns
		Data TTLDRV=L	-	2.4	4.2	ns
		Clock TTLDRV=H	-	0.8	2.2	ns
		Data TTLDRV=H	-	1.6	2.8	ns
tTHL	TTL High to Low Transition Time	Clock TTLDRV=L	-	1.2	2.4	ns
		Data TTLDRV=L	-	2.4	4.2	ns
		Clock TTLDRV=H	-	0.8	2.2	ns
		Data TTLDRV=H	-	1.6	2.8	ns

AC Timing Diagrams and Test Circuits

CMOS/TTL Output Switching Characteristics

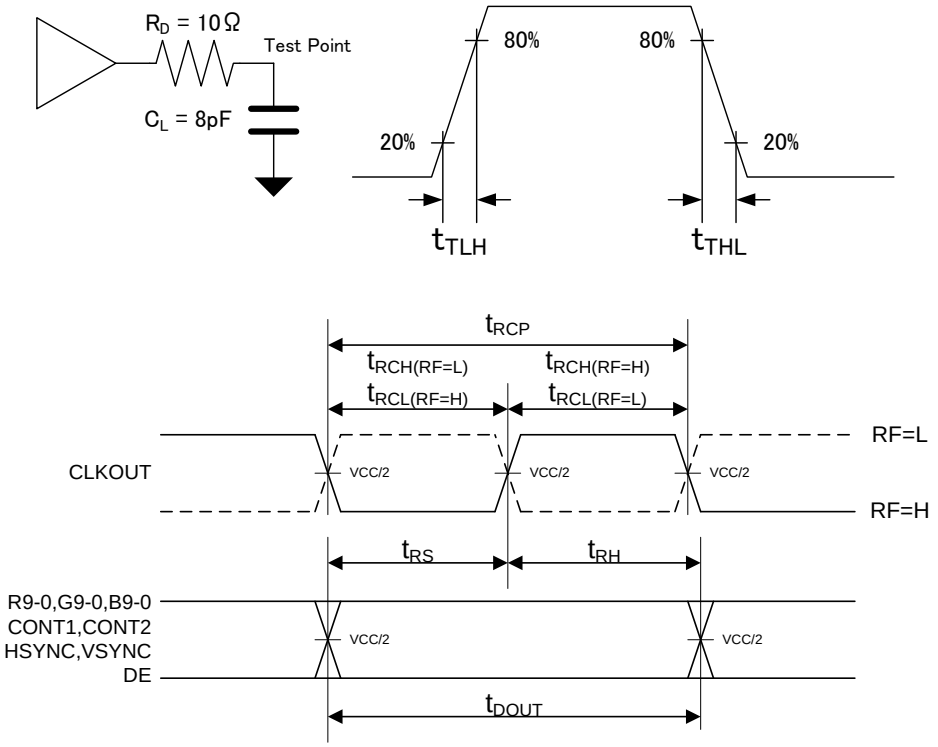


Figure 6. CMOS/TTL Output Switching Timing Diagrams and Test Circuit

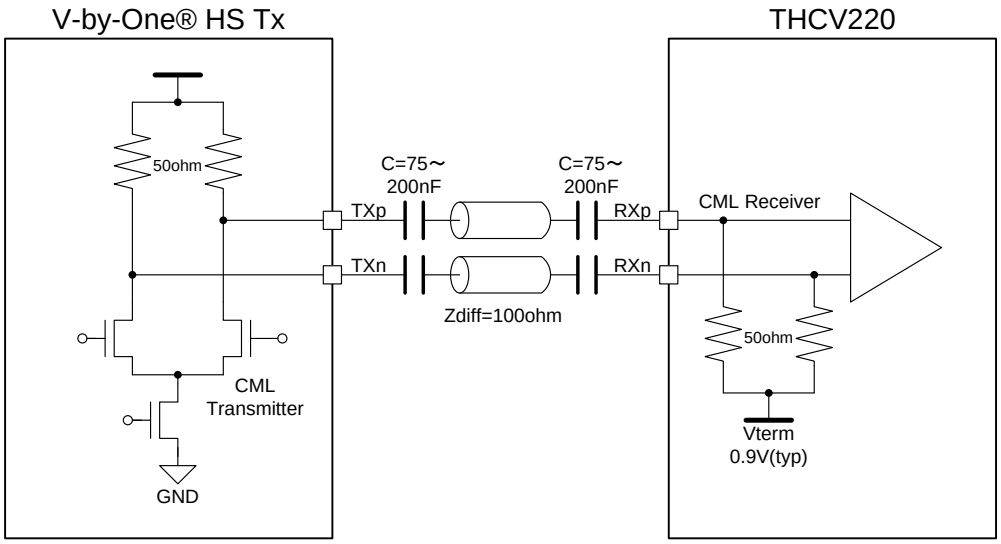


Figure 7. CML buffer scheme

Latency Characteristics

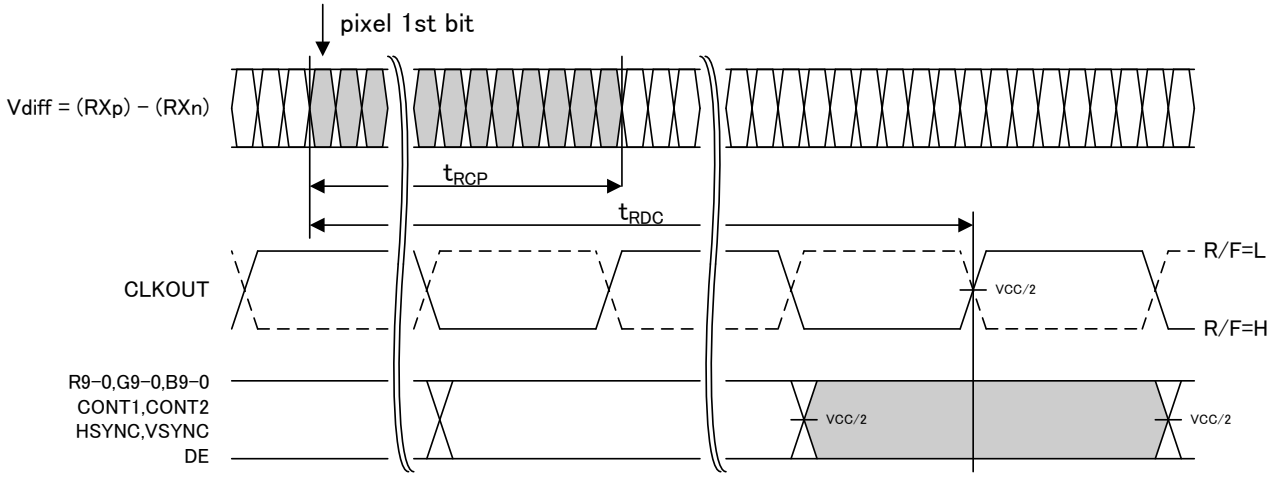


Figure 8. THCV220 Latency

Lock and Unlock Sequence

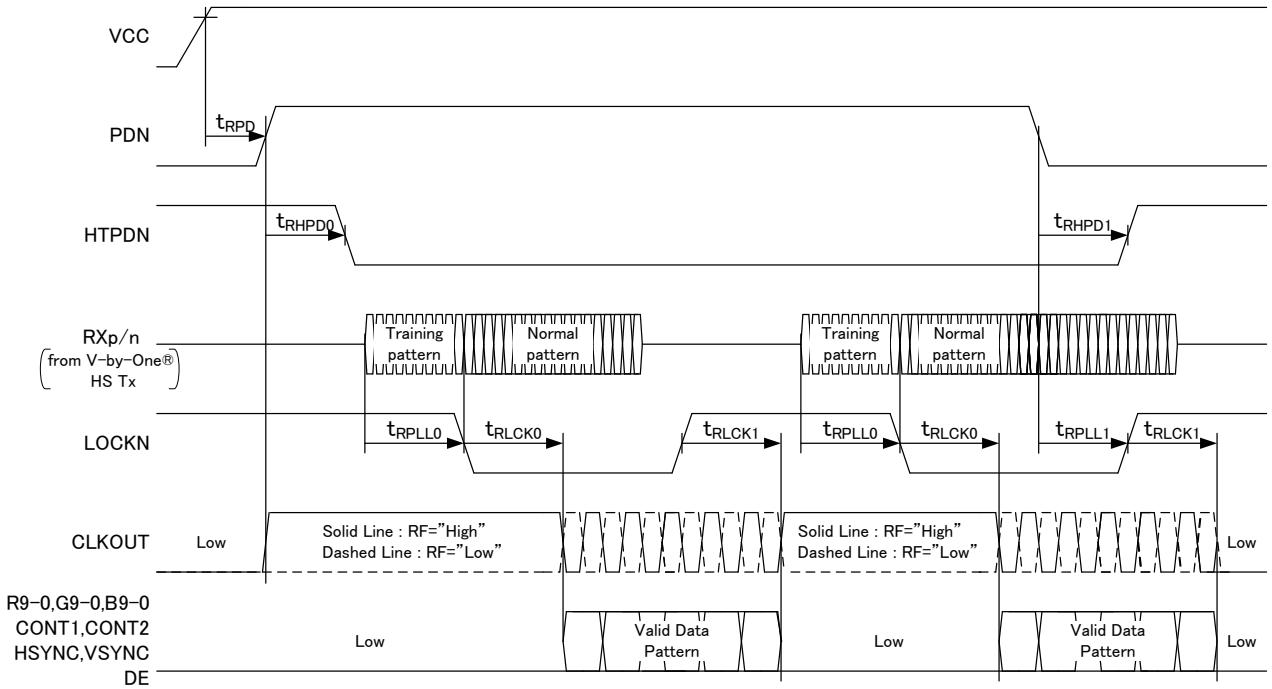


Figure 9. THCV220 Sequence

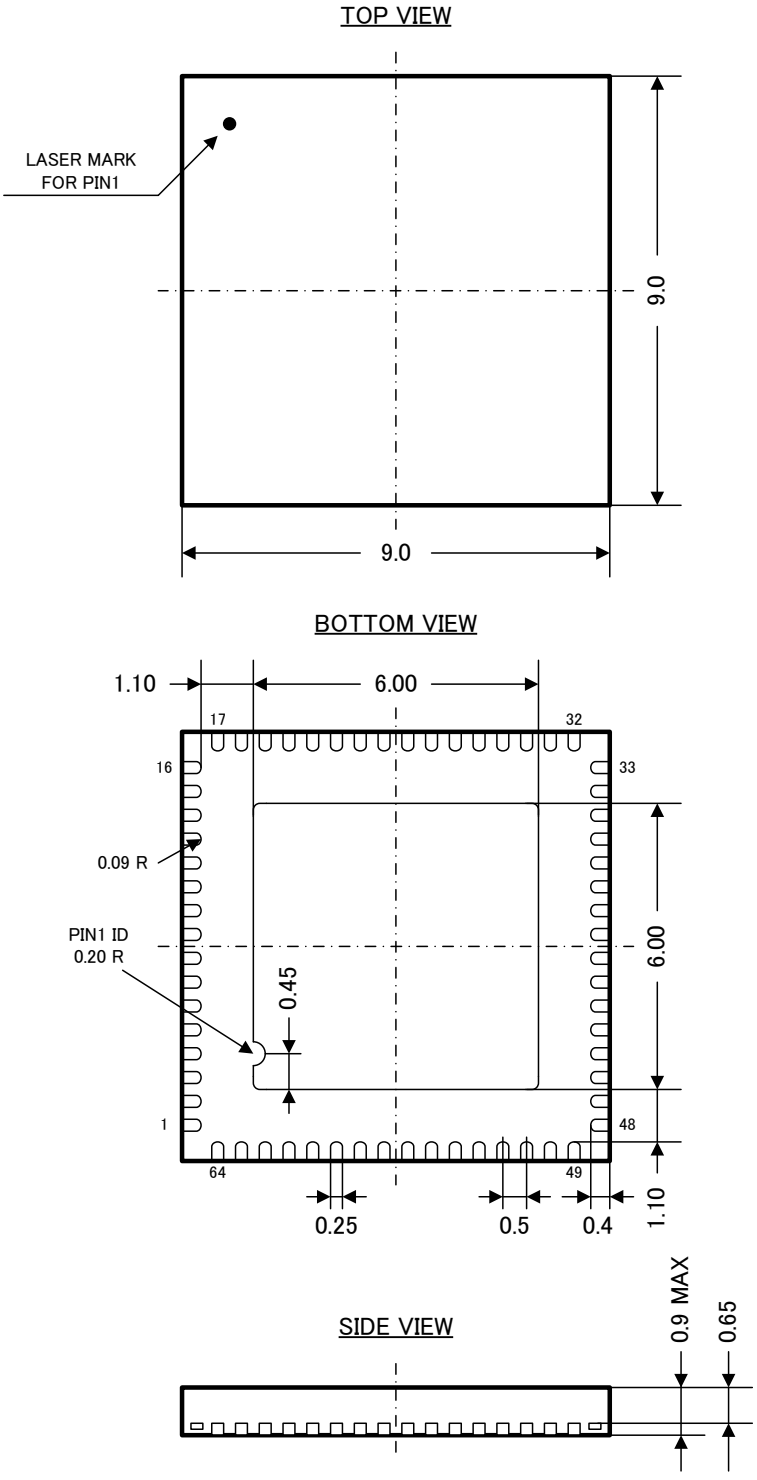
Data Mapping

Table 8. CMOS/TTL Output Data Mapping

Data Signals		Receiver Output Pin Name		Symbol defined by V-by-One® HS
10bit (30bpp)	8bit (24bpp)	10bit (30bpp)	8bit (24bpp)	
R0 *1	-	R0	-	D30
R1 *1	-	R1	-	D31
R2	R0	R2	R2	D0
R3	R1	R3	R3	D1
R4	R2	R4	R4	D2
R5	R3	R5	R5	D3
R6	R4	R6	R6	D4
R7	R5	R7	R7	D5
R8	R6	R8	R8	D6
R9	R7	R9	R9	D7
G0 *1	-	G0	-	D28
G1 *1	-	G1	-	D29
G2	G0	G2	G2	D8
G3	G1	G3	G3	D9
G4	G2	G4	G4	D10
G5	G3	G5	G5	D11
G6	G4	G6	G6	D12
G7	G5	G7	G7	D13
G8	G6	G8	G8	D14
G9	G7	G9	G9	D15
B0 *1	-	B0	-	D26
B1 *1	-	B1	-	D27
B2 *1	B0 *1	B2	B2	D16
B3 *1	B1 *1	B3	B3	D17
B4 *1	B2 *1	B4	B4	D18
B5 *1	B3 *1	B5	B5	D19
B6 *1	B4 *1	B6	B6	D20
B7 *1	B5 *1	B7	B7	D21
B8 *1	B6 *1	B8	B8	D22
B9 *1	B7 *1	B9	B9	D23
CONT1 *1	-	CONT1	-	D25
CONT2 *1	-	CONT2	-	D24
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE

*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

Package



Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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4. THINE ACCEPTS NO LIABILITY FOR ANY DAMAGE OR LOSS IN CONNECTION WITH ANY DISPUTE RELATING TO INTELLECTUAL PROPERTY RIGHTS BETWEEN THE USER AND ANY THIRD PARTY, ARISING OUT OF THIS PRODUCT, EXCEPT FOR SUCH DAMAGE OR LOSS IN CONNECTION WITH DISPUTES SUCCESSFULLY PROVED BY THE USER THAT SUCH DISPUTES ARE DUE SOLELY TO THINE. NOTE, HOWEVER, EVEN IN THE AFOREMENTIONED CASE, THINE ACCEPTS NO LIABILITY FOR SUCH DAMAGE OR LOSS IF THE DISPUTE IS CAUSED BY THE USER'S INSTRUCTION.

5. This product is not designed for applications that require extremely high-reliability/safety such as aerospace device, nuclear power control device, or medical device related to critical care, excluding when this product is specified for automotive use by THine and used it for that purpose. THine accepts no liability whatsoever for any damages, claims or losses arising out of the uses set forth above.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently fail-safe design principles such as redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

10. This product must be stored according to storage method which is specified in this specifications. THine accepts no liability whatsoever for any damage or loss caused to the user due to any storage not according to above-mentioned method.

11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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