



THCV217 and THCV218

V-by-One® HS High-speed Video Data Transmitter and Receiver

General Description

THCV217 and THCV218 are designed to support video data transmission between the host and display.

One high-speed lane can carry up to 32bit data and 3 bits of synchronizing signals at a pixel clock frequency from 20MHz to 85MHz.

The chipset, which has two high-speed data lanes, can transmit video data up to 1080p/10b/60Hz. The maximum serial data rate is 3.4Gbps/lane.

Features

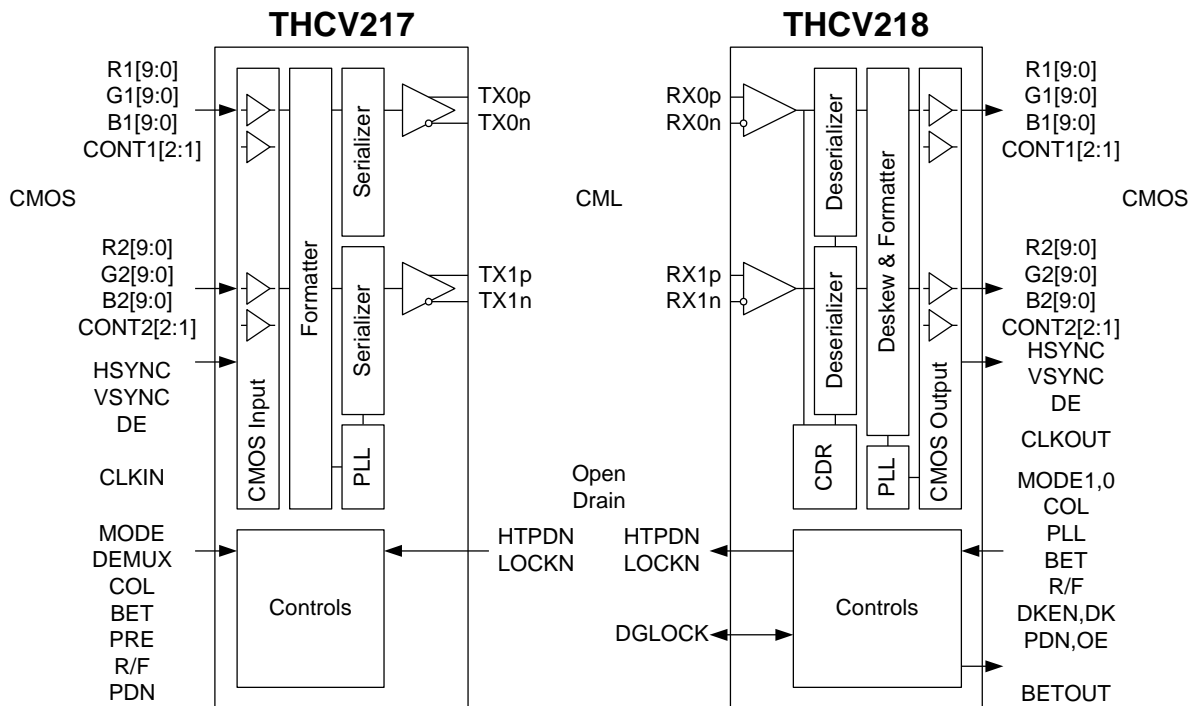
- Color depth selectable: 24(8×3)/32(10×3)bit
- Single-in/Single-out, Single-in/Dual-out, and Dual-in/Dual-out selectable for THCV217
- Single-in/Single-out, Dual-in/Single-out, and Dual-in/Dual-out selectable for THCV218
- AC coupling for high-speed lines

- CORE 1.8V, CMOS IO 3.3V
- Package: 217(TFBGA105), 218(TFBGA145)
- Wide frequency range
- CDR requires no external frequency reference
- Spread Spectrum Clocking tolerant
Up to 30kHz / ±0.5% (center spread)
- V-by-One® HS standard Version1.4 compliant.

| Product | Link | Pixel Clock Frequency |
|---------|-------|-----------------------|
| THCV217 | Si/So | 20MHz to 85MHz |
| | Di/Do | |
| | Si/Do | 40MHz to 170MHz |
| THCV218 | Si/So | 20MHz to 85MHz |
| | Di/Do | |
| | Di/So | 40MHz to 170MHz |

Si/So: Single-in/Single-out, Di/Do: Dual-in/Dual-out
Di/So: Dual-in/Single-out, Si/Do: Single-in/Dual-out

Block Diagram



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Pin Configuration
THCV217

TOP VIEW

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | | | |
|-----|-----|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------|------|-------|-------|-------|-------|-----|-----|-----|-----|-----|-----|-------|--------|--------|---|
| A | B10 | B11 | G18 | G16 | G14 | G12 | G10 | R18 | R16 | R14 | R12 | A | | | | | | | | | |
| B | B12 | B13 | G19 | G17 | G15 | G13 | G11 | R19 | R17 | R15 | R13 | B | | | | | | | | | |
| C | B14 | B15 | DVDH | GND | GND | VDL | VDL | HTPDN | LOCKN | R11 | R10 | C | | | | | | | | | |
| D | B16 | B17 | DVDH | <table border="1" style="margin: auto;"> <tr> <td>GND</td> <td>GND</td> <td>GND</td> </tr> <tr> <td>GND</td> <td>GND</td> <td>GND</td> </tr> <tr> <td>GND</td> <td>GND</td> <td>GND</td> </tr> </table> | | | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | CAVDL | CONT11 | CONT12 | D |
| GND | GND | GND | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | | | | | | | | | | | | | | | | | | | |
| E | B18 | B19 | DVDH | CAVDL | TX0n | TX0p | E | | | | | | | | | | | | | | |
| F | R20 | R21 | R/F | CAVDL | TX1n | TX1p | F | | | | | | | | | | | | | | |
| G | R22 | R23 | PRE | CPVDL | CONT21 | CONT22 | G | | | | | | | | | | | | | | |
| H | R24 | R25 | COL | PDN | B29 | B28 | H | | | | | | | | | | | | | | |
| J | R26 | R27 | GND | DVDH | DEMUX | Reserved 0 | MODE | DVDH | BET | CLKIN | DE | J | | | | | | | | | |
| K | R28 | R29 | G23 | G25 | G27 | G29 | B21 | B23 | B25 | B27 | VSYNC | K | | | | | | | | | |
| L | G20 | G21 | G22 | G24 | G26 | G28 | B20 | B22 | B24 | B26 | HSYNC | L | | | | | | | | | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | | | |

THCV218

TOP VIEW

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|------------|------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|----------|------|------|------|------|-----|-----|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|----------|
| A | HSYNC | B19 | B17 | B15 | B13 | B11 | G19 | G17 | G15 | G13 | G11 | G10 | R19 | A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | DE | VSYNC | B18 | B16 | B14 | B12 | B10 | G18 | G16 | G14 | G12 | R18 | R17 | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | CONT11 | CONT12 | Reserved 4 | Reserved 1 | VDL | VDL | DVDH | DVDH | DVDH | DVDH | DVDH | R16 | R15 | C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | HTPDN | LOCKN | Reserved 3 | <table border="1" style="margin: auto;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> | | | | | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDH | R14 | R13 | D |
| GND | GND | GND | GND | | | | | | | | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | | | | | | | | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | GND | GND | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | BETOUT | Reserved 5 | CAVDL | DVDH | R12 | R11 | E | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | RX0n | RX0p | CAVDL | DVDH | DVDH | R10 | F | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | Reserved 6 | Reserved 7 | CAVDL | GND | GND | CLKOUT | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | RX1n | RX1p | CAVDL | DVDH | CONT22 | CONT21 | H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | MODE1 | BET | CAVDL | DVDH | B29 | B28 | J | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | PLL | MODE0 | DK | DVDH | B27 | B26 | K | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | PDN | OE | COL | DKEN | VDL | VDL | DVDH | DVDH | DVDH | DVDH | DVDH | B25 | B24 | L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | R/F | R21 | R23 | R25 | R27 | R29 | G21 | G23 | G25 | G27 | G29 | B23 | B22 | M | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | DGLOCK | R20 | R22 | R24 | R26 | R28 | G20 | G22 | G24 | G26 | G28 | B21 | B20 | N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Pin Description

THCV217

THCV217 Pin Description

| Name | Ball # | Type* | Description |
|-----------|---------------------------------------------|-------|---------------------------------------------------------------------------------------|
| TX0n,TX0p | E10,E11 | CO | CML output for Lane0 |
| TX1n,TX1p | F10,F11 | CO | CML output for Lane1. Must be left OPEN when not used. |
| R19-R10 | B8,A8,B9,A9, B10,A10,B11, A11,C10,C11 | I3 | 1st pixel data inputs |
| G19-G10 | B3,A3,B4,A4, B5,A5,B6, A6,B7,A7 | I3 | 1st pixel data inputs |
| B19-B10 | E2,E1,D2,D1, C2,C1,B2, B1,A2,A1 | I3 | 1st pixel data inputs |
| CONT11,12 | D10,D11 | I3 | User defined data inputs, serialized with 1st pixel data. Active only in 10bit mode. |
| R29-R20 | K2,K1,J2,J1, H2,H1,G2, G1,F2,F1 | I3 | 2nd pixel data inputs |
| G29-G20 | K6,L6,K5,L5, K4,L4,K3, L3,L2,L1 | I3 | 2nd pixel data inputs |
| B29-B20 | H10,H11,K10, L10,K9,L9, K8,L8,K7,L7 | I3 | 2nd pixel data inputs |
| CONT21,22 | G10,G11 | I3 | User defined data inputs, serialized with 2nd pixel data. Active only in 10bit |
| DE | J11 | I3 | DE input |
| HSYNC | L11 | I3 | Hsync input |
| VSYNC | K11 | I3 | Vsync input |
| CLKIN | J10 | I3 | Pixel clock input |
| HTPDN | C8 | I3L | Hot plug detect input. Must be connected to Rx HTPDN with a 10kΩ pull-up resistor. |
| LOCKN | C9 | I3L | Lock detect input. Must be connected to Rx LOCKN with a 10kΩ pull-up resistor. |

*type symbol

CO=CML Output

I3=3.3V CMOS input, I3L=Low speed 3.3V CMOS input

O3=3.3V CMOS output

P=1.8V power supply, P3=3.3V power supply

THCV217 Pin Description (Continued)

| Name | Ball # | Type* | Description |
|-----------|-----------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| PDN | H9 | I3 | Power down input H: Normal operation L: Power Down |
| COL | H3 | I3 | Color depth select input H: 8bit mode L: 10bit mode |
| PRE | G3 | I3 | Pre emphasis level select input H: 100% L: 0% |
| BET | J9 | I3L | Field BET enable H: Enable L: Normal Operation |
| DEMUX | J5 | I3 | Operation mode select input DEMUX,MODE=HH: Reserved (Forbidden) HL: Single-in/Dual-out LH: Single-in/Single-out LL: Dual-in/Dual-out |
| MODE | J7 | I3L | |
| R/F | F3 | I3 | Input clock triggering edge select input for latching input data H: Rising edge L: Falling edge |
| Reserved0 | J6 | I3 | Reserved Inputs. Must be tied to GND |
| VDL | C6,C7 | P | 1.8V power supply pins for digital circuitry |
| CAVDL | D9,E9,F9 | P | 1.8V power supply pins for CML outputs |
| CPVDL | G9 | P | 1.8V power supply pins for PLL circuitry |
| DVDH | C3,D3,E3,J4,J8 | P3 | 3.3V power supply pins for TTL inputs |
| GND | C4,C5,E5,E6,E7,F5, F6,F7,G5,G6,G7,J3 | GND | Ground pins |

*type symbol

CO=CML Output

I3=3.3V CMOS input, I3L=Low speed 3.3V CMOS input

O3=3.3V CMOS output

P=1.8V power supply, P3=3.3V power supply

THCV218

THCV218 Pin Description

| PIN Name | Ball # | Type* | Description |
|-----------|-------------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| RX0n,RX0p | F1,F2 | CI | CML input for Lane0 |
| RX1n,RX1p | H1,H2 | CI | CML input for Lane1. Must be left OPEN when not used. |
| R19-R10 | A13,B12,B13, C12,C13,D12, D13,E12,E13,F13 | O3 | 1st pixel data outputs |
| G19-G10 | A7,B8,A8,B9, A9,B10,A10, B11,A11,A12 | O3 | 1st pixel data outputs |
| B19-B10 | A2,B3,A3,B4, A4,B5,A5, B6,A6,B7 | O3 | 1st pixel data outputs |
| CONT11,12 | C1,C2 | O3 | User defined data outputs. Active only in 10bit mode. |
| R29-R20 | M6,N6,M5,N5, M4,N4,M3, N3,M2,N2 | O3 | 2nd pixel data outputs |
| G29-G20 | M11,N11,M10, N10,M9,N9, M8,N8,M7,N7 | O3 | 2nd pixel data outputs |
| B29-B20 | J12,J13,K12, K13,L12,L13, M12,M13,N12,N13 | O3 | 2nd pixel data outputs |
| CONT21,22 | H13,H12 | O3 | User defined data outputs. Active only in 10bit mode. |
| DE | B1 | O3 | DE Output |
| VSYNC | B2 | O3 | Vsync Output |
| HSYNC | A1 | O3 | Hsync Output |
| CLKOUT | G13 | O3 | Pixel clock output |
| HTPDN | D1 | OD3 | Hot plug detect output. Must be connected to Tx HTPDN with a 10kW pull-up resistor. Hi-Z : when PDN=L, L: when PDN=H |
| LOCKN | D2 | OD3 | Lock detect output. Must be connected to Tx LOCKN with a 10kW pull-up resistor. It drives Low when the CDR locks to the incoming data. |
| PDN | L1 | I3 | Power down input H: Normal operation L: Power Down |
| COL | L3 | I3 | Color depth select input H: 8bit mode L: 10bit mode |
| BET | J2 | I3L | Field BET enable H: Enable L: Normal Operation When BET=High. Reserved7 must be Low. |
| MODE1,0 | J1,K2 | I3 | Operation mode select input HH: Reserved (Forbidden) HL: Single-in/Single-out LH: Dual-in/Single-out LL: Dual-in/Dual-out |

*type symbol

CI=CML Input, OD3=3.3V Open drain output, O3=3.3V CMOS output

I3=3.3V CMOS input, I3L=Low speed 3.3V CMOS input, I3PU=3.3V CMOS inout with an on-chip pullup resistor

P=1.8v power supply, P3=3.3v power supply

THCV218 Pin Description (Continued)

| PIN Name | Ball # | Type* | Description |
|----------------|----------------------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLL | K1 | I3 | PLL bandwidth select H: CLKIN<40MHz, when SiSo,DiDo L: Normal Operation |
| OE | L2 | I3 | Output enable input (See Table 1 for details) H: All CMOS outputs enabled L: All CMOS outputs disabled, except for LOCKN, HTPDN |
| DGLOCK | N1 | I3PU | Connect all DGLOCK pins in multiple-chip configuration. Must be left OPEN for single-chip configuration. |
| R/F | M1 | I3 | Output clock triggering edge select input H: Rising edge L: Falling edge |
| DKEN | L4 | I3 | DK enable H: DK enabled L: DK disabled (Default) |
| DK | K3 | I3 | Output clock delay timing select input. Enabled by DKEN. H: Late L: Early Refer to Figure 10 for details. |
| BETOUT | E1 | O3 | Field BET result output. Must be left OPEN when NOT used. |
| Reserved7 | G2 | I3 | CTL bit transmission on DE=low blanking period enable H: CTL bit enabled (CTL are transmitted except the 1st and the last pixel of DE=Low) L: CTL bit disabled (CTL are Low fixed during DE=Low) When BET=High, Reserved7 must be Low. |
| Reserved3 | D3 | O3 | Reserved outputs. Must be left OPEN. |
| Reserved1, 4-6 | C4,C3,E2,G1 | I3 | Reserved input. Must be tied to GND |
| VDL | C5,C6,L5,L6 | P | 1.8V power supply pins for digital circuitry |
| CAVDL | E3,F3,G3,H3,J3 | P | 1.8V power supply pins for CML inputs and PLL circuitry |
| DVDH | C7,C8,C9,C10,C11, D11,E11,F11,F12, H11,J11,K11,L7, L8,L9,L10,L11 | P3 | 3.3V power supply pins for TTL outputs |
| GND | E5,E6,E7,E8,E9,F5, F6,F7,F8,F9,G5,G6, G7,G8,G9,G11, G12,H5,H6,H7,H8, H9,J5,J6,J7,J8,J9 | GND | Ground pins |

*type symbol
 CI=CML Input, OD3=3.3V Open drain output, O3=3.3V CMOS output
 I3=3.3V CMOS input, I3L=Low speed 3.3V CMOS input, I3PU=3.3V CMOS inout with an on-chip pullup resistor
 P=1.8V power supply, P3=3.3V power supply

| PDN | OE | R/G/B/CONT H,Vsync,DE,CLKOUT |
|-----|----|---------------------------------|
| L | L | Hi-Z |
| L | H | All Low |
| H | L | Hi-Z |
| H | H | Data Out |

Table 1. Output Control

Functional Description

Functional Overview

With V-by-One[®]HS's proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV217 and THCV218 enable transmission of 8/10 bit RGB, 2bits of user-defined data (CONT), synchronizing signals HSYNC, VSYNC, and DE by single/dual differential pair cable with minimal external components.

THCV217, the transmitter, inputs CMOS data (including video data, CONT, HSYNC, VSYNC, and DE) and serializes video data and synchronizing signals separately, depending on the polarity of DE. DE is a signal which indicates whether video or synchronizing data are active. When DE is high, it serializes video data inputs into differential data streams. And it transmits serialized synchronizing data when DE is low.

Figure 1 is the conceptual diagram of the basic operation of the chipset.

THCV218, the receiver, automatically extracts the clock from the incoming data streams and converts the serial data into video data with DE being high or synchronizing data with DE being low, recognizing which type of serial data is being sent by the transmitter. And it outputs the recovered data in the form of CMOS data.

THCV218 can operate for a wide range of a serial bit rate from 600Mbps to 3.4Gbps/channel.

Figure 2 shows the timing diagram of the basic operation of the chipset.

It does not need any external frequency reference, such as a crystal oscillator.

Data Enable

There are some requirements for DE signal as described in Figure 1, Figure 2, and Table 18.

If DE=Low, control data of same cycle and possibly particular assigned data bit 'CTL' except the first and the last pixel are transmitted. Otherwise video data are transmitted during DE=High.

Control data from receiver in DE=High period are previous data of DE transition. See Figure 2.

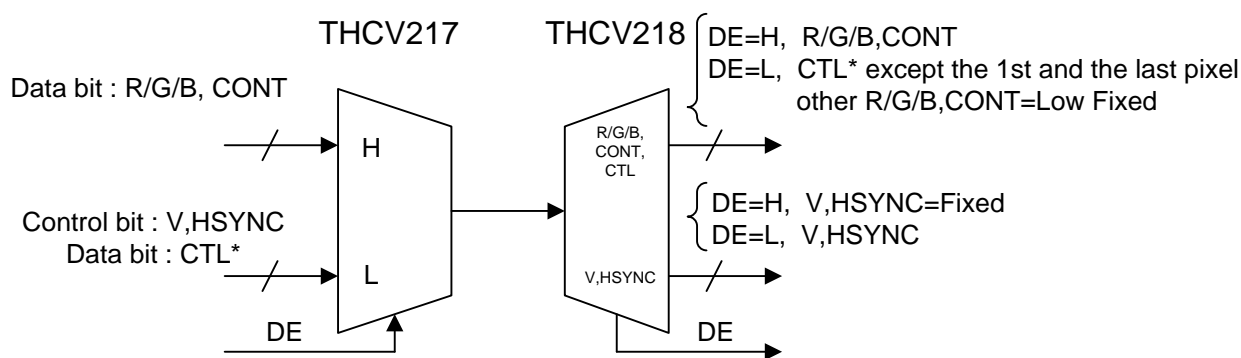
The length of DE being low and high is at least 2 clock cycles long, as described in Table 18.

Data Enable must be toggled like High -> Low -> High at regular interval.

CTL bit transmission

There are particular assigned data bit 'CTL' which can be transmitted both on DE=High and on DE=Low except the first and the last pixel on DE=Low.

This function is enabled by setting THCV218 Reserved7 pin to High.



*CTL are particular assigned bit among R/G/B, CONT that can carry arbitrary data during DE=Low period.

*CTL bit transmission is activated by setting THCV218 Reserved7 pin to High.

Figure 1. Conceptual diagram of the basic operation of the chipset

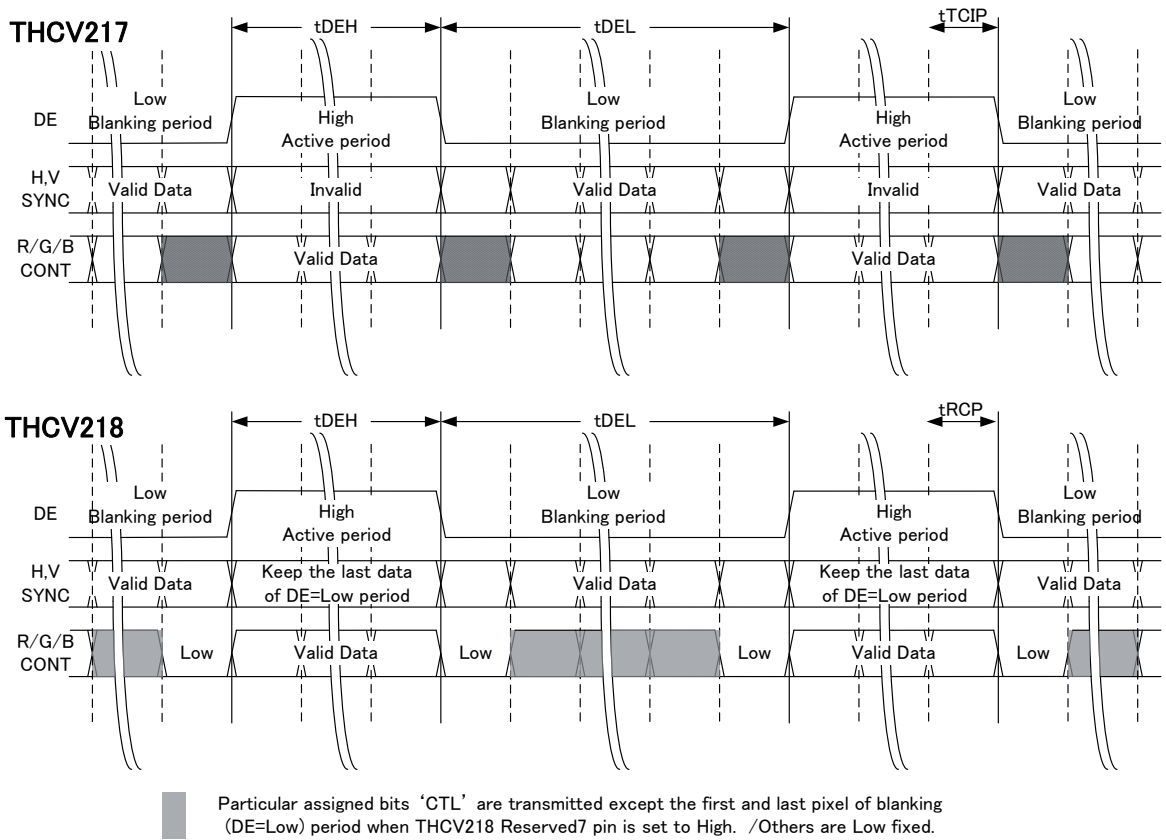
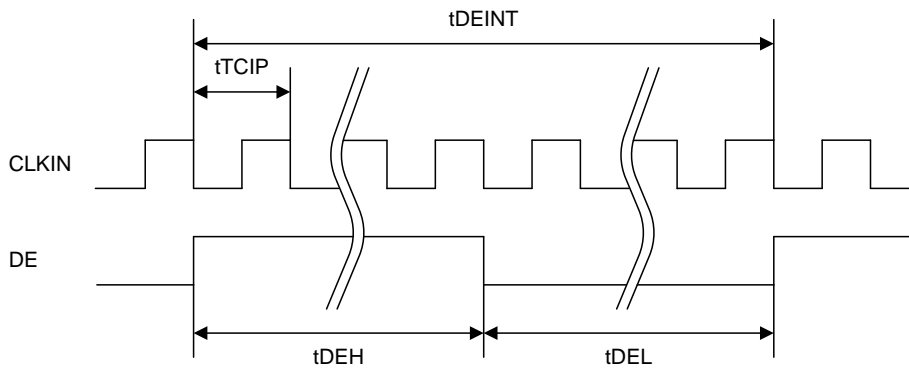


Figure 2. Data and synchronizing signals transmission timing diagram



Note: The period between rising edges of DE(tDEINT),high time of DE(tDEH) should always satisfy following equations.

$$tDEH = tTCIP \times (2m)$$

$$tDEINT = tTCIP \times (2n)$$

$$tDEL \geq 4tTCIP \text{ (This } tDEL \text{ rule is only in SiDo mode.)}$$

m,n = positive integer, m≠n

Requirement for DE minimum length limitation is described in Table 18.

Figure2-1. DE input timing

Operation Mode and Color Depth Mode function

THCV217 and 218 support a variety of operation modes to optimize power consumption, number of PCB traces, or signal integrity. Refer to Table 2, Table 3, and Figure 3 for details.

| COL | DEMUX | MODE | Description | CMOS Input | | CML Output | |
|-----|-------|------|----------------------------|---------------|-----------|-----------------|------------|
| | | | | CLKIN Range | # of data | TX0/1 Range | # of lanes |
| L | L | L | 10bit Dual-in/Dual-out | 20 to 85 MHz | (32+3)×2 | 0.8 to 3.4Gbps | 2 |
| L | L | H | 10bit Single-in/Single-out | 20 to 85 MHz | (32+3)×1 | 0.8 to 3.4Gbps | 1 |
| L | H | L | 10bit Single-in/Dual-out | 40 to 170 MHz | (32+3)×1 | 0.8 to 3.4Gbps | 2 |
| L | H | H | Reserved (Forbidden) | - | - | - | - |
| H | L | L | 8bit Dual-in/Dual-out | 20 to 85 MHz | (24+3)×2 | 0.6 to 2.55Gbps | 2 |
| H | L | H | 8bit Single-in/Single-out | 20 to 85 MHz | (24+3)×1 | 0.6 to 2.55Gbps | 1 |
| H | H | L | 8bit Single-in/Dual-out | 40 to 170 MHz | (24+3)×1 | 0.6 to 2.55Gbps | 2 |
| H | H | H | Reserved (Forbidden) | - | - | - | - |

Table 2. THCV217 operation mode select

| COL | MODE1 | MODE0 | Description | CML Input | | CMOS Output | |
|-----|-------|-------|----------------------------|-----------------|------------|---------------|-----------|
| | | | | RX0/1 Range | # of lanes | CLKOUT Range | # of data |
| L | L | L | 10bit Dual-in/Dual-out | 0.8 to 3.4Gbps | 2 | 20 to 85 MHz | (32+3)×2 |
| L | L | H | 10bit Dual-in/Single-out | 0.8 to 3.4Gbps | 2 | 40 to 170 MHz | (32+3)×1 |
| L | H | L | 10bit Single-in/Single-out | 0.8 to 3.4Gbps | 1 | 20 to 85 MHz | (32+3)×1 |
| L | H | H | Reserved (Forbidden) | - | - | - | - |
| H | L | L | 8bit Dual-in/Dual-out | 0.6 to 2.55Gbps | 2 | 20 to 85 MHz | (24+3)×2 |
| H | L | H | 8bit Dual-in/Single-out | 0.6 to 2.55Gbps | 2 | 40 to 170 MHz | (24+3)×1 |
| H | H | L | 8bit Single-in/Single-out | 0.6 to 2.55Gbps | 1 | 20 to 85 MHz | (24+3)×1 |
| H | H | H | Reserved (Forbidden) | - | - | - | - |

Table 3. THCV218 operation mode select

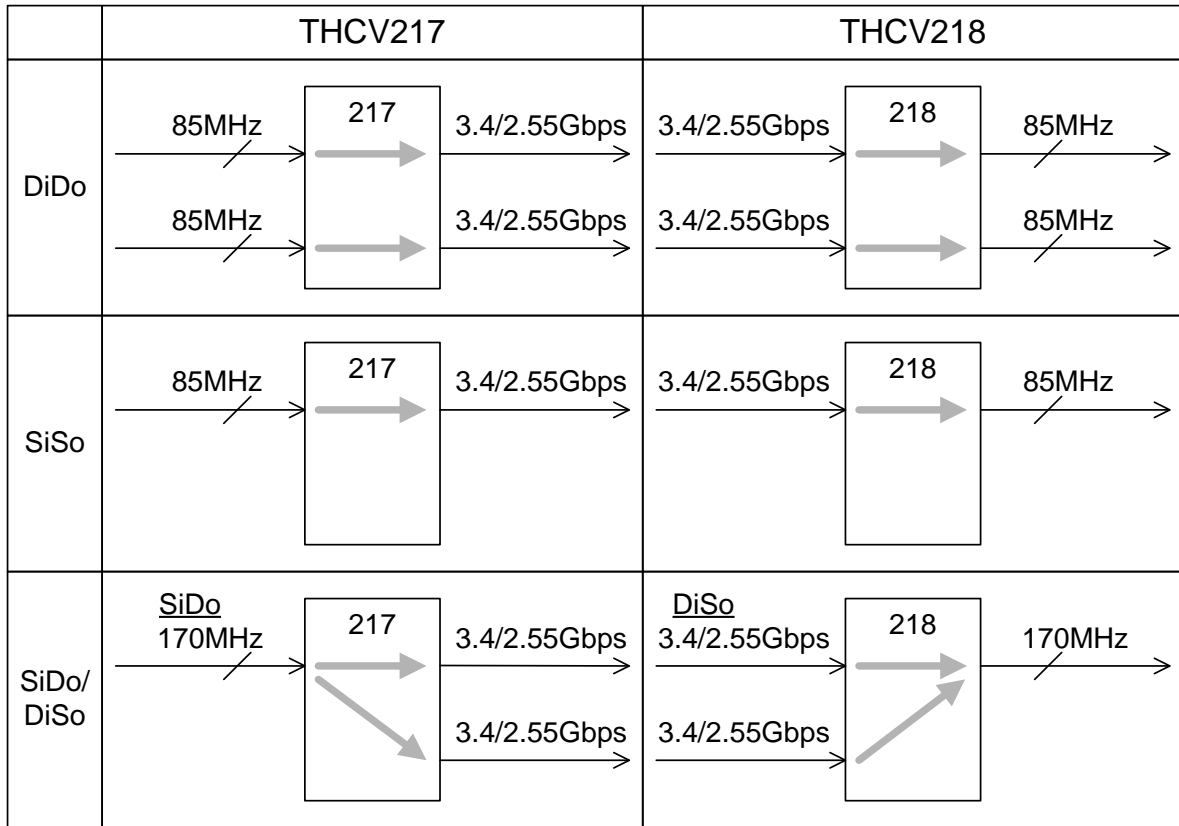


Figure 3. Operation modes of the chipset (10bit/8bit)

CML Buffer

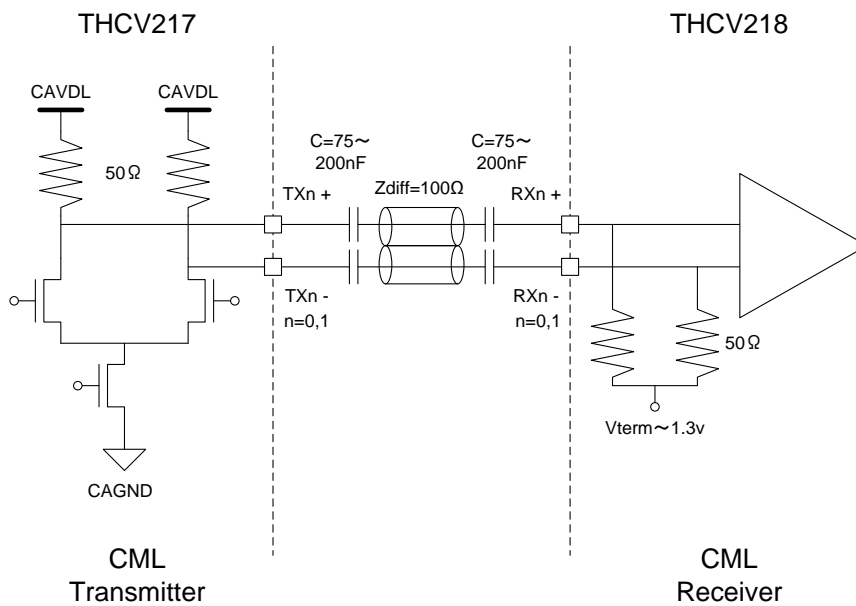


Figure 4. CML buffer scheme

Lock Detect and Hot-Plug Function

LOCKN and HTPDN of Rx must be connected with those of Tx as in Figure 5.

LOCKN and HTPDN on THCV218 are both open drain outputs. Pull-up resistors are needed at Tx side.

If THCV218 is not active (in the power down mode, powered off, or not connected), THCV218's HTPDN turns high-Z, and the pull-up resistor at the Tx side makes the HTPDN input of THCV217 high. THCV217 then enters into the power down mode.

When THCV218 is active, HTPDN is pulled down by THCV218. Then THCV217 starts up and transmits the "training pattern" for link training.

LOCKN indicates whether THCV218 is in the lock state or not. If THCV218 is not the lock state, LOCKN turns high-Z. Otherwise (in the lock state), it's pulled down by THCV218.

THCV217 keeps transmitting the "training pattern" until LOCKN turns low. And then THCV217 starts transmitting serialized input data.

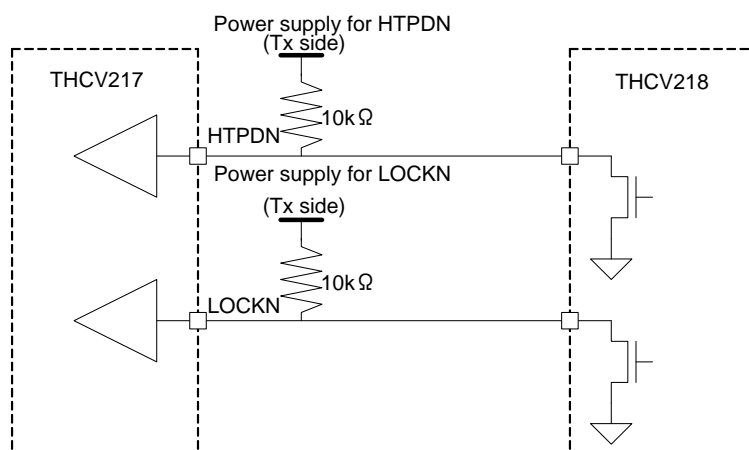


Figure 5. Hot-plug and Lock detect scheme

HTPDN connection between THCV217 and THCV218 can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as Low. See Figure 6.

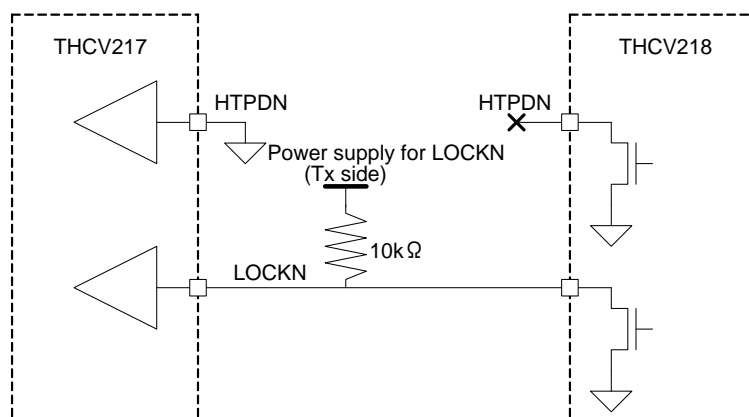


Figure 6. HTPDN is not connected scheme

Pre-emphasis

Pre-emphasis can equalize severe signal degradation caused by long-distance or high-speed transmission. The PRE pin selects the strength of pre-emphasis. See Table 4.

| PRE | Description |
|-----|----------------------|
| H | w/ 100% Pre-emphasis |
| L | w/o Pre-emphasis |

Table 4. Pre-emphasis function table

Power Down Function

Setting the PDN pin low places THCV217 in the power-down mode. All the internal circuitry turns off and the TXmp/n (m=0, 1) outputs turn to CAVDL.

Setting the PDN pin low places THCV218 in the power-down mode. All the internal circuitry turns off and the CMOS outputs drives low.

Field BET Operation

In order to help users to debug high-speed serial links (CML lines), THCV217 and THCV218 have an operation mode in which they act as the bit error tester (BET). In this mode, THCV217 internally generates a test pattern, which is then serialized onto CML high-speed lines. THCV218 receives the data stream and checks the sampled data for bit errors.

This "Field BET" mode is activated by setting BET= H on THCV217, and BET=H and Reserved7=L on THCV218.

In the Field BET mode, the on-chip pattern generator on THCV217 is enabled and generates the test pattern as long as the clock is applied onto CLKIN. Other CMOS data inputs are ignored. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto CML channels. As for THCV218, the internal test pattern check circuit gets enabled and the pattern check result is output on BETOUT. The BETOUT pin goes LOW whenever bit errors occur, and it stays HIGH when there is no bit error. Please refer to Figure 7 and Figure 8.

Table 5 shows possible combinations of Tx and Rx for normal operation and Field BET operation.

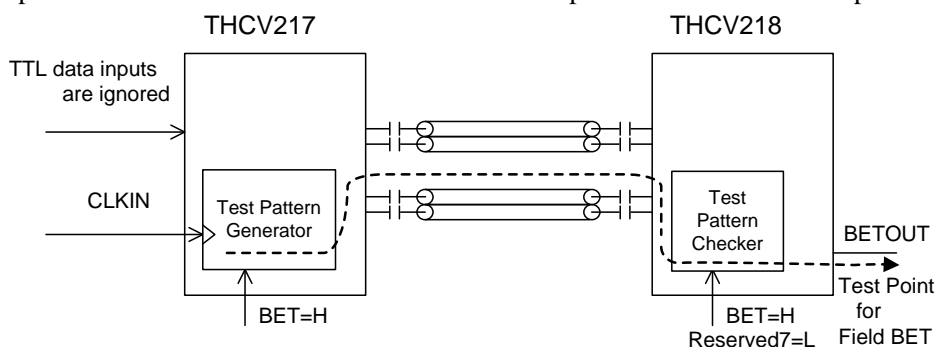


Figure 7. Field BET Configuration

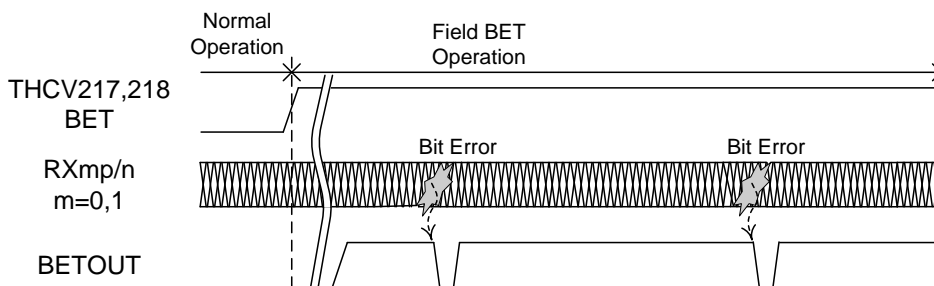


Figure 8. Relationship between bit error and BETOUT

| | Tx | Rx |
|---|---------|---------|
| 1 | THCV217 | THCV218 |
| 2 | THCV215 | THCV218 |
| 3 | THCV217 | THCV216 |

Table 5. Possible combinations of Tx and Rx for Field BET mode

DGLOCK

In order to reduce the number of cables needed for HTPDN and LOCKN in multiple-Rx chip configuration, THCV218 is equipped with the DGLOCK pin. When all the DGLOCK pins are connected as in Figure 9, the connected Rx chips can share the CDR lock status, making all the Rx chips in the same operation status.

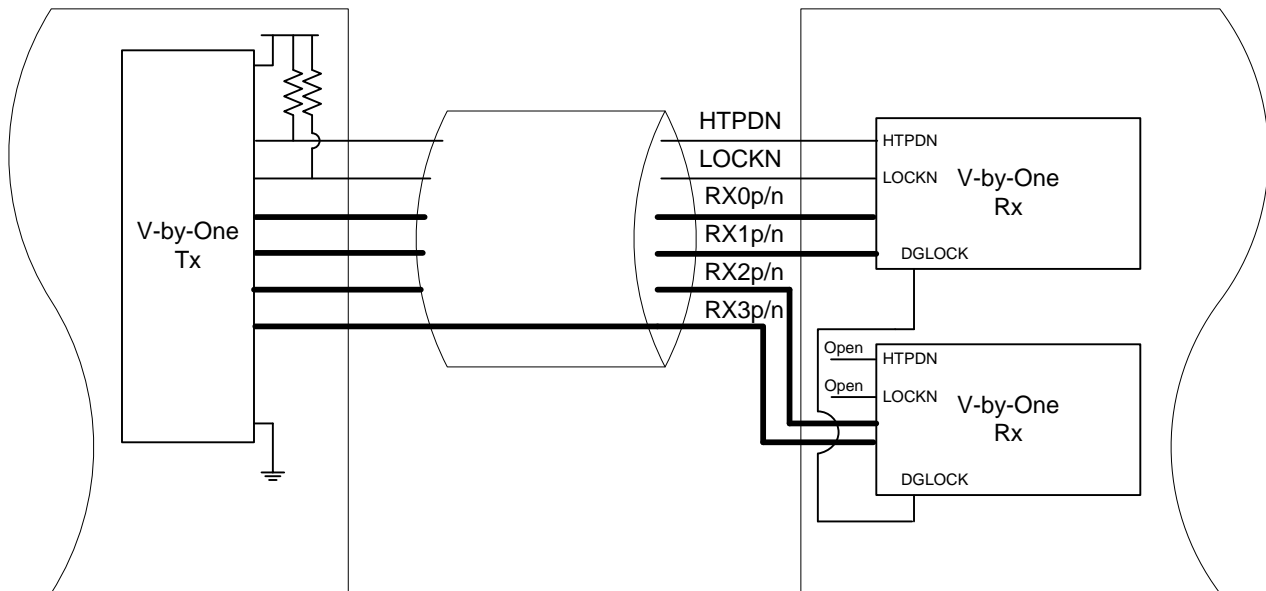


Figure 9. Usage of DGLOCK in multiple-Rx configuration

PLL Frequency Range Select

The THCV218's PLL input pin selects the operating frequency range of THCV218. Table 6 shows the selectable frequency ranges for operation modes.

| Operation Mode | PLL | CLKOUT |
|----------------------|-----|--------------|
| Dual-in/Dual-out | H | 20 to 40MHz |
| | L | 40 to 85MHz |
| Dual-in/Single-out | H | Forbidden |
| | L | 40 to 170MHz |
| Single-in/Single-out | H | 20 to 40MHz |
| | L | 40 to 85MHz |

Table 6. Frequency range select

Absolute Maximum Ratings

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------------------|------|------|------------|-------|
| 1.8V Supply Voltage (VDL,CAVDL,CPVDL) | -0.3 | - | +2.1 | V |
| 3.3V Supply Voltage (DVDH) | -0.3 | - | +4.0 | V |
| CMOS Input Voltage | -0.3 | - | DVDH+0.3 | V |
| CML Transmitter Output Voltage | -0.3 | - | CAVDL+0.3 | V |
| CML Output Current | -50 | - | 50 | mA |
| Storage Temperature | -55 | - | +125 | °C |
| Junction Temperature | - | - | +125 | °C |
| Reflow Peak Temperature/Time | - | - | +260/10sec | °C |
| Maximum Power Dissipation @+25°C | 2.47 | | | W |

Table 7. THCV217 Absolute Maximum Ratings

| Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|------|------|------------|-------|
| 1.8V Supply Voltage (VDL,CAVDL) | -0.3 | - | +2.1 | V |
| 3.3V Supply Voltage (DVDH) | -0.3 | - | +4.0 | V |
| CMOS Input Voltage | -0.3 | - | DVDH+0.3 | V |
| CMOS Output Voltage | -0.3 | - | DVDH+0.3 | V |
| CMOS Open drain Output Voltage | -0.3 | - | +4.0 | V |
| CML Receiver Input Voltage | -0.3 | - | CAVDL+0.3 | V |
| Storage Temperature | -55 | - | +125 | °C |
| Junction Temperature | - | - | +125 | °C |
| Reflow Peak Temperature/Time | - | - | +260/10sec | °C |
| Maximum Power Dissipation @+25°C | 2.7 | | | W |

Table 8. THCV218 Absolute Maximum Ratings

Operating Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------------------|------|------|------|-------|
| 1.8V Supply Voltage (VDL,CAVDL,CPVDL) | 1.62 | 1.80 | 1.98 | V |
| 3.3V Supply Voltage (DVDH) | 3.00 | 3.30 | 3.60 | V |
| Operating Temperature | -20 | - | 85 | °C |

Table 9. THCV217 Operating Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---------------------------------------|------|------|------|-------|
| 1.8V Supply Voltage (VDL,CAVDL,CPVDL) | 1.62 | 1.80 | 1.98 | V |
| 3.3V Supply Voltage (DVDH) | 3.00 | 3.30 | 3.60 | V |
| Operating Temperature | -20 | - | 85 | °C |

Table 10. THCV218 Operating Conditions

* “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Electrical Specifications

3.3V CMOS DC Specifications

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|-----------------------------|------------------|------|------|------|-------|
| VIH | High Level Input Voltage | I3,I3PU | 2.0 | - | DVDH | V |
| | | I3L | 2.0 | - | DVDH | V |
| VIL | Low Level Input Voltage | I3,I3PU | 0 | - | 0.8 | V |
| | | I3L | 0 | - | 0.7 | V |
| VOH | High Level Output Voltage | O3 IOH=-8mA | 2.4 | - | - | V |
| VOL | Low Level Output Voltage | O3 IOL=8mA | - | - | 0.4 | V |
| | | OD3,I3PU IOL=4mA | - | - | 0.4 | V |
| IiH | Input Leak Current High | VIN=DVDH | - | - | ±10 | uA |
| IiL | Input Leak Current Low | VIN=0V | - | - | ±10 | uA |
| IOZH | Output Leak Current High in | VIN=DVDH, OE=L | - | - | ±10 | uA |
| IOZL | Output Leak Current Low in | VIN=0V, OE=L | - | - | ±10 | uA |

Table 11. THCV217and THCV218 3.3V CMOS DC Specifications

CML DC Specifications

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|--------------------------------------|------------|--------------|------|------|-------|
| VTOD | CML Differential Mode Output Voltage | PRE=L | 200 | 300 | 400 | mV |
| PRE | CML Pre-emphasis Level | PRE=L | - | 0 | - | % |
| | | PRE=H | 80 | 100 | 120 | % |
| VTOC | CML Common Mode Output Voltage | PRE=L | CAVDL-VTOD | | | mV |
| | | PRE=H | CAVDL-2xVTOD | | | mV |
| ITOH | CML Output Leak Current High | PDN=H | - | - | ±10 | uA |
| ITOS | CML Output Short Circuit | CAVDL=1.8V | -90 | - | - | mA |

Table 12. THCV217 CML DC Specifications

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|---------------------------------------|-----------------------|------|------|------|-------|
| VRTH | CML Differential Input High Threshold | | - | - | 50 | mV |
| VRTL | CML Differential Input Low Threshold | | -50 | - | - | mV |
| IRIH | CML Input Leak Current High | PDN=L, RX0/1=CAVDL | - | - | ±10 | uA |
| IRIL | CML Input Leak Current Low | PDN=L,RX0/1=0V | - | - | ±10 | uA |
| IRRIH | CML Input Current High | RX0/1=CAVDL | - | - | 2 | mA |
| IRRIL | CML Input Current Low | RX0/1=0V | -6 | - | - | mA |
| RRIN | CML Differential Input Resistance | | 80 | 100 | 120 | Ω |

Table 13. THCV218 CML DC Specifications

Supply Currents

| Symbol | Parameter | conditions | Min. | Typ. | Max. | Units |
|---------|-----------------------------------------------------------------------|--------------------|------|------|------|-------|
| ITCCW | Transmitter Supply Current for VDL, CAVDL, CPVDL (Worst Case Pattern) | DiDo 10bit PRE = H | - | - | 185 | mA |
| | | SiSo 10bit PRE = H | - | - | 115 | mA |
| | | SiDo 10bit PRE = H | - | - | 180 | mA |
| ITCCW33 | Transmitter Supply Current for DVDH (Worst Case Pattern) | DiDo 10bit PRE = H | - | - | 10 | mA |
| | | SiSo 10bit PRE = H | - | - | 7 | mA |
| | | SiDo 10bit PRE = H | - | - | 10 | mA |
| ITCCS | Transmitter Power Down | PDN = L | - | - | 200 | uA |

Table 14. THCV217 Supply Currents

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------|-------------------------------------------------------------|---------------------------------|------|------|------|------|
| IRCCW | Receiver Supply Current for VDL, CAVDL (Worst Case Pattern) | DiDo 10bit | - | - | 180 | mA |
| | | SiSo 10bit | - | - | 95 | mA |
| | | DiSo 10bit | - | - | 170 | mA |
| IRCCW33 | Receiver Supply Current for DVDH (Worst Case Pattern) | DiDo 10bit CL=8pF | - | - | 200 | mA |
| | | SiSo 10bit CL=8pF | - | - | 100 | mA |
| | | DiSo 10bit CL=8pF | - | - | 200 | mA |
| IRCCS | Receiver Power Down Supply Current | PDN = L Input = Fixed L or H | - | - | 200 | uA |

Table 15. THCV218 Supply Currents

Switching Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|------------------------------------------------|-------------------|---------------|-----------------|---------------|-------|
| tTRF | TX0/1 Rise and Fall Time (20%-80%) | | 50 | - | 150 | ps |
| tTOSK | TX0/1 Output Inter Pair Skew | | -2 | - | 2 | UI |
| tTCIP | CLKIN Period | SiSo, DiDo | 11.76 | - | 50 | ns |
| | | SiDo | 5.88 | - | 25 | ns |
| tTCH | CLK IN High Time | | 0.35xtTCIP | 0.5xtTCIP | 0.65xtTCIP | ns |
| tTCL | CLK IN Low Time | | 0.35txTCIP | 0.5xtTCIP | 0.65xtTCIP | ns |
| tTS | CMOS Data Setup to CLK IN | | 2.0 | - | - | ns |
| tTH | CMOS Data Hold to CLK IN | | 0.5 | - | - | ns |
| tTCD | Input Clock to Output Data Delay | SiSo / DiDo 8bit | typ.-10 | (13+7/10)xtTCIP | typ.+10 | ns |
| | | SiSo / DiDo 10bit | | 13xtTCIP | | |
| | | SiDo 8bit | typ.-10-tTCIP | (21+4/10)xtTCIP | typ.+10+tTCIP | |
| | | SiDo 10bit | | 20xtTCIP | | |
| tTPD | Power On to PDN High Delay | | 0 | - | - | ns |
| tTPLL0 | PDN High to CML Output Delay | | - | - | 10 | ms |
| tTPLL1 | PDN Low to CML Output High Fix Delay | | - | - | 20 | ns |
| tTNP0 | LOCKN High to Training Pattern Output Delay | | - | - | 10 | ms |
| tTNP1 | LOCKN Low to Data Pattern Output Delay | | - | - | 10 | ms |

Table 16. THCV217 Switching Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|-------------------------------------------|-----------------------|----------------|----------------|---------|-------|
| tRBIT | Unit Interval | COL=L | 294 | - | 1250 | ps |
| | | COL=H | 392 | - | 1667 | ps |
| tRISK | RX0/1 Input Inter Pair Skew | | - | - | 15 | UI |
| tRCP | CLKOUT Period | SiSo, DiDo | 11.76 | T | 50.0 | ns |
| | | DiSo | 5.88 | | 25.0 | ns |
| tRCH | CLKOUT High Time | | - | T/2 | - | ns |
| tRCL | CLKOUT Low Time | | - | T/2 | - | ns |
| tDOUT | CMOS Data OUT Period | | - | T | - | ns |
| tRS | CMOS Data Setup to CLKOUT | | 0.45xtRCP-0.45 | - | - | ns |
| tRH | CMOS Data Hold to CLKOUT | | 0.45xtRCP-0.45 | - | - | ns |
| tDK | CLKOUT Delay Time | PLL=H | - | 3T/16 | - | ns |
| | | PLL=L | - | 3T/32 | - | ns |
| tTLH | CMOS Low to High Transition Time | Clock | - | 0.7 | 1.0 | ns |
| | | Data | - | 1.4 | 2.0 | ns |
| tTHL | CMOS High to Low Transition Time | Clock | - | 0.7 | 1.0 | ns |
| | | Data | - | 1.4 | 2.0 | ns |
| tRDC | Input Data to Output Clock Delay | SiSo/DiDo 8bit PLL=L | typ.-10 | (18+5/10)xtRCP | typ.+10 | ns |
| | | SiSo/DiDo 10bit PLL=L | | 18xtRCP | | |
| | | SiSo/DiDo 8bit PLL=H | | (16+4/10)xtRCP | | |
| | | SiSo/DiDo 10bit PLL=H | | (15+7/10)xtRCP | | |
| | | DiSo 8bit | | (39+5/10)xtRCP | | |
| | | DiSo 10bit | | 38xtRCP | | |
| tRPD | Power On to PDN High Delay | | 0 | - | - | ns |
| tRHPD0 | PDN High to HTPDN Low Delay | | - | - | 1 | us |
| tRHPD1 | PDN Low to HTPDN High Delay | | - | - | 1 | us |
| tRPLL0 | Training Pattern Input to LOCKN Low Delay | | - | - | 10 | ms |
| tRPLL1 | PDN Low to LOCKN High | | - | - | 10 | us |
| tRLCK0 | LOCKN Low to TTL Output | | - | - | 5 | ms |
| tRLCK1 | LOCKN High to TTL Low-fixed | | - | - | 0 | ns |

Table 17. THCV218 Switching Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|------------------|------------|---------|------|------|-------|
| tDEH | DE=High Duration | | 2xtTCIP | - | - | sec |
| tDEL | DE=Low Duration | SiSo, DiDo | 2xtTCIP | - | - | sec |
| | | SiDo, DiSo | 4xtTCIP | - | - | sec |

Table 18. DE requirement

AC Timing Diagrams and Test Circuits
 CMOS Input Switching Characteristics

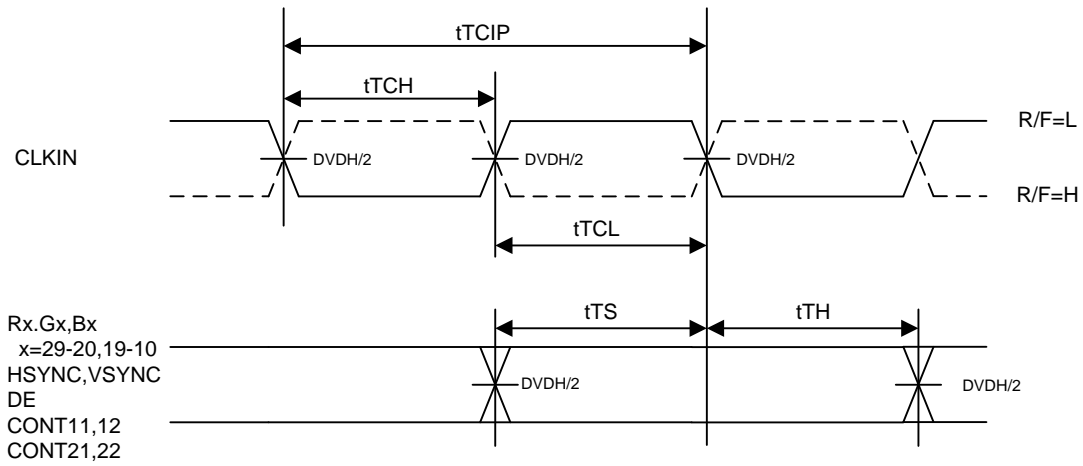


Figure 10. CMOS Input Switching Timing Diagrams

CMOS Output Switching Characteristics

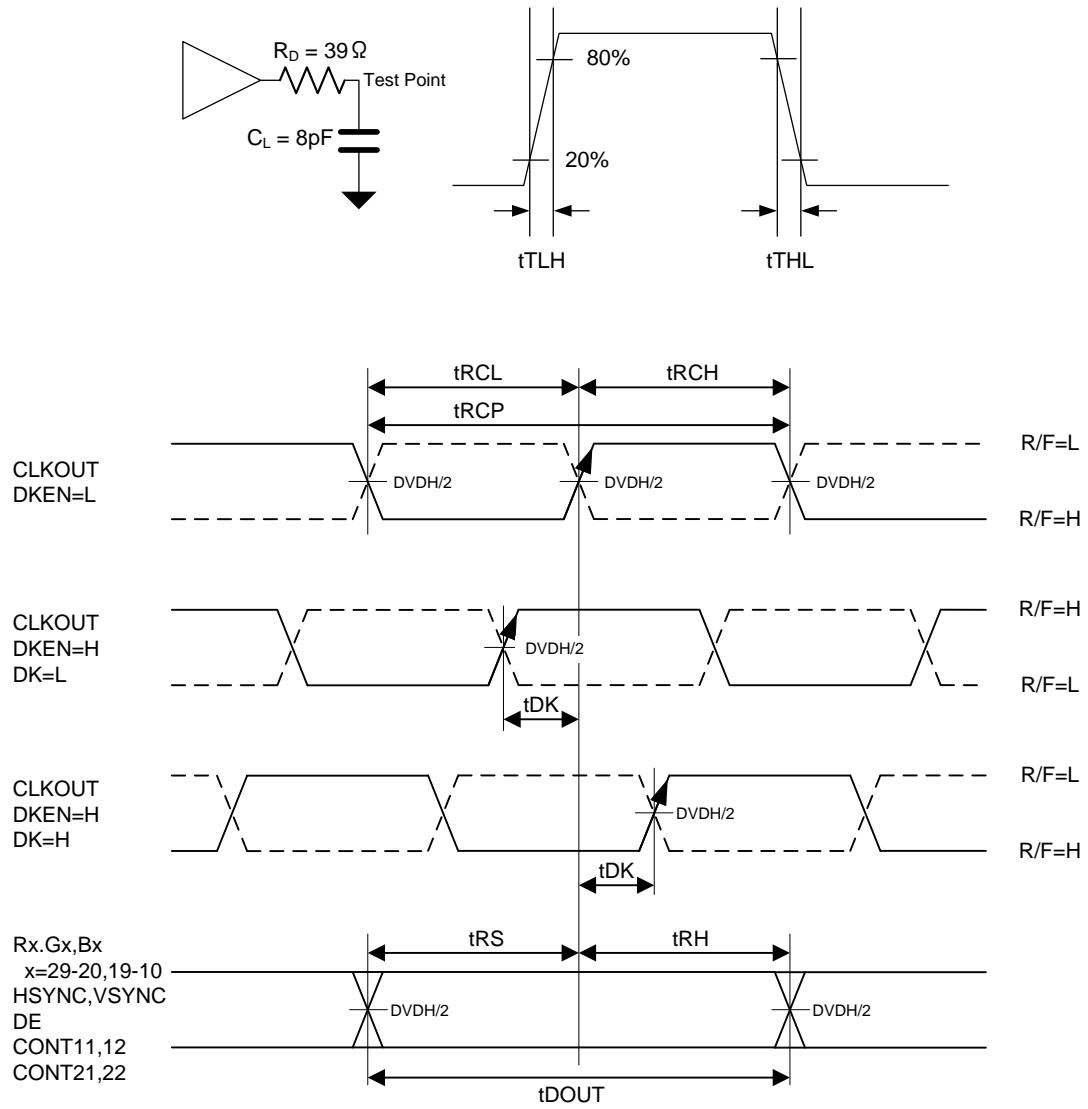


Figure 11. CMOS Output Switching Timing Diagrams and Test Circuit

CML Output Switching Characteristics

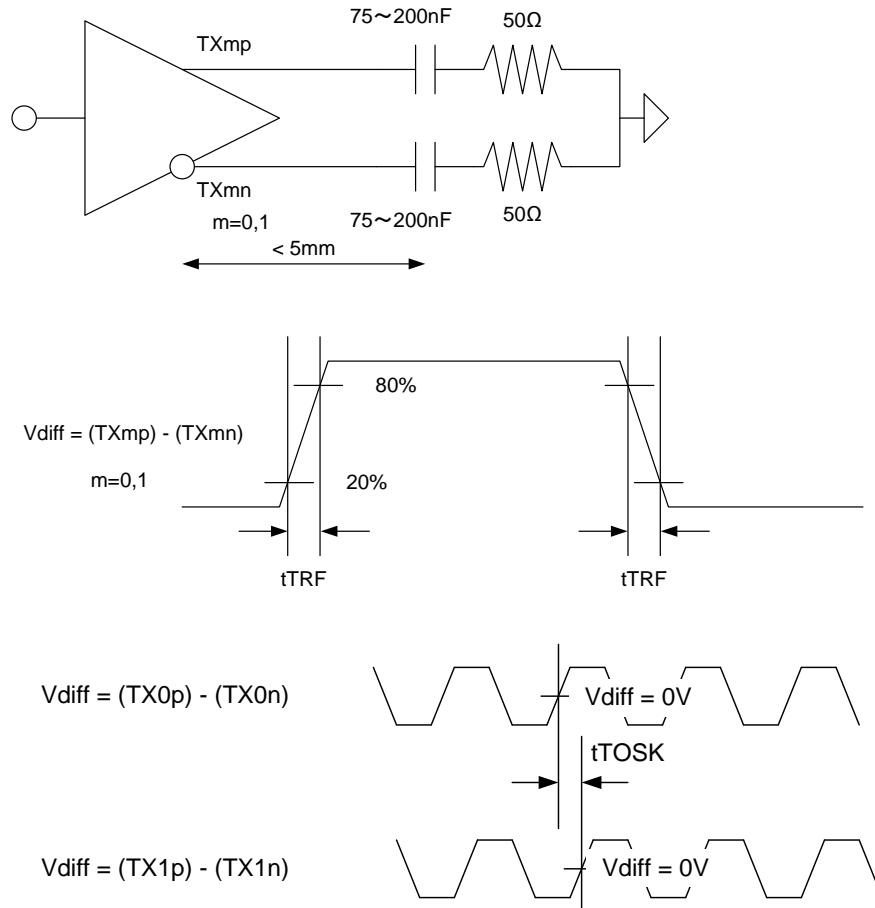


Figure 12. CML Output Switching Timing Diagrams and Test Circuit

CML Input Switching Characteristics

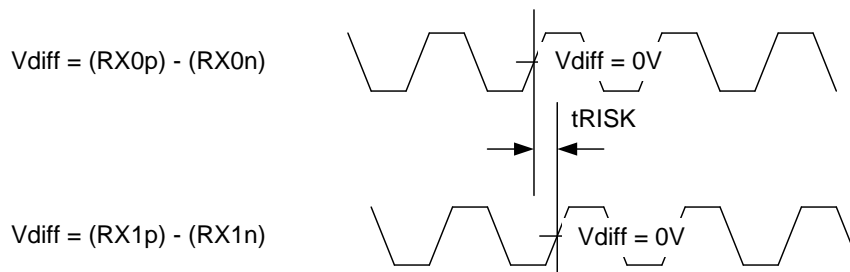


Figure 13. CML Input Timing Diagrams

Latency Characteristics

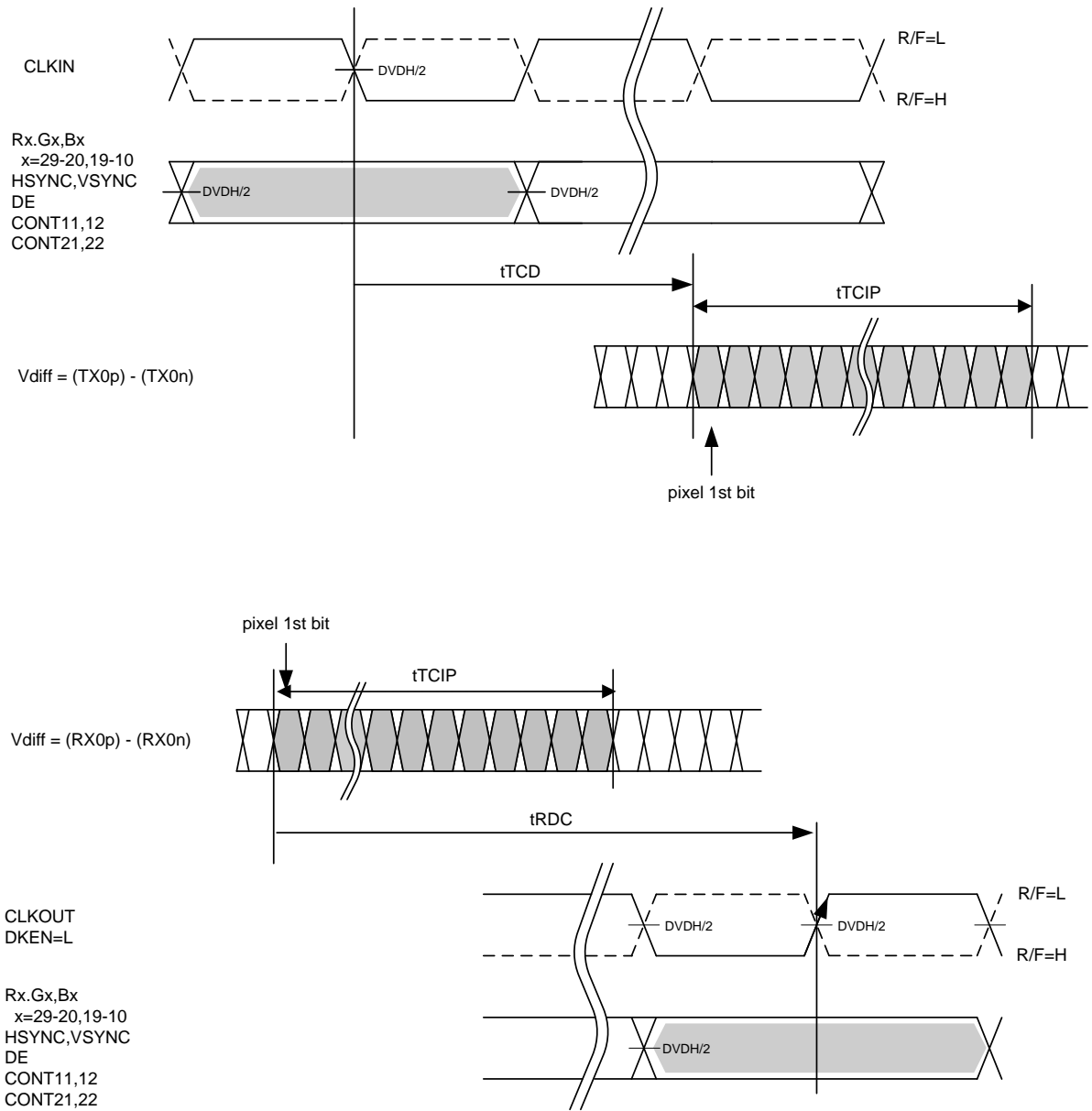


Figure 14. THCV217 and THCV218 Latency

Lock and Unlock Sequence

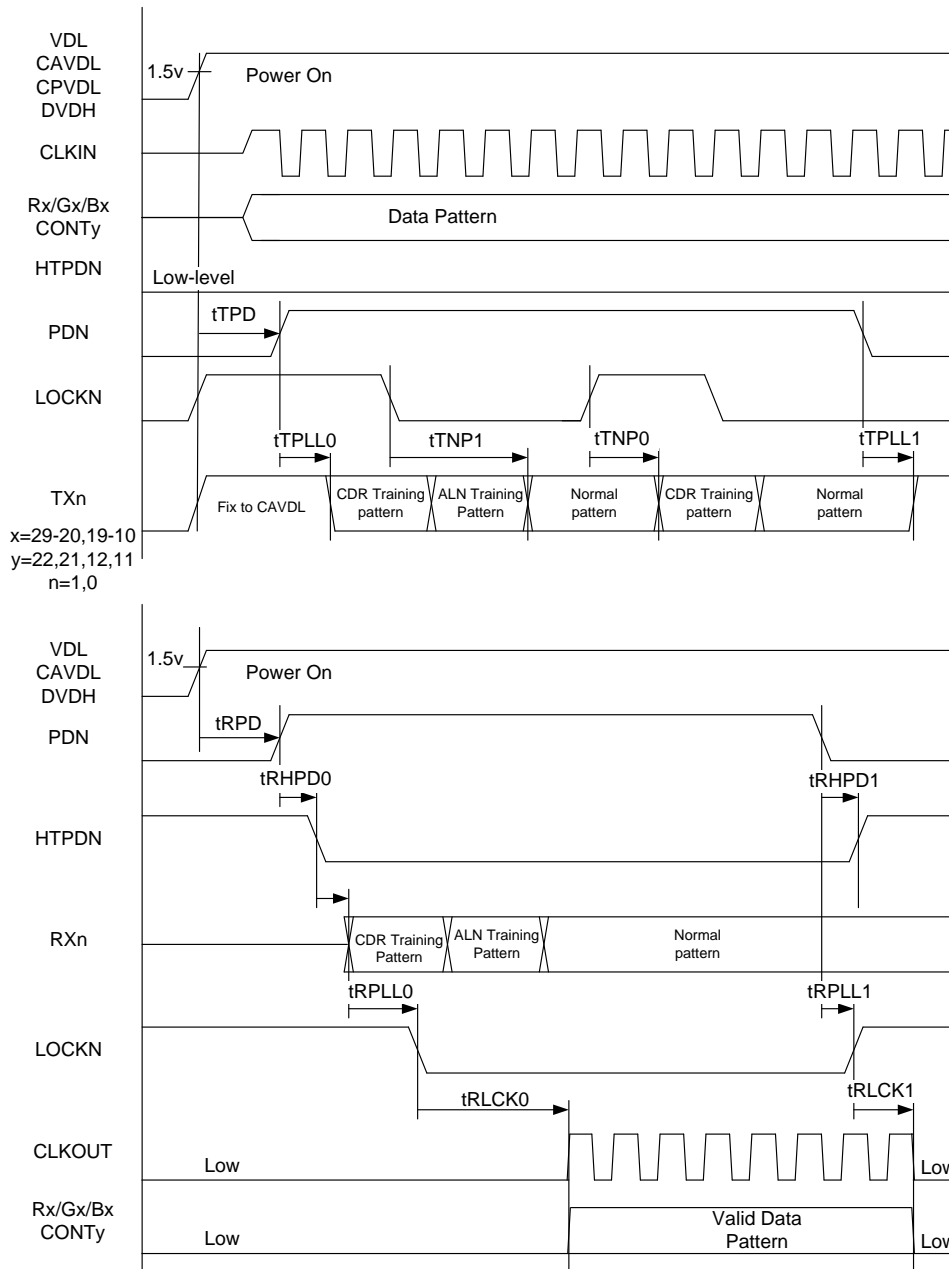


Figure 15. THCV217 and THCV218 Lock and Unlock Sequence

tTPD and tRPD minimum is 0sec; therefore, PDN can be applied at the same time as VDL, CAVDL, CPVDL and DVDH. tTPLL0 is the time from “both PDN=High and HTPDN=Low“ moment to Training pattern ignition. HTPDN could transit from High to Low under PDN=High condition at THCV217, which is different from what Figure 15 indicates but is natural situation.

Note: When change and discontinuation occur in the clock frequency to THCV217, in order to collateralize the operation after clock frequency change or return, please insert a Low pulse to the PDN pin of THCV218 to reset the internal PLL.

THCV217 Input Data Mapping

| Data Signals | | Transmitter Input Pin Name | | Symbol defined by V-by-One® HS |
|---------------|--------------|----------------------------|--------------|--------------------------------|
| 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | |
| R0*1 | - | R10 | - | D30 |
| R1*1 | - | R11 | - | D31 |
| R2 | R0 | R12 | R12 | D0 |
| R3 | R1 | R13 | R13 | D1 |
| R4 | R2 | R14 | R14 | D2 |
| R5 | R3 | R15 | R15 | D3 |
| R6 | R4 | R16 | R16 | D4 |
| R7 | R5 | R17 | R17 | D5 |
| R8 | R6 | R18 | R18 | D6 |
| R9 | R7 | R19 | R19 | D7 |
| G0*1 | - | G10 | - | D28 |
| G1*1 | - | G11 | - | D29 |
| G2 | G0 | G12 | G12 | D8 |
| G3 | G1 | G13 | G13 | D9 |
| G4 | G2 | G14 | G14 | D10 |
| G5 | G3 | G15 | G15 | D11 |
| G6 | G4 | G16 | G16 | D12 |
| G7 | G5 | G17 | G17 | D13 |
| G8 | G6 | G18 | G18 | D14 |
| G9 | G7 | G19 | G19 | D15 |
| B0*1 | - | B10 | - | D26 |
| B1*1 | - | B11 | - | D27 |
| B2*1 | B0*1 | B12 | B12 | D16 |
| B3*1 | B1*1 | B13 | B13 | D17 |
| B4*1 | B2*1 | B14 | B14 | D18 |
| B5*1 | B3*1 | B15 | B15 | D19 |
| B6*1 | B4*1 | B16 | B16 | D20 |
| B7*1 | B5*1 | B17 | B17 | D21 |
| B8*1 | B6*1 | B18 | B18 | D22 |
| B9*1 | B7*1 | B19 | B19 | D23 |
| CONT1*1*2 | - | CONT11 | - | D25 |
| CONT2*1*2 | - | CONT12 | - | D24 |
| HSYNC | HSYNC | HSYNC | HSYNC | HSYNC |
| VSYNC | VSYNC | VSYNC | VSYNC | VSYNC |
| DE | DE | DE | DE | DE |

*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

*2 3D flags defined in the V-by-One® HS Standard are assigned to the following bit.

V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> CONT2

V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> CONT1

Table 19. CMOS Input Data Mapping for Single-in/Single-out, Single-in/Dual-out mode

THCV217 Input Data Mapping (Continued)

| 1st Pixel Data | | | | 2nd Pixel Data | | | | Symbol defined by V-by-One® HS |
|----------------|--------------|----------------------------|--------------|----------------|--------------|----------------------------|--------------|--------------------------------|
| Data Signals | | Transmitter Input Pin Name | | Data Signals | | Transmitter Input Pin Name | | |
| 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | |
| R10*1 | - | R10 | - | R20*1 | - | R20 | - | D30 |
| R11*1 | - | R11 | - | R21*1 | - | R21 | - | D31 |
| R12 | R10 | R12 | R12 | R22 | R20 | R22 | R22 | D0 |
| R13 | R11 | R13 | R13 | R23 | R21 | R23 | R23 | D1 |
| R14 | R12 | R14 | R14 | R24 | R22 | R24 | R24 | D2 |
| R15 | R13 | R15 | R15 | R25 | R23 | R25 | R25 | D3 |
| R16 | R14 | R16 | R16 | R26 | R24 | R26 | R26 | D4 |
| R17 | R15 | R17 | R17 | R27 | R25 | R27 | R27 | D5 |
| R18 | R16 | R18 | R18 | R28 | R26 | R28 | R28 | D6 |
| R19 | R17 | R19 | R19 | R29 | R27 | R29 | R29 | D7 |
| G10*1 | - | G10 | - | G20*1 | - | G20 | - | D28 |
| G11*1 | - | G11 | - | G21*1 | - | G21 | - | D29 |
| G12 | G10 | G12 | G12 | G22 | G20 | G22 | G22 | D8 |
| G13 | G11 | G13 | G13 | G23 | G21 | G23 | G23 | D9 |
| G14 | G12 | G14 | G14 | G24 | G22 | G24 | G24 | D10 |
| G15 | G13 | G15 | G15 | G25 | G23 | G25 | G25 | D11 |
| G16 | G14 | G16 | G16 | G26 | G24 | G26 | G26 | D12 |
| G17 | G15 | G17 | G17 | G27 | G25 | G27 | G27 | D13 |
| G18 | G16 | G18 | G18 | G28 | G26 | G28 | G28 | D14 |
| G19 | G17 | G19 | G19 | G29 | G27 | G29 | G29 | D15 |
| B10*1 | - | B10 | - | B20*1 | - | B20 | - | D26 |
| B11*1 | - | B11 | - | B21*1 | - | B21 | - | D27 |
| B12*1 | B10*1 | B12 | B12 | B22*1 | B20*1 | B22 | B22 | D16 |
| B13*1 | B11*1 | B13 | B13 | B23*1 | B21*1 | B23 | B23 | D17 |
| B14*1 | B12*1 | B14 | B14 | B24*1 | B22*1 | B24 | B24 | D18 |
| B15*1 | B13*1 | B15 | B15 | B25*1 | B23*1 | B25 | B25 | D19 |
| B16*1 | B14*1 | B16 | B16 | B26*1 | B24*1 | B26 | B26 | D20 |
| B17*1 | B15*1 | B17 | B17 | B27*1 | B25*1 | B27 | B27 | D21 |
| B18*1 | B16*1 | B18 | B18 | B28*1 | B26*1 | B28 | B28 | D22 |
| B19*1 | B17*1 | B19 | B19 | B29*1 | B27*1 | B29 | B29 | D23 |
| CONT11*1*2 | - | CONT11 | - | CONT21*1*2 | - | CONT21 | - | D25 |
| CONT12*1*2 | - | CONT12 | - | CONT22*1*2 | - | CONT22 | - | D24 |
| HSYNC | HSYNC | HSYNC | HSYNC | - | - | - | - | HSYNC |
| VSYNC | VSYNC | VSYNC | VSYNC | - | - | - | - | VSYNC |
| DE | DE | DE | DE | - | - | - | - | DE |

*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

*2 3D flags defined in the V-by-One® HS Standard are assigned to the following bit.

V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> CONT12/CONT22

V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> CONT11/CONT21

Table 20. CMOS Input Data Mapping for Dual-in/Dual-out mode

THCV218 Output Data Mapping

| Data Signals | | Receiver Output Pin Name | | Symbol defined by V-by-One® HS |
|---------------|--------------|--------------------------|--------------|--------------------------------|
| 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | |
| R0*1 | - | R10 | - | D30 |
| R1*1 | - | R11 | - | D31 |
| R2 | R0 | R12 | R12 | D0 |
| R3 | R1 | R13 | R13 | D1 |
| R4 | R2 | R14 | R14 | D2 |
| R5 | R3 | R15 | R15 | D3 |
| R6 | R4 | R16 | R16 | D4 |
| R7 | R5 | R17 | R17 | D5 |
| R8 | R6 | R18 | R18 | D6 |
| R9 | R7 | R19 | R19 | D7 |
| G0*1 | - | G10 | - | D28 |
| G1*1 | - | G11 | - | D29 |
| G2 | G0 | G12 | G12 | D8 |
| G3 | G1 | G13 | G13 | D9 |
| G4 | G2 | G14 | G14 | D10 |
| G5 | G3 | G15 | G15 | D11 |
| G6 | G4 | G16 | G16 | D12 |
| G7 | G5 | G17 | G17 | D13 |
| G8 | G6 | G18 | G18 | D14 |
| G9 | G7 | G19 | G19 | D15 |
| B0*1 | - | B10 | - | D26 |
| B1*1 | - | B11 | - | D27 |
| B2*1 | B0*1 | B12 | B12 | D16 |
| B3*1 | B1*1 | B13 | B13 | D17 |
| B4*1 | B2*1 | B14 | B14 | D18 |
| B5*1 | B3*1 | B15 | B15 | D19 |
| B6*1 | B4*1 | B16 | B16 | D20 |
| B7*1 | B5*1 | B17 | B17 | D21 |
| B8*1 | B6*1 | B18 | B18 | D22 |
| B9*1 | B7*1 | B19 | B19 | D23 |
| CONT1*1*2 | - | CONT11 | - | D25 |
| CONT2*1*2 | - | CONT12 | - | D24 |
| HSYNC | HSYNC | HSYNC | HSYNC | HSYNC |
| VSYNC | VSYNC | VSYNC | VSYNC | VSYNC |
| DE | DE | DE | DE | DE |

*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

*2 3D flags defined in the V-by-One® HS Standard are assigned to the following bit.

V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> CONT2

V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> CONT1

Table 21. CMOS Output Data Mapping for Single-in/Single-out, Dual-in/Single-out mode

THCV218 Output Data Mapping (Continued)

| 1st Pixel Data | | | | 2nd Pixel Data | | | | Symbol defined by V-by-One® HS |
|----------------|--------------|--------------------------|--------------|----------------|--------------|--------------------------|--------------|--------------------------------|
| Data Signals | | Receiver Output Pin Name | | Data Signals | | Receiver Output Pin Name | | |
| 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | 10bit (30bpp) | 8bit (24bpp) | |
| R10*1 | - | R10 | - | R20*1 | - | R20 | - | D30 |
| R11*1 | - | R11 | - | R21*1 | - | R21 | - | D31 |
| R12 | R10 | R12 | R12 | R22 | R20 | R22 | R22 | D0 |
| R13 | R11 | R13 | R13 | R23 | R21 | R23 | R23 | D1 |
| R14 | R12 | R14 | R14 | R24 | R22 | R24 | R24 | D2 |
| R15 | R13 | R15 | R15 | R25 | R23 | R25 | R25 | D3 |
| R16 | R14 | R16 | R16 | R26 | R24 | R26 | R26 | D4 |
| R17 | R15 | R17 | R17 | R27 | R25 | R27 | R27 | D5 |
| R18 | R16 | R18 | R18 | R28 | R26 | R28 | R28 | D6 |
| R19 | R17 | R19 | R19 | R29 | R27 | R29 | R29 | D7 |
| G10*1 | - | G10 | - | G20*1 | - | G20 | - | D28 |
| G11*1 | - | G11 | - | G21*1 | - | G21 | - | D29 |
| G12 | G10 | G12 | G12 | G22 | G20 | G22 | G22 | D8 |
| G13 | G11 | G13 | G13 | G23 | G21 | G23 | G23 | D9 |
| G14 | G12 | G14 | G14 | G24 | G22 | G24 | G24 | D10 |
| G15 | G13 | G15 | G15 | G25 | G23 | G25 | G25 | D11 |
| G16 | G14 | G16 | G16 | G26 | G24 | G26 | G26 | D12 |
| G17 | G15 | G17 | G17 | G27 | G25 | G27 | G27 | D13 |
| G18 | G16 | G18 | G18 | G28 | G26 | G28 | G28 | D14 |
| G19 | G17 | G19 | G19 | G29 | G27 | G29 | G29 | D15 |
| B10*1 | - | B10 | - | B20*1 | - | B20 | - | D26 |
| B11*1 | - | B11 | - | B21*1 | - | B21 | - | D27 |
| B12*1 | B10*1 | B12 | B12 | B22*1 | B20*1 | B22 | B22 | D16 |
| B13*1 | B11*1 | B13 | B13 | B23*1 | B21*1 | B23 | B23 | D17 |
| B14*1 | B12*1 | B14 | B14 | B24*1 | B22*1 | B24 | B24 | D18 |
| B15*1 | B13*1 | B15 | B15 | B25*1 | B23*1 | B25 | B25 | D19 |
| B16*1 | B14*1 | B16 | B16 | B26*1 | B24*1 | B26 | B26 | D20 |
| B17*1 | B15*1 | B17 | B17 | B27*1 | B25*1 | B27 | B27 | D21 |
| B18*1 | B16*1 | B18 | B18 | B28*1 | B26*1 | B28 | B28 | D22 |
| B19*1 | B17*1 | B19 | B19 | B29*1 | B27*1 | B29 | B29 | D23 |
| CONT11*1*2 | - | CONT11 | - | CONT21*1*2 | - | CONT21 | - | D25 |
| CONT12*1*2 | - | CONT12 | - | CONT22*1*2 | - | CONT22 | - | D24 |
| HSYNC | HSYNC | HSYNC | HSYNC | - | - | - | - | HSYNC |
| VSYNC | VSYNC | VSYNC | VSYNC | - | - | - | - | VSYNC |
| DE | DE | DE | DE | - | - | - | - | DE |

*1 CTL bits, which are carried during DE=Low except the 1st and the last pixel.

*2 3D flags defined in the V-by-One® HS Standard are assigned to the following bit.

V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> CONT12/CONT22

V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> CONT11/CONT21

Table 22. CMOS Output Data Mapping for Dual-in/Dual-out mode

Note

1)Power On Sequence

Don't input clock nor data before THCV217 is on in order to keep absolute maximum ratings.

2)Cable Connection and Disconnection

Don't connect and disconnect the CML cable, when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THCV217-218 on it. It is better for EMI reduction to place GND cable as close to CML cable as possible.

4)Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.

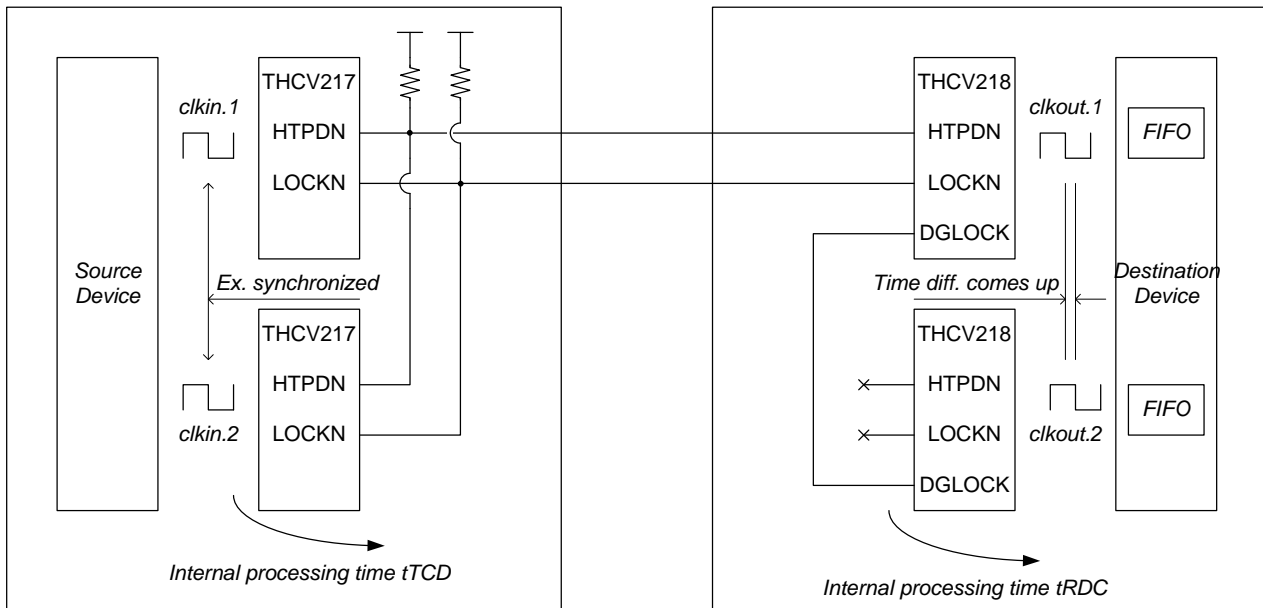
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.

LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.

LOCKN of Tx side can be simply split to multiple Tx.

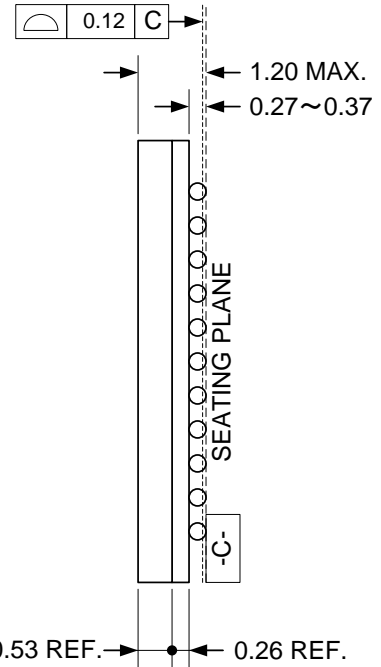
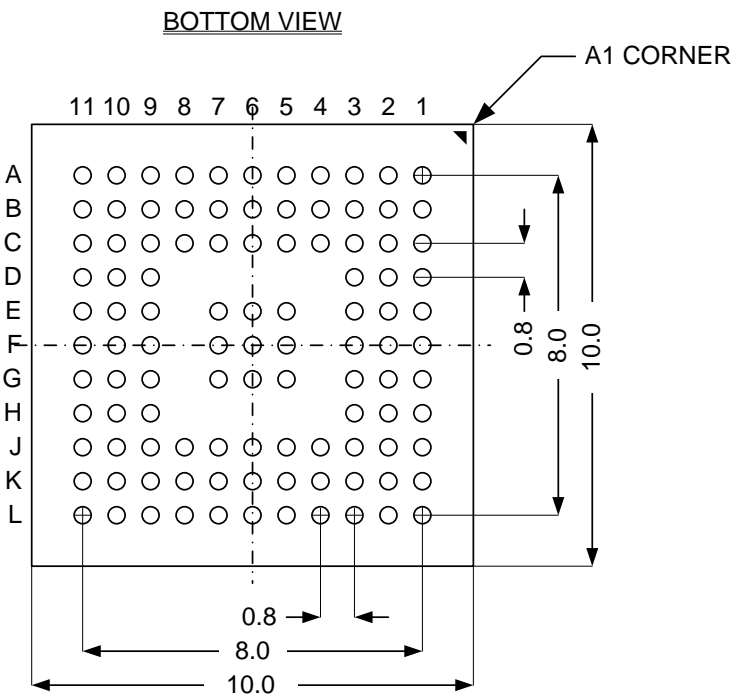
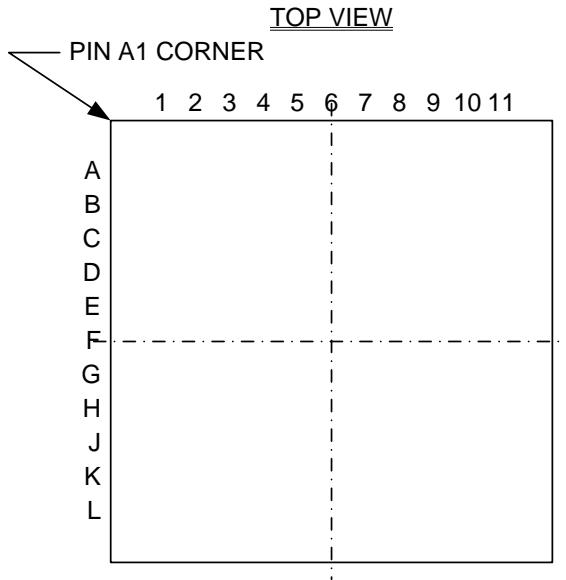
THCV218 DGLOCK connection is appropriate for multiple Rx use.

Also possible time difference of internal processing time (p.19 THCV217 t_{TCD} and p.20 THCV218 t_{RDC}) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV218, which may have internal FIFO.



Package

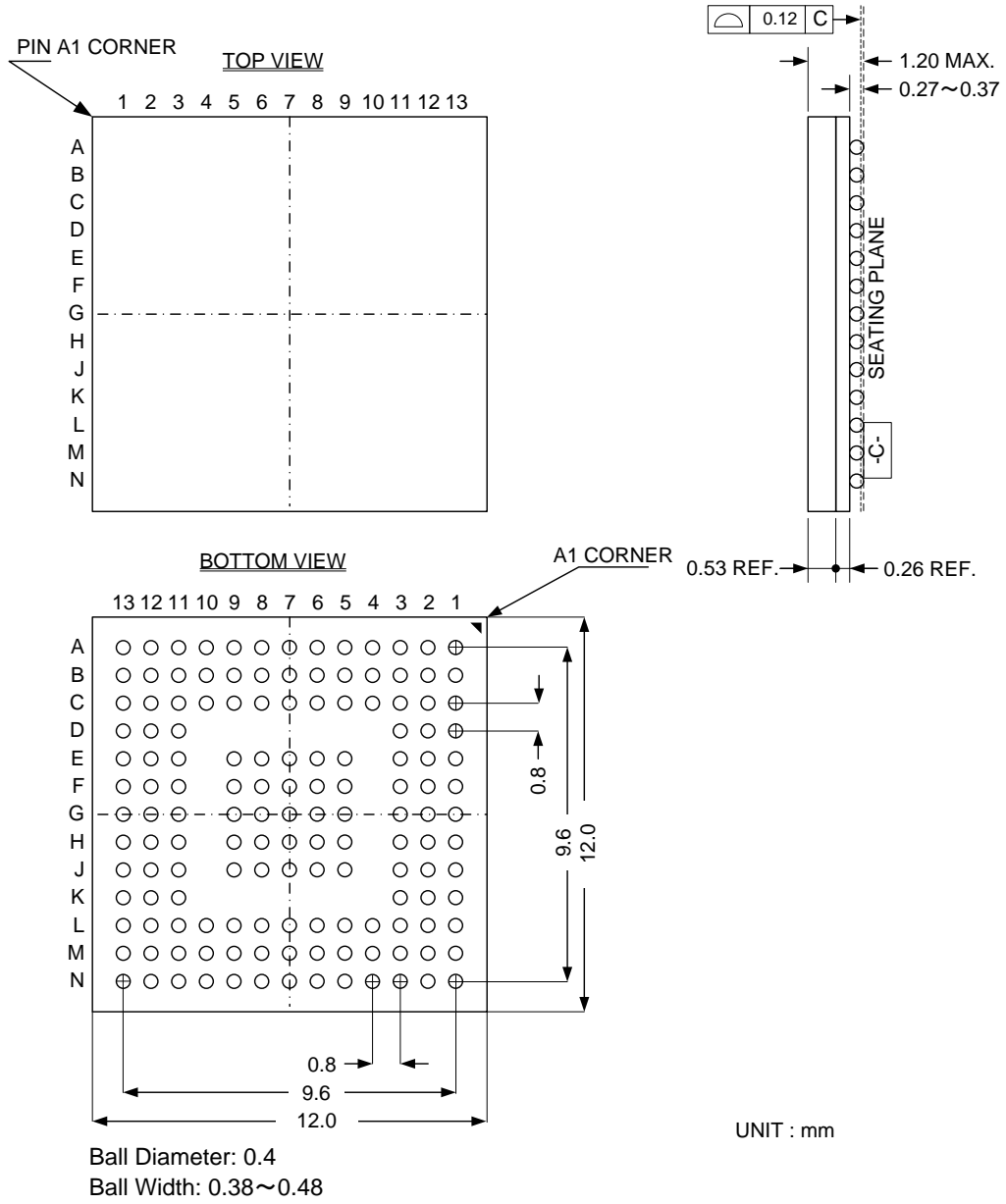
THCV217 TFBGA 10x10 105L



Ball Diameter: 0.4
Ball Width: 0.38~0.48

UNIT : mm

THCV218 TFBGA 12x12 145L



Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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5. Product Application
 - 5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
 - 5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. ("THine") accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
 - 5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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