THC63LVD1024

30Bit Color/135MHz Dual Link LVDS to LVCMOS converter

General Description

The THC63LVD1024 receiver is designed to support Dual Link transmission between display controller and Flat Panel Display module. The THC63LVD1024 converts the LVDS Data streams back into 67bits of LVCMOS Data with falling edge or rising edge clock for convenient with a variety of display controllers.
In Dual Link, Data transmit clock frequency of 135MHz, 67bits of RGB Data are transmitted data effective rate of 945Mbps per LVDS channel.
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Features

- Wide pixel clock range : 8-135MHz
- Flexible Input / Output mode
  - Dual-Link in/out
  - Dual-in / Single-out
  - Single-in / Dual-out
- Output clock edge and timing selectable
- DDR (Double Data Rate) output function
- VESA/JEIDA Data mapping support
- Flexible static output state control
- Power down mode
- 3.3V single power supply
- 144pin LQFP
- Compliant with RoHS and REACH

Block Diagram

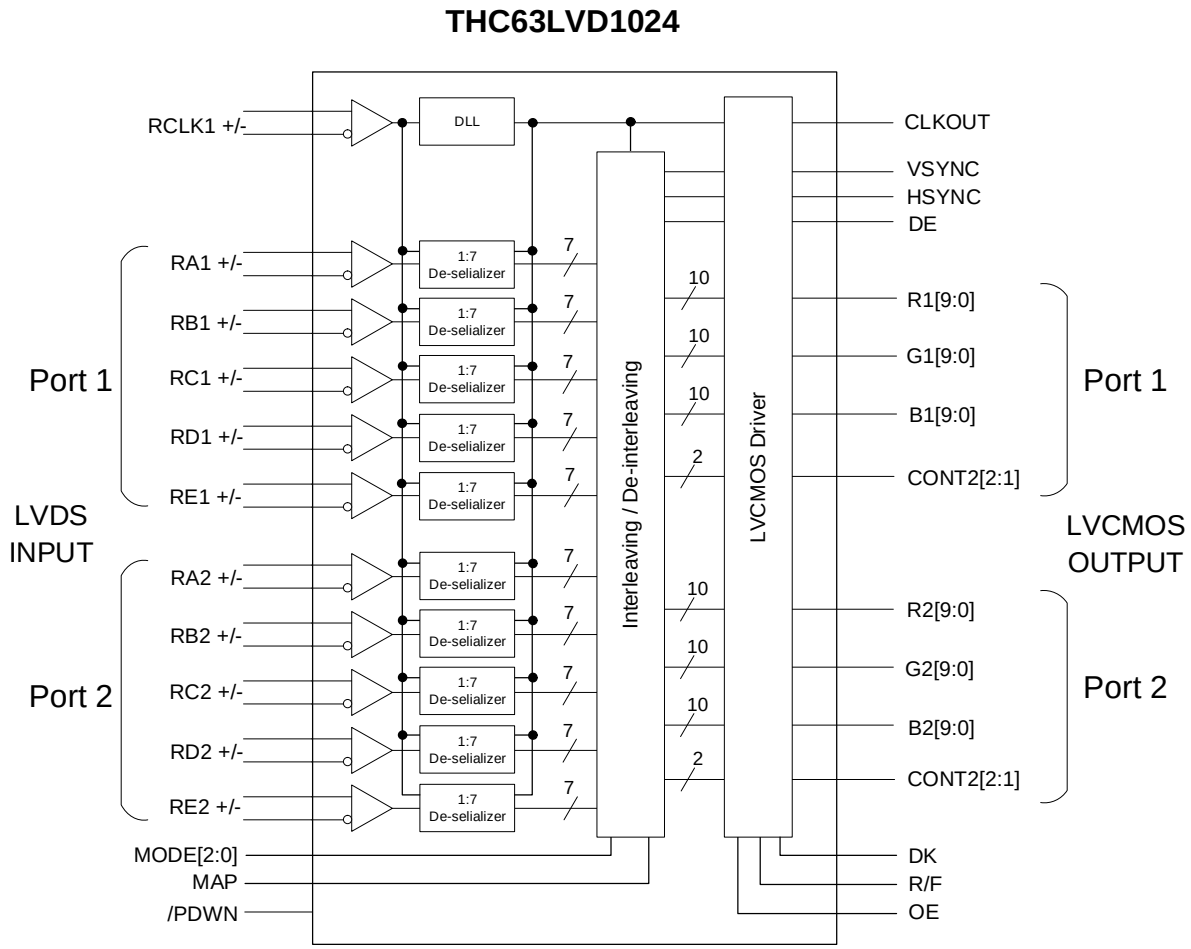


Figure 1. Block Diagram

Pin Diagram

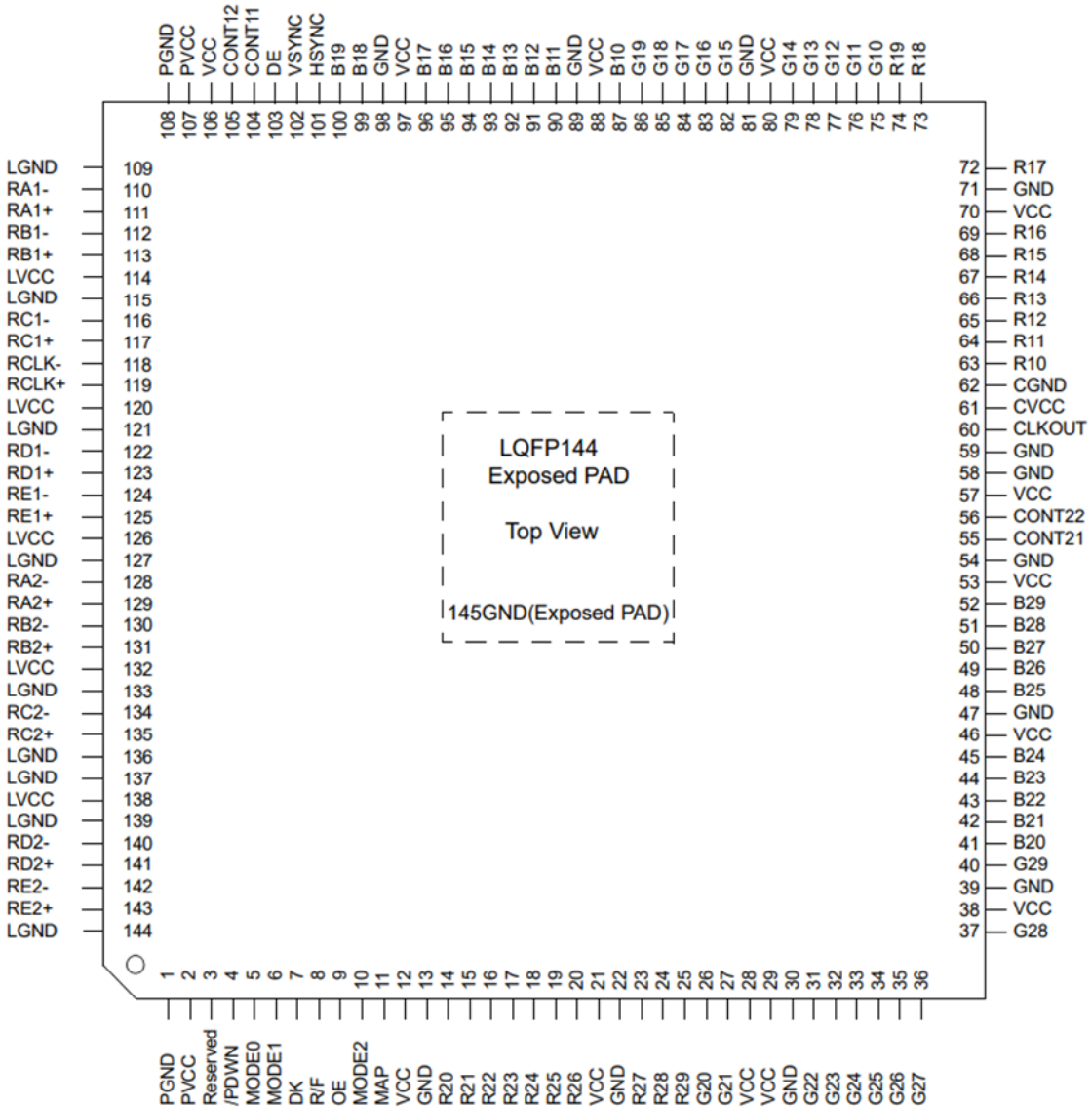


Figure 2. Pin Diagram

Pin Description

Table 1. Pin Description

Pin Name	Type	Description
RA1+, RA1- RB1+, RB1- RC1+, RC1- RD1+, RD1- RE1+, RE1-	LVDS Input	Serial Data Input Port 1 (1st pixel)
RCLK+,RCLK-		Clock Input
RA2+, RA2- RB2+, RB2- RC2+, RC2- RD2+, RD2- RE2+, RE2-		Serial Data Input Port 2 (2nd pixel)
R19 - R10 G19 - G10 B19 - B10 CONT11, CONT12	LVCMOS Output	Parallel Data Output Port 1
R29 – R20 G29 – G20 B29 – B20 CONT21, CONT22		Parallel Data Output Port 2
DE		Data Enable Output
VSYNC		Vsync Output
HSYNC		Hsync Output
CLKOUT		Clock Output
MODE1, MODE0	LVCMOS Input	Input / Output mode select. **See Table 2.**
MODE2		DDR (Double Data Rate) function enable. **See Figure 9.** MODE<1:0>=LH(Dual-in/Single-out Mode) H: DDR function enable. L: DDR function disable. MODE<1:0>=Other Must be tied to GND
MAP		LVDS mapping mode select. **See Figure 4, Figure 5.**
R/F		CLKOUT triggering edge select H : Rising edge L : Falling edge
OE		Output Enable. **See Table 4.** H : Output Enable L : Output Disable
/PDWN		Power down mode. **See Table 4.** H : Normal operation L : Power down
Reserved		Must be tied to VCC
DK	3-level LVCMOS Input	Output Clock Delay timing select. **See Table 3.**
VCC	Power	Power Supply for LVCMOS buffer and digital circuitry
GND	Ground	Ground for LVCMOS buffer and digital circuitry
LVCC	Power	Power Supply for LVDS inputs
LGND	Ground	Ground for LVDS inputs
PVCC	Power	Power Supply for PLL
PGND	Ground	Ground for PLL
CVCC	Power	Power supply for CLKOUT
CGND	Ground	Ground for CLKOUT

Functional Description

Pixel alignment

In Single-in/Dual-out and Dual-in/Single-out modes, interleaving and de-interleaving of odd and even pixels is performed.

Table 2. Pixel alignment mode pin settings

Mode name	Port	Input Pixel Order	Output Pixel Order	Pin settings			See Figure 4,5,6
				MODE0	MODE1	MODE2	
Dual-Link (*1)	1	1,3…	1,3…	L	L	-	x=1
	2	2,4…	2,4…				y=2
Single-Link	1	1,2,3,4…	1,2,3,4…	H	H	-	x=1
	2	Unused	Unused				Unused
Single-in/Dual-out (*2)	1	1,2,3,4…	1,3…	L	H	-	x=1,2
	2	Unused	2,4…				Unused
Dual-in/Single-out mode	1	1,3…	1,2,3,4…	H	L	H/L	x=1
	2	2,4…	Unused				y=1

*1: In Dual-link mode, the DE1, HSYNC1 and VSYNC1 signals input from RC1 are output from the DE, HSYNC and VSYNC pins and the DE2, HSYNC2 and VSYNC2 input from RC2 are not used.

*2: Single-in/Dual-out mode has timing requirements for DE input signals (**See Table 9 and Figure 12**). The pixel data immediately after the rising edge of the DE signal is the 1st pixel.

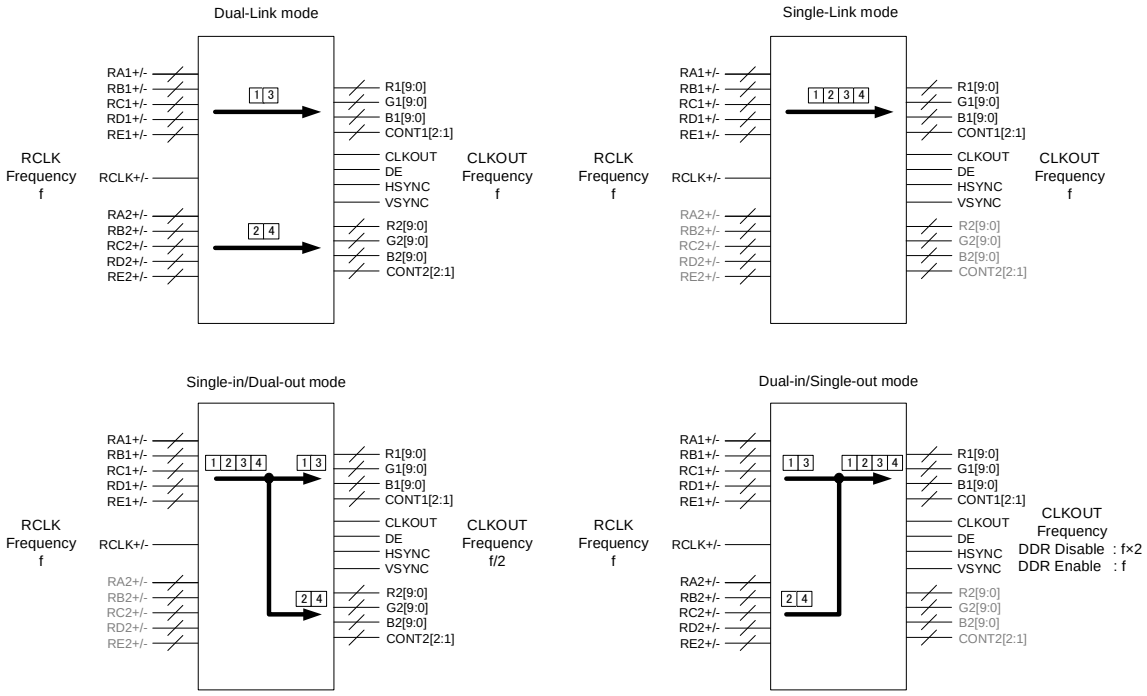
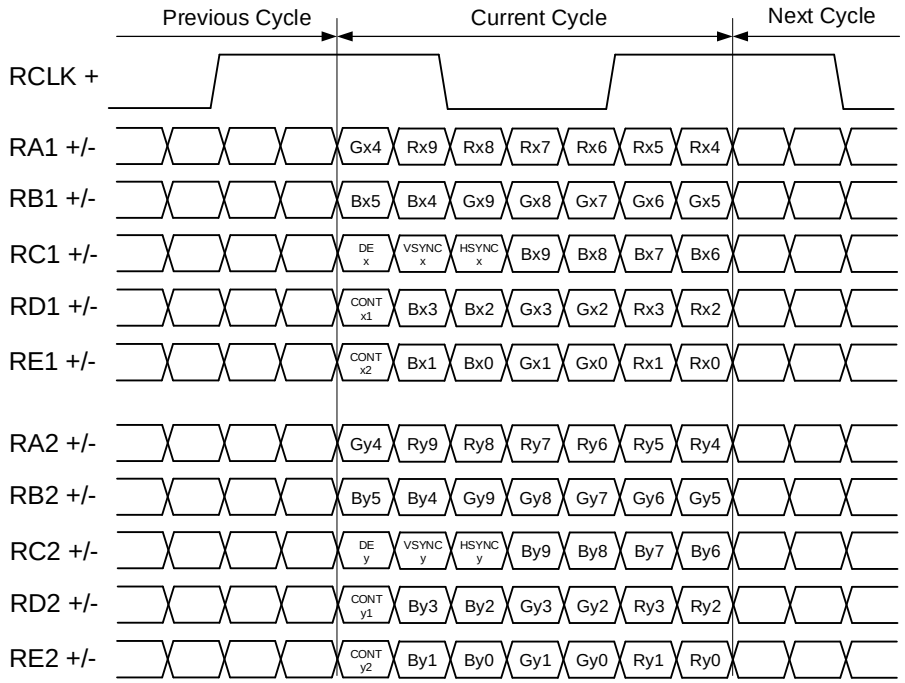
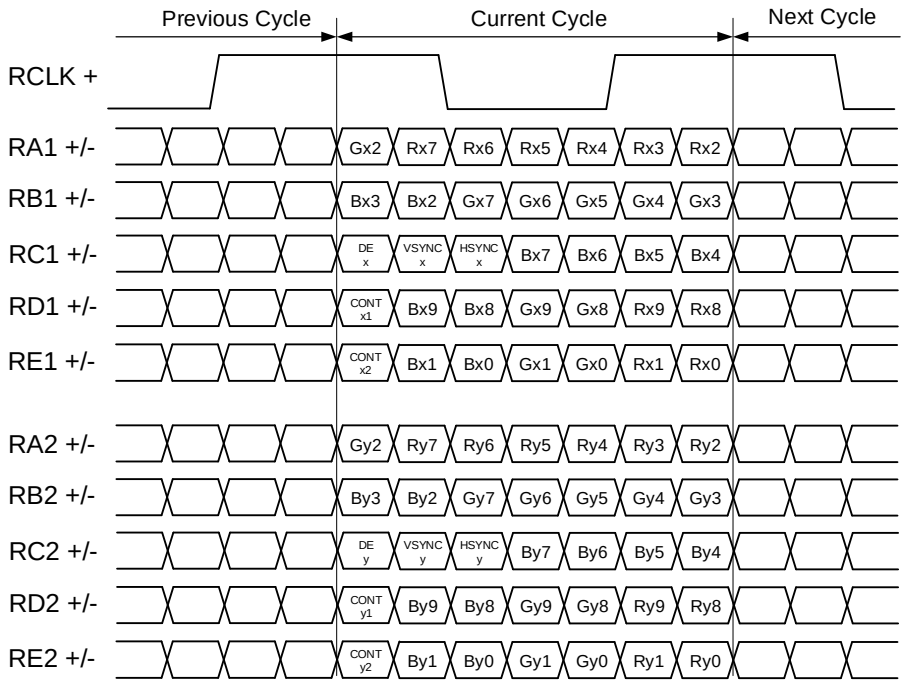


Figure 3. Input to Output signal flow



x, y : See the rightmost column of Table 2.

Figure 4. LVDS Inputs Mapped to LVCMOS Outputs (MAP=High)



x, y : See the rightmost column of Table 2.

Figure 5. LVDS Inputs Mapped to LVCMOS Outputs (MAP=Low)

Output clock-data phase adjustment

Depending on the voltage applied to the DK pin, the phase between the output clock and data can be controlled. Precisely, the delay time between the input clock and output data is constant, and the delay time between the input clock and output clock is controlled (**See Figure 9**).

Table 3. DK pin

MODE[1:0]	DK pin voltage	Offset [ns]
LL HH HL	V_{IL3}	0
	V_{IM3}	$-6\frac{t_{DOUT}}{28}$
	V_{IH3}	$6\frac{t_{DOUT}}{28}$
LH	V_{IL3}	0
	V_{IM3}	$-7\frac{t_{DOUT}}{28}$
	V_{IH3}	$7\frac{t_{DOUT}}{28}$

Output Control

The clock/data output status can be controlled by setting the Power Down and Output enable pins.
In the PWDN=High and OE=High settings, when no clock signal is input to the RCLK pin, all data output pins and the CLKOUT pin state is Low.

Table 4. Output Control

/PDWN	OE	Data Outputs	CLKOUT
L	L	Hi-Z	Hi-Z
L	H	Low	Low
H	L	Hi-Z	Hi-Z
H	H	Data signal	Clock signal

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power Supply Voltage	-0.3	+4.0	V
LVCMOS Input / Output Voltage	-0.3	VDD + 0.3	V
LVDS Input Voltage	-0.3	VDD + 0.3	V
Output Current	-30	+30	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	4.4	W

"Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. "Absolute Maximum Rating" value also includes behavior of overshooting and undershooting.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Parameter				Min	Typ	Max	Unit
All Supply Voltage (VDD, LVDD, PVDD, CVDD)				3.0	3.3	3.6	V
Operating Ambient Temperature				-40	-	85	°C
Clock Frequency	Dual-in / Dual-out Ta ≦ 70°C (Ta ≦ 85°C)		RCLK	8	-	135 (80)	MHz
			CLKOUT	8	-	135 (80)	
	Single-in / Single-out		RCLK	8	-	135	
			CLKOUT	8	-	135	
	Single-in / Dual-out		RCLK	8	-	135	
			CLKOUT	4	-	67.5	
	Dual-in / Single-out	DDR : Disable	RCLK	20	-	75	
			CLKOUT	40	-	150	
		DDR : Enable	RCLK	20	-	75	
			CLKOUT	20	-	75	

Power Consumption

Table 7. Supply Current

Parameter	Conditions			Max	Unit
Operating Current	RL=100Ω CL=8pF Test Signal Pattern (Figure 6)	Dual-in / Dual-out	RCLK=65MHz	366	mA
			RCLK=85MHz	453	mA
			RCLK=135MHz Ta ≦ 70°C	671	mA
		Single-in / Single-out	RCLK=65MHz	201	mA
			RCLK=85MHz	248	mA
			RCLK=135MHz	364	mA
		Single-in / Dual-out	RCLK=32.5MHz	138	mA
			RCLK=42.5MHz	164	mA
			RCLK=67.5MHz	233	mA
		Dual-in / Single-out (DDR : OFF)	RCLK=65MHz	146	mA
			RCLK=85MHz	165	mA
			RCLK=135MHz	210	mA
			RCLK=150MHz	223	mA
		Dual-in / Single-out (DDR : ON)	RCLK=32.5MHz	147	mA
			RCLK=42.5MHz	165	mA
			RCLK=67.5MHz	205	mA
			RCLK=75MHz	217	mA
Power Down Current	/PDWN=L			50	uA

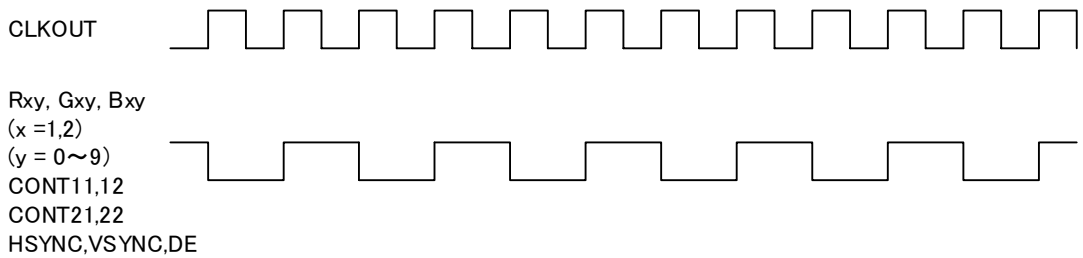


Figure 6. Test Signal Pattern

Output load limitation

Output load is limited so that Junction temperature is not over 125℃.

Calculating formula

$$Tj = Ta + \theta ja * P$$

P = VCC * (IOUTDT + IOUTCK + ICORE)
IOUTDT = 1/2 * FCLK * VCC * CLOAD * n
IOUTCK = FCLK * VCC * CLOAD

Tj	: Junction temperature ≦ 125℃
Ta	: Ambient temperature ≦ 70℃
θ ja	: Package thermal resistance = 22 [℃ /W]
ICORE	: Supply Current except all output buffers = 520mA
IOUTDT	: Supply Current only output buffers of data output. (R1,G1,B1,R2,G2,B2,HSYNC,VSYNC,DE,CONT11,CONT12,CONT21,CONT22)
IOUTCK	: Supply Current only output buffer of CLKOUT.
FCLK	: CLKOUT Frequency
n	: 67 (Number of data output pin)

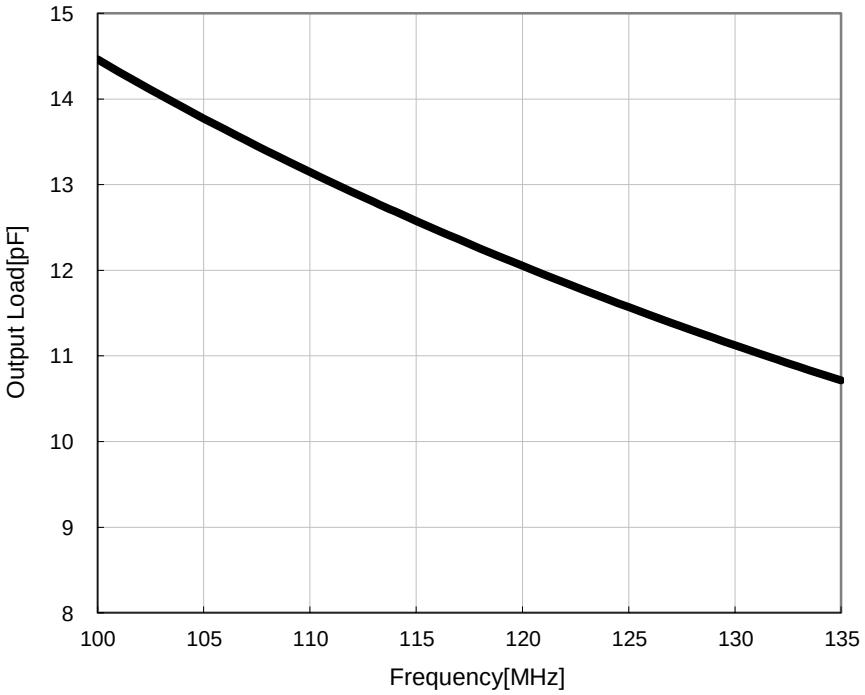


Figure 7. Output Load Limitation

Electrical Characteristics

Table 8. DC Specifications

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
LVCMOS DC Specifications						
V_{IH}	LVCMOS Input High Level Voltage		2.0	-	VCC	V
V_{IL}	LVCMOS Input Low Level Voltage		GND	-	0.8	V
V_{IH3}	3-level Input High Level Voltage		0.8 ×VCC	-	VCC	V
V_{IM3}	3-level Input Middle Level Voltage		0.4 ×VCC	-	0.6 ×VCC	V
V_{IL3}	3-level Input Low Level Voltage		GND	-	0.2 ×VCC	V
V_{OH}	LVCMOS Output High Level Voltage	I_{OH}=-8mA	2.4	-	-	V
V_{OL}	LVCMOS Output Low Level Voltage	I_{OH}=8mA	-	-	0.4	V
I_{IL}	Input Leakage Current	V_{IN}=GND~VDD	-	-	±10	uA
I_{IL3}	3-level Input Leakage Current	V_{IN}=GND~VDD	-	-	±10	uA
LVDS DC Specifications						
V_{TH}	Differential Input High Threshold	VIC=1.2V	-	-	100	mV
V_{TL}	Differential Input Low Threshold	VIC=1.2V	-100	-	-	mV
I_{ILD}	Differential Input Leakage Current	V_{IN}=0V / 2.4V	-	-	30	uA

* Typ values are at the conditions of VCC=LVCC=PVCC=CVCC=3.3V and TA = +25ºC

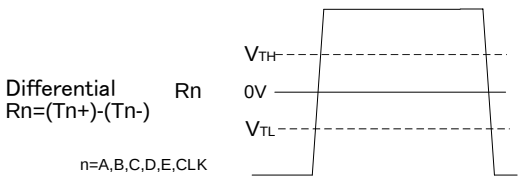


Figure 8. LVDS Input Threshold Voltage

Switching Characteristics

Table 9. AC Specifications

Symbol	Parameters	Conditions	Min	Typ*	Max	Units
LVCMOS AC Specifications						
t_{RCP}	CLKOUT Period		6.67	-	250	ns
t_{RCH}	CLKOUT High Time		-	$0.5\times t_{RCP}$	-	ns
t_{RCL}	CLKOUT Low Time		-	$0.5\times t_{RCP}$	-	ns
t_{RS}	Data Setup time to CLKOUT		$0.45\times t_{RCP}$ -0.45	-	-	ns
t_{RH}	Data Hold time to CLKOUT		$0.45\times t_{RCP}$ -0.45	-	-	ns
t_{TLH}	LVCMOS Output Low to High Transition Time	C_L=8pF, 20%-80%	-	0.7	1.0	ns
t_{THL}	LVCMOS Output High to Low Transition Time	C_L=8pF, 80%-20%	-	0.7	1.0	ns
LVDS AC Specifications						
t_{RCIP}	RCLK Period		7.4	-	125.0	ns
t_{RCIH}	Differential RCLK High Time		$2\times t_{RCIP}/7$	-	$5\times t_{RCIP}/7$	ns
t_{RCIL}	Differential RCLK Low Time		$2\times t_{RCIP}/7$	-	$5\times t_{RCIP}/7$	ns
t_{SK}	Receiver Skew Margin	t_{RCIP}=65MHz	-	-	650	ps
		t_{RCIP}=85MHz	-	-	450	ps
		t_{RCIP}=108MHz	-	-	250	ps
		t_{RCIP}=135MHz	-	-	170	ps
t_{RIP1}	Input Data Position1		$-t_{SK}$	0.0	$+t_{SK}$	ns
t_{RIP0}	Input Data Position 0		$t_{RCIP}/7$ $-t_{SK}$	$t_{RCIP}/7$	$t_{RCIP}/7$ $+t_{SK}$	ns
t_{RIP6}	Input Data Position6		$2\times t_{RCIP}/7$ $-t_{SK}$	$2\times t_{RCIP}/7$	$2\times t_{RCIP}/7$ $+t_{SK}$	ns
t_{RIP5}	Input Data Position5		$3\times t_{RCIP}/7$ $-t_{SK}$	$3\times t_{RCIP}/7$	$3\times t_{RCIP}/7$ $+t_{SK}$	ns
t_{RIP4}	Input Data Position4		$4\times t_{RCIP}/7$ $-t_{SK}$	$4\times t_{RCIP}/7$	$4\times t_{RCIP}/7$ $+t_{SK}$	ns
t_{RIP3}	Input Data Position3		$5\times t_{RCIP}/7$ $-t_{SK}$	$5\times t_{RCIP}/7$	$5\times t_{RCIP}/7$ $+t_{SK}$	ns
t_{RIP2}	Input Data Position2		$6\times t_{RCIP}/7$ $-t_{SK}$	$6\times t_{TCOP}/7$	$6\times t_{RCIP}/7$ $+t_{SK}$	ns
Delay Time						
t_{RPLL}	PLL Lock Time		-	-	10	ms
t_{RPD}	Power On to /PDWN High		0	-	-	ns
t_{RCD}	RCLK to CLKOUT Delay	Dual Link mode, DK=Low, t_{RCIP}=13.3ns	89.7	-	94	ns
DE Input requirment						
t_{DEINT}	DE Input Period	Single-in/Dual-out mode n="integer"	$4\times t_{TCIP}$	$2n\times t_{TCIP}$	-	ns
t_{DEH}	DE High Time	Single-in/Dual-out mode m="integer"	$2\times t_{TCIP}$	$2m\times t_{TCIP}$	-	ns
t_{DEINT}	DE Low Time	Single-in/Dual-out mode	$2\times t_{TCIP}$	-	-	ns

* Typ values are at the conditions of VCC=LVCC=PVCC=CVCC=3.3V and TA = +25ºC

AC Timing Diagram

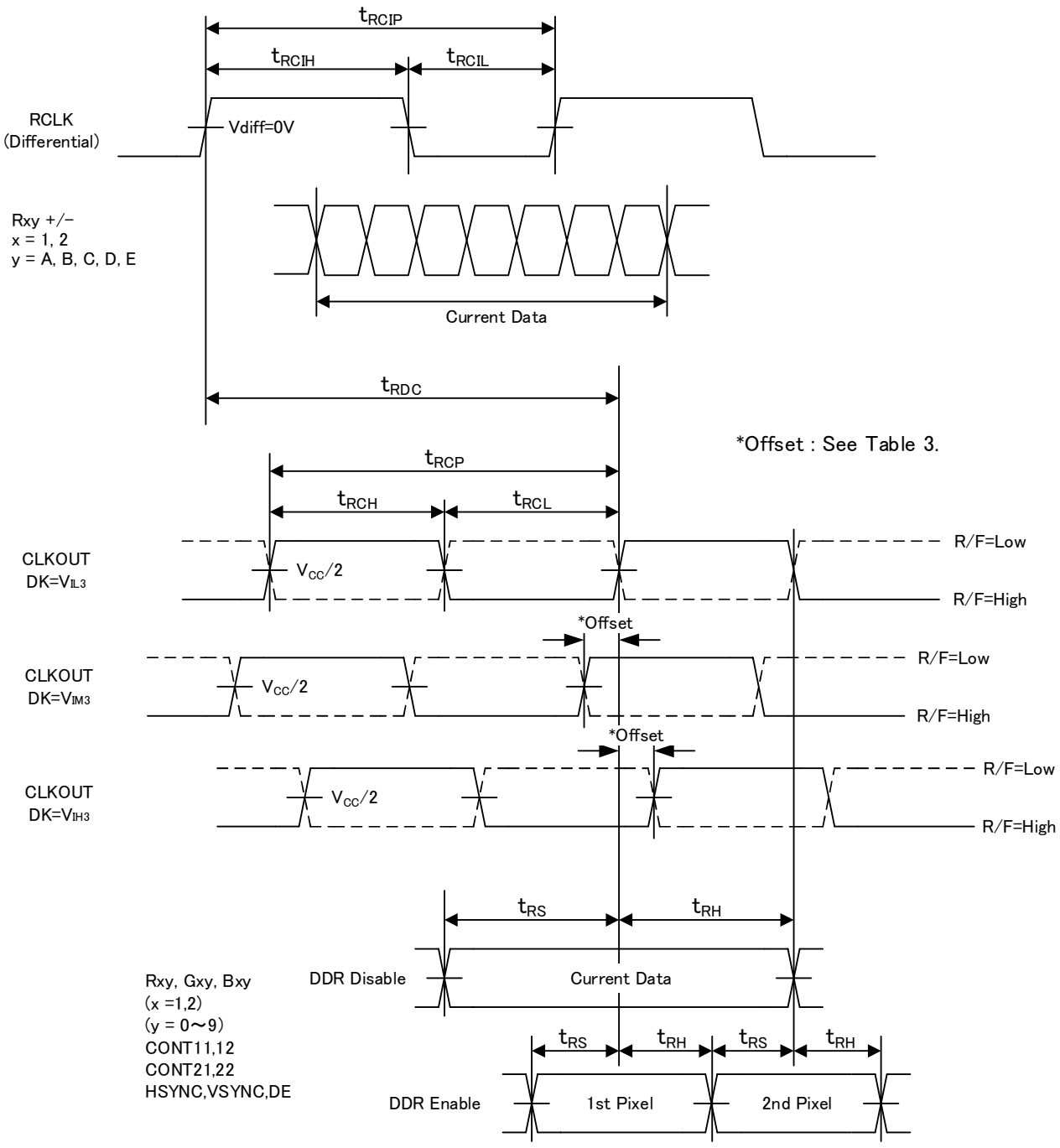


Figure 9. Input to Output timing

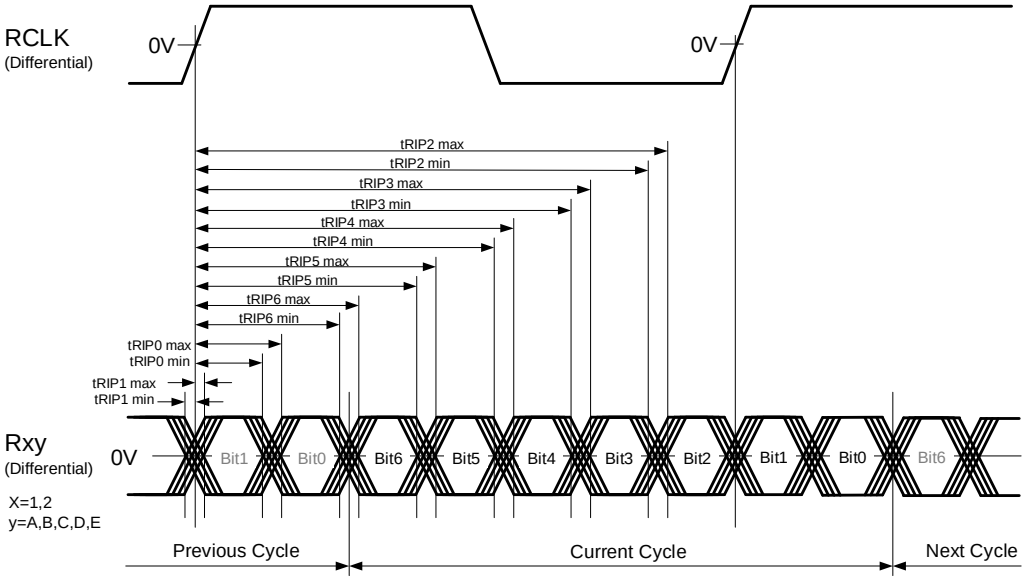


Figure 10. LVDS Input Data Position

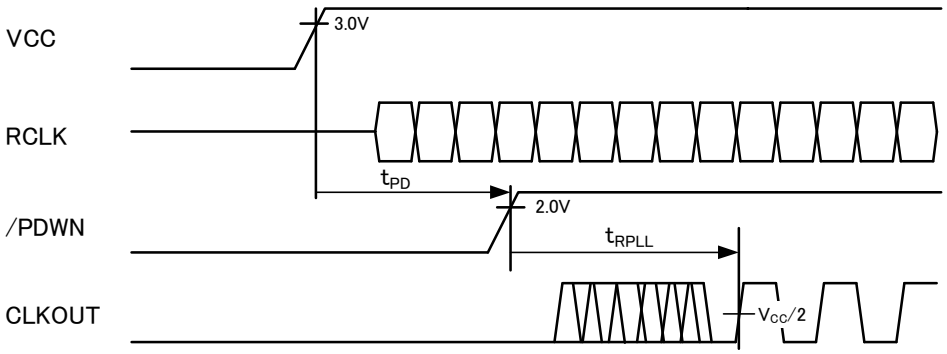


Figure 11. Power on Sequence

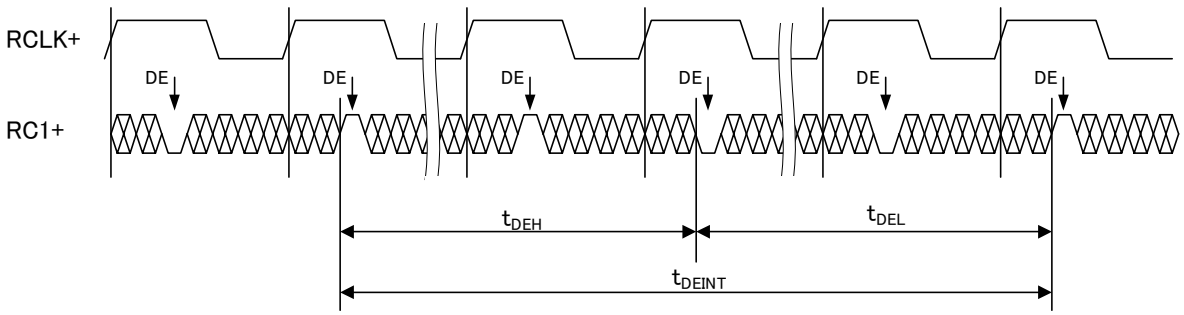


Figure 12. Data Enable (DE) signal input timing requirement

Notes

1) Cable Connection and Disconnection

Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which LVDS-Tx and THC63LVD1024 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

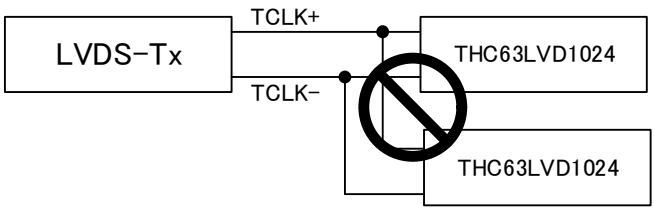


Figure 13. Multi Drop Connection

4) Asynchronous use

Asynchronous using such as following system is not recommended.

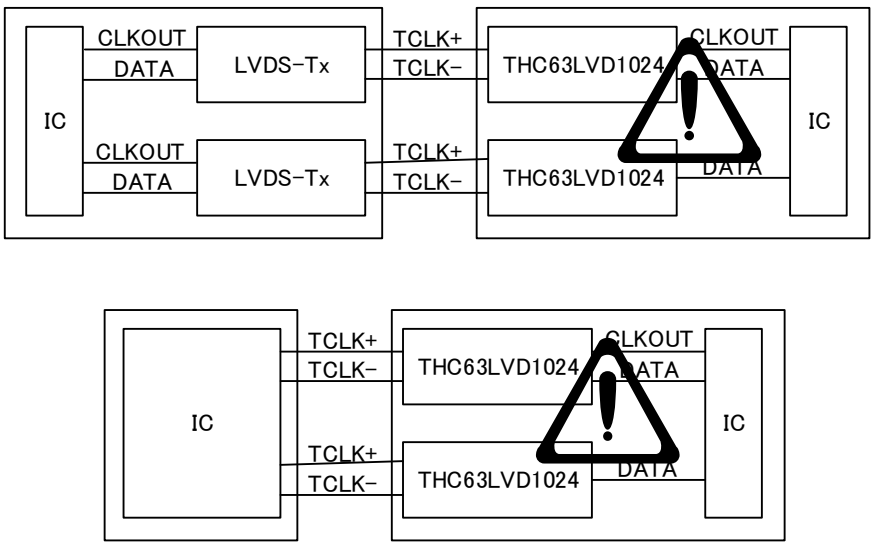
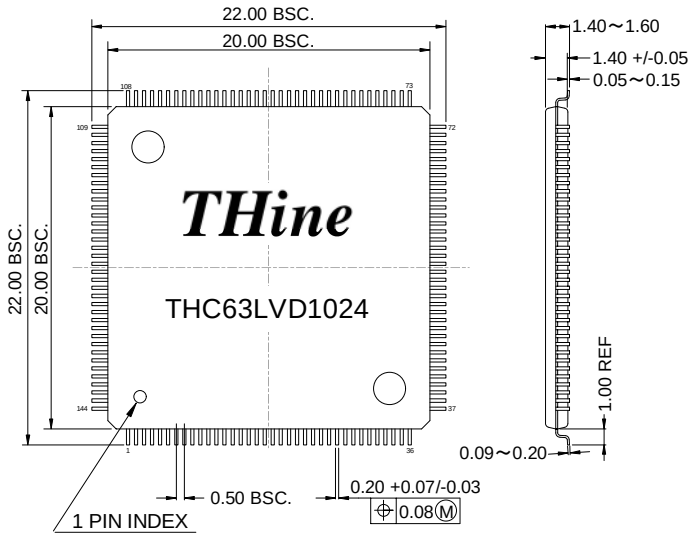
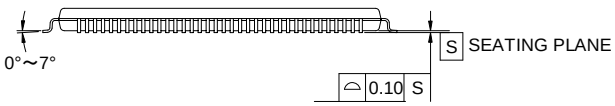


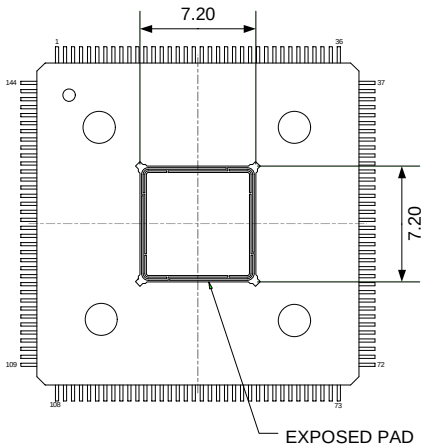
Figure 14. Asynchronous Use

Package



TOP VIEW





BOTTOM VIEW

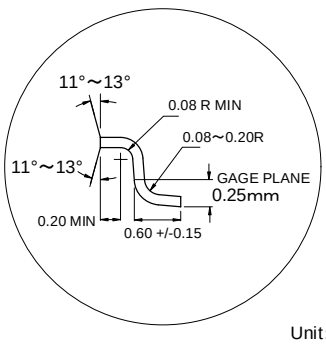


Figure 15. Package Diagram

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2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently fail-safe design principles such as redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

10. This product must be stored according to storage method which is specified in this specifications. THine accepts no liability whatsoever for any damage or loss caused to the user due to any storage not according to above-mentioned method.

11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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