THC63LVDR84B

24bit COLOR LVDS RECEIVER (Rising Edge Clock)

General Description

The THC63LVDR84B receiver supports wide VCC range as 2.5 to 3.6V. At single 2.5V supply, the THC63LVDR84B reduces EMI and power consumption.
The THC63LVDR84B converts the four LVDS data streams back into 24bits of CMOS/TTL data with Rising edge clock. At a transmit clock frequency of 85MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted at an effective rate of 2.38Gbps.

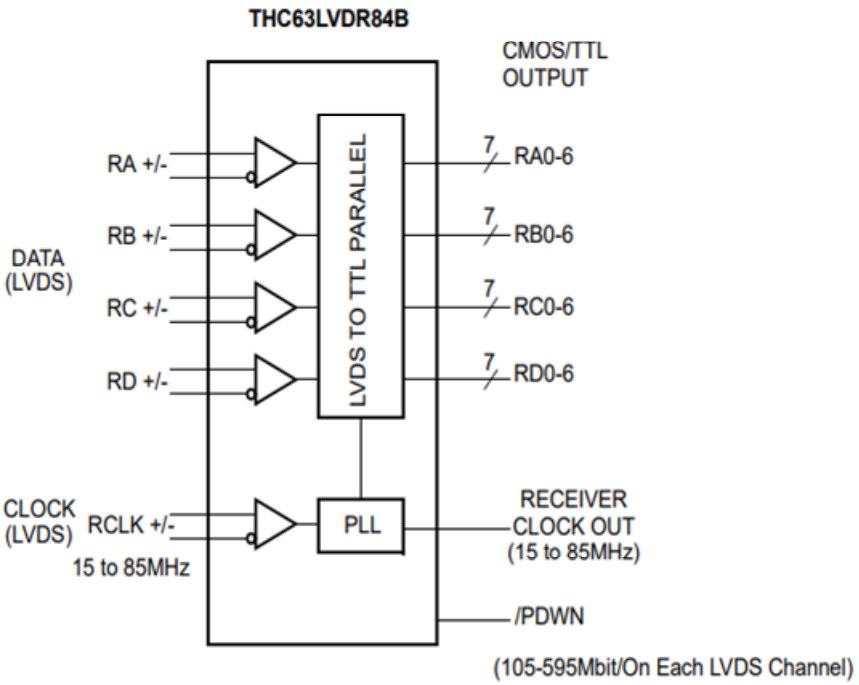
Application

- Medium and Small Size Panel
- Tablet PC / Notebook PC
- Security Camera / Industrial Camera
- Multi Function Printer
- Industrial Equipment
- Medical Equipment Monitor

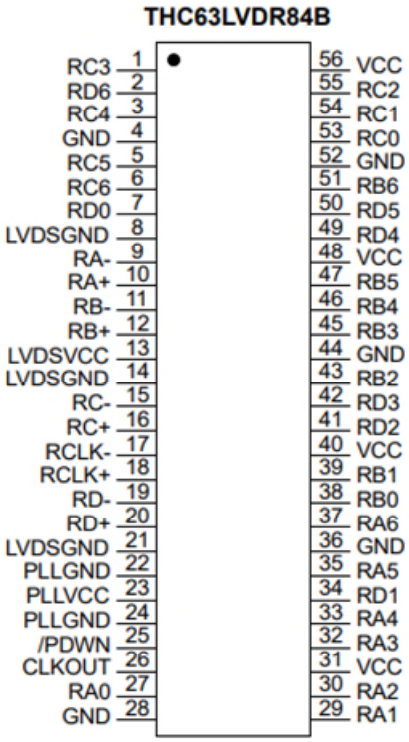
Features

- 1:7 LVDS to CMOS/TTL De-Serializer
- Operating Temperature Range : -10 to +70°C
- Spread Spectrum Clocking Tolerant up to 100kHz Frequency Modulation and +/-2.5% Deviations.
- Input Clock Range: 15 to 85MHz
- 56pin TSSOP Package
- Power Down Mode.
- Rising Edge Clock
- EU RoHS Compliant.

Block Diagram



Pin Diagram



Pin Description

Pin Name	Pin #	Direction	Type	Description
RA+, RA-	10, 9	Input	LVDS	4ch Serial Data Inputs
RB+, RB-	12, 11			
RC+, RC-	16, 15			
RD+, RD-	20, 19			
RCLK+, RCLK-	18, 17			Clock Inputs
RA0 ~ RA6	27, 29, 30, 32, 33, 35, 37	Output	CMOS/TTL	28bits Parallel Data Outputs
RB0 ~ RB6	38, 39, 43, 45, 46, 47, 51			
RC0 ~ RC6	53, 54, 55, 1, 3, 5, 6			
RD0 ~ RD6	7, 34, 41, 42, 49, 50, 2			
CLKOUT	26			Clock Output
/PDWN	25	Input		H : Normal Operation L : Power Down (all outputs are pulled to ground)
VCC	31, 40, 48, 56	Power	-	Digital circuit and CMOS/TTL I/O Power Supply
GND	4, 28, 36, 44, 52			Digital circuit and CMOS/TTL I/O Ground
LVDSVCC	13			LVDS circuit and input buffer Power Supply
LVDSGND	8, 14, 21			LVDS circuit and input buffer Ground
PLLVCC	23			PLL circuit Power Supply
PLLGND	22, 24			PLL circuit Ground

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (VCC)	-0.3	+4.0	V
CMOS/TTL Input Voltage	-0.3	VCC + 0.3	V
CMOS/TTL Output Voltage	-0.3	VCC + 0.3	V
LVDS Input Pin	-0.3	VCC + 0.3	V
Junction Temperature	-	+125	°C
Storage Temperature	-55	+150	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.9	W

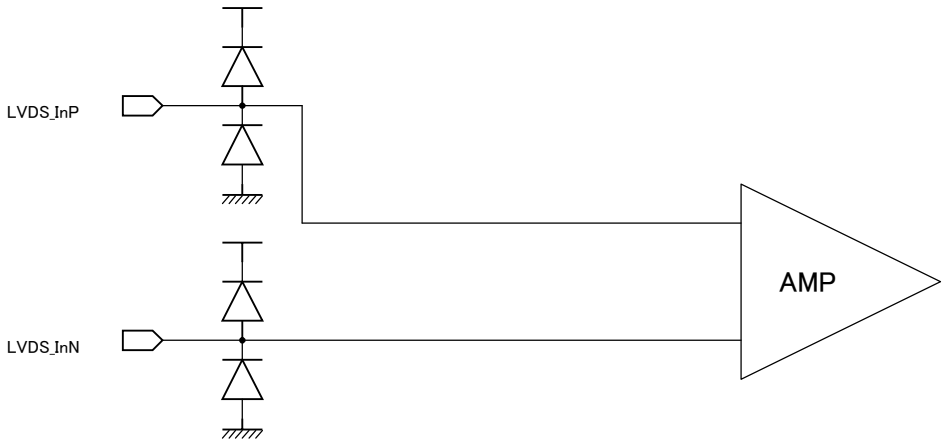
Recommended Operating Conditions

VCC=LVDSVCC=PLLVCC

Symbol	Parameter		Min	Typ	Max	Unit
-	All Supply Voltage		2.5	-	3.6	V
Ta	Operating Ambient Temperature		-10	+25	+70	°C
-	Clock Frequency	VCC = 2.5V to 2.7V	20	-	70	MHz
		VCC = 2.7V to 3.0V	15	-	70	MHz
		VCC = 3.0V to 3.6V	15	-	85	MHz

"Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
"Absolute Maximum Rating" value also includes behavior of overshooting and undershooting.

Equivalent LVDS Input Schematic Diagram



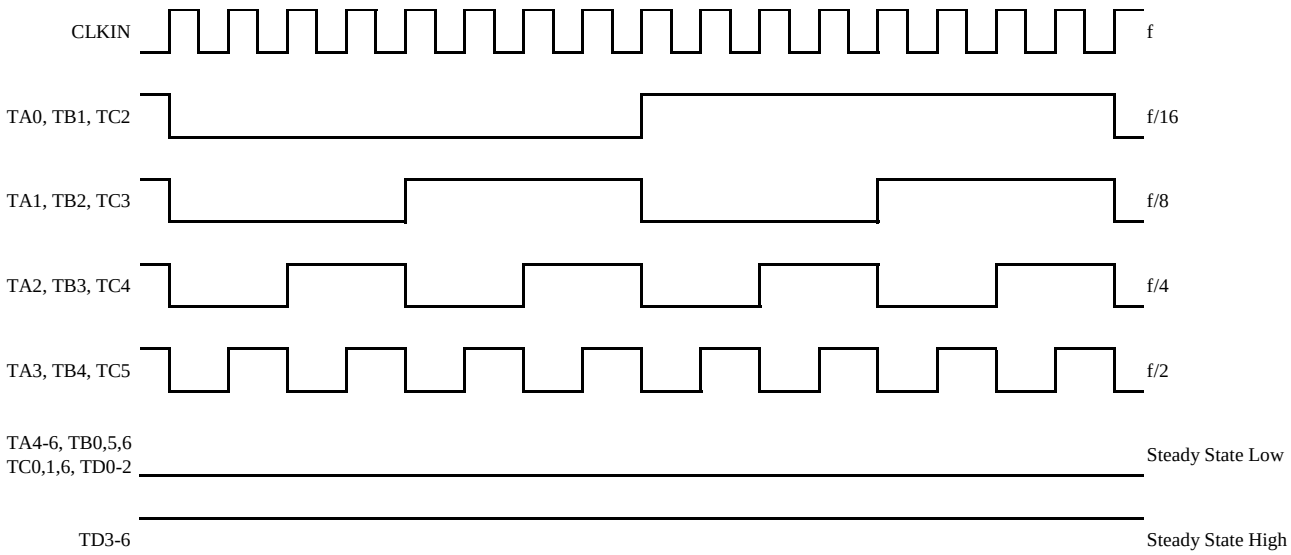
LVDS Input Schematic Diagram

Power Consumption

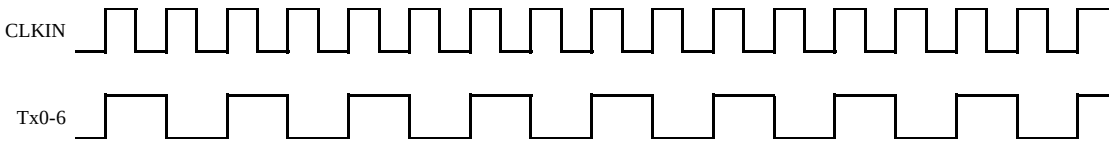
VCC=LVDSVCC=PLLVCC

Symbol	Parameter	Conditions	Typ*	Max	Unit
I_{RCCG}	LVDS Receiver Operating Current 16 Gray Scale Pattern	RL=100Ω, C_{Load}=8pF, f=65MHz, VCC=3.3V	41	53	mA
		RL=100Ω, C_{Load} =8pF, f=85MHz, VCC=3.3V	52	64	mA
		RL=100Ω, C_{Load} =8pF, f=65MHz, VCC=2.5V	30	42	mA
I_{RCCW}	LVDS Receiver Operating Current Worst Case Pattern	RL=100Ω, C_{Load} =8pF, f=65MHz, VCC=3.3V	72	94	mA
		RL=100Ω, C_{Load} =8pF, f=85MHz, VCC=3.3V	84	96	mA
		RL=100Ω, C_{Load} =8pF, f=65MHz, VCC=2.5V	42	64	mA
I_{RCCS}	LVDS Receiver Power Down Current	/PDWN=L	-	10	µA

*Typ values are at the conditions of Ta = +25ºC



16 Grayscale Pattern



x=A,B,C,D

Worst Case Pattern

Electrical Characteristics

CMOS/TTL DC Specifications

VCC=LVDSVCC=PLLVCC

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{IH}	High Level Input Voltage	-	2.0	-	VCC	V
V_{IL}	Low Level Input Voltage	-	GND	-	0.8	V
V_{OH1}	High Level Output Voltage	VCC = 3.0V to 3.6V I_{OH} = -4mA	2.4	-	-	V
V_{OL1}	Low Level Output Voltage	VCC = 3.0V to 3.6V I_{OL} = 4mA	-	-	0.4	V
V_{OH2}	High Level Output Voltage	VCC = 2.5V to 3.0V I_{OH} = -2mA	2.1	-	-	V
V_{OL2}	Low Level Output Voltage	VCC = 2.5V to 3.0V I_{OL} = 2mA	-	-	0.4	V
I_{IN}	Input Current	GND ≤ V_{IN} ≤ VCC	-	-	±10	μA

LVDS DC Specifications

VCC=LVDSVCC=PLLVCC

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{TH}	Differential Input High Threshold	RL=100Ω, VIC=+1.2V	-	-	100	mV
V_{TL}	Differential Input Low Threshold		-100	-	-	mV
I_{IN}	Input Current	V_{IN} = +2.4 / 0V VCC = 3.6V	-	-	±10	μA

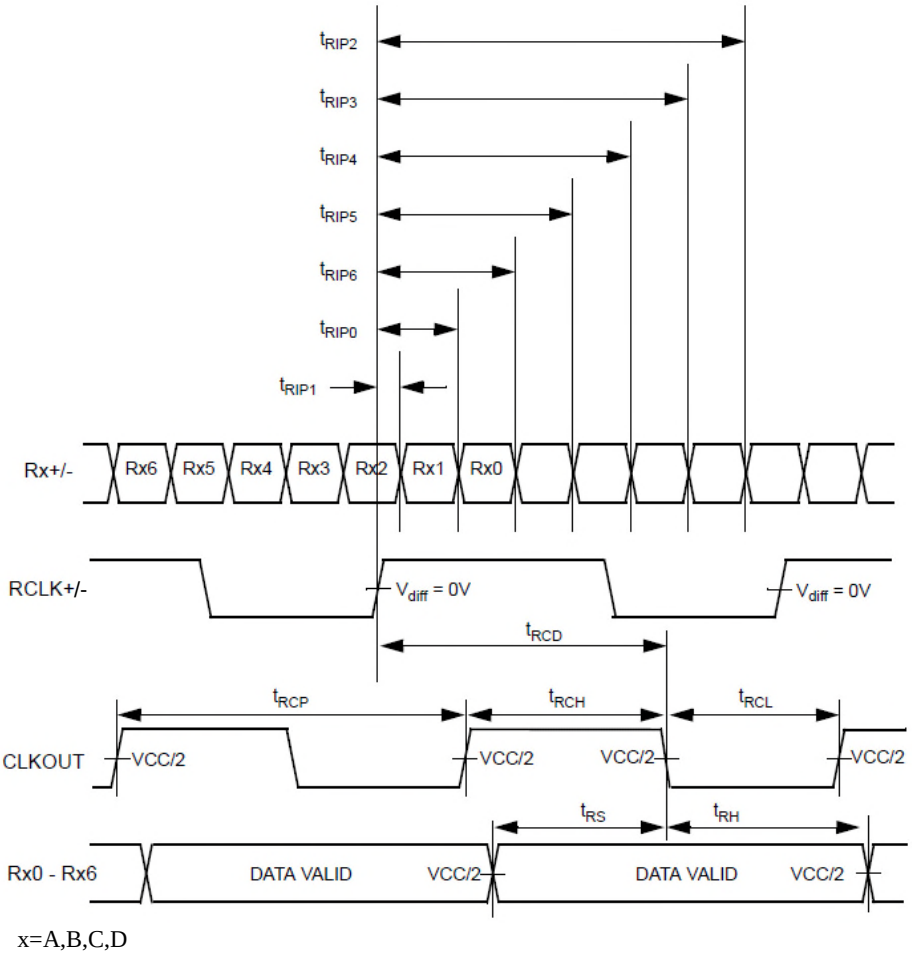
CMOS/TTL & LVDS AC Specifications

VCC=LVDSVCC=PLLVCC

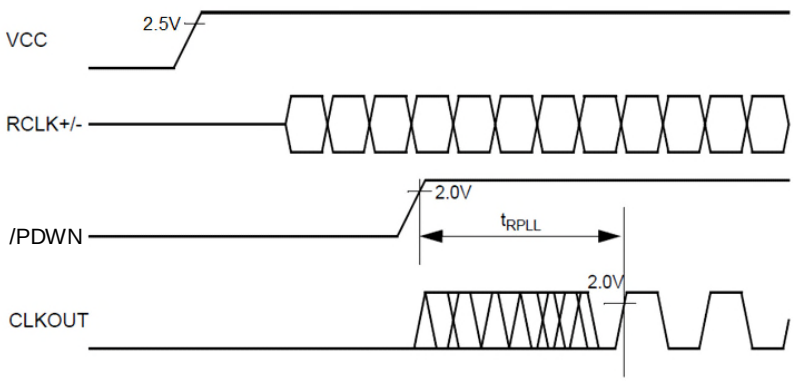
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RCP}	CLKOUT Transition Time	VCC = 2.5V to 2.7V	14.3	T	50.0	ns
		VCC = 2.7V to 3.0V	14.3	T	66.6	
		VCC = 3.0V to 3.6V	11.8	T	66.6	
t_{RCH}	CLKOUT High Time		-	4T/7	-	ns
t_{RCL}	CLKOUT Low Time		-	3T/7	-	ns
t_{RCD}	RCLK IN to CLKOUT +/- Delay		-	5T/7	-	ns
t_{RS}	CMOS/TTL Data Setup to CLKOUT		0.35T - 0.3	-	-	ns
t_{RH}	CMOS/TTL Data Hold from CLKOUT		0.45T – 1.6	-	-	ns
t_{TLH}	CMOS/TTL Low to High Transition Time	C_{Load}=8pF, 20-80%	-	2.0	3.0	ns
t_{THL}	CMOS/TTL High to Low Transition Time	C_{Load}=8pF, 80-20%	-	1.8	3.0	ns
t_{RIP1}	LVDS Input Data Position0	T=11.76ns	-0.4	0.0	+0.4	ns
t_{RIP0}	LVDS Input Data Position1	T=11.76ns	T/7-0.4	T/7	T/7+0.4	ns
t_{RIP6}	LVDS Input Data Position2	T=11.76ns	2T/7-0.4	2T/7	2T/7+0.4	ns
t_{RIP5}	LVDS Input Data Position3	T=11.76ns	3T/7-0.4	3T/7	3T/7+0.4	ns
t_{RIP4}	LVDS Input Data Position4	T=11.76ns	4T/7-0.4	4T/7	4T/7+0.4	ns
t_{RIP3}	LVDS Input Data Position5	T=11.76ns	5T/7-0.4	5T/7	5T/7+0.4	ns
t_{RIP2}	LVDS Input Data Position6	T=11.76ns	6T/7-0.4	6T/7	6T/7+0.4	ns
t_{RPLL}	Phase Lock Loop Set	T=11.76ns	-	-	10.0	ms

*Typ values are at the conditions of VCC/LVDSVCC/PLLVCC=3.3V and Ta = +25ºC

AC Timing Diagram

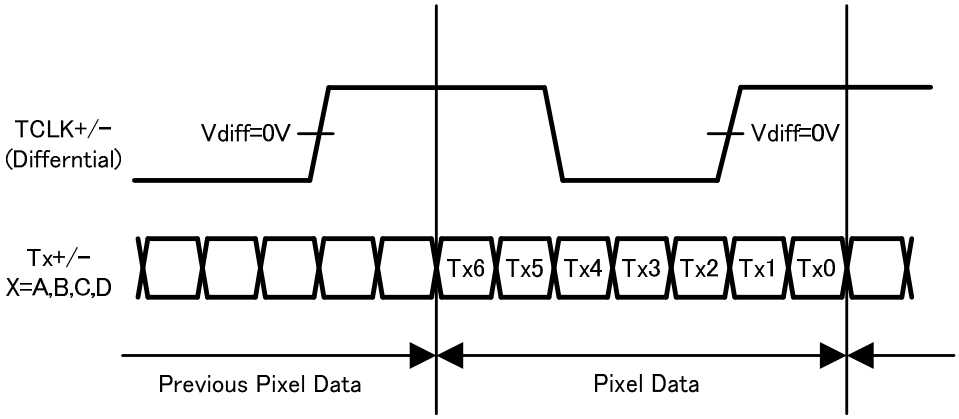


Data and Clock Input to Output AC Timing Diagram



Power on Sequence

LVDS Data Mapping



LVDS Data Mapping

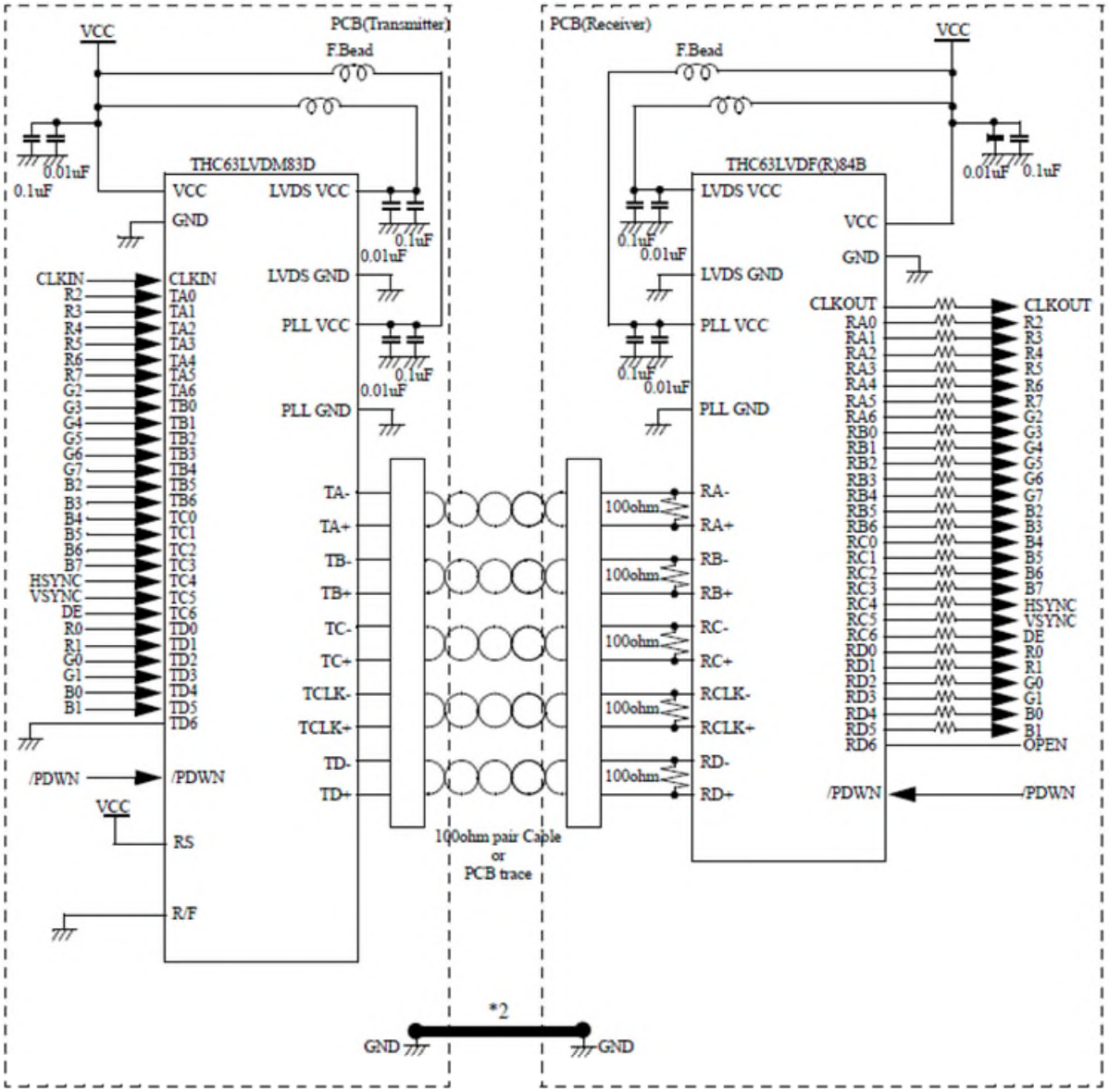
Pixel Data Mapping for JEIDA Format (6bit, 8bit Application)

TX Pin	6bit	8bit	RX Pin
TA0	R2	R2	RA0
TA1	R3	R3	RA1
TA2	R4	R4	RA2
TA3	R5	R5	RA3
TA4	R6	R6	RA4
TA5	R7	R7	RA5
TA6	G2	G2	RA6
TB0	G3	G3	RB0
TB1	G4	G4	RB1
TB2	G5	G5	RB2
TB3	G6	G6	RB3
TB4	G7	G7	RB4
TB5	B2	B2	RB5
TB6	B3	B3	RB6
TC0	B4	B4	RC0
TC1	B5	B5	RC1
TC2	B6	B6	RC2
TC3	B7	B7	RC3
TC4	Hsync	Hsync	RC4
TC5	Vsync	Vsync	RC5
TC6	DE	DE	RC6
TD0	-	R0	RD0
TD1	-	R1	RD1
TD2	-	G0	RD2
TD3	-	G1	RD3
TD4	-	B0	RD4
TD5	-	B1	RD5
TD6	-	N/A	RD6

Pixel Data Mapping for VESA Format (6bit, 8bit Application)

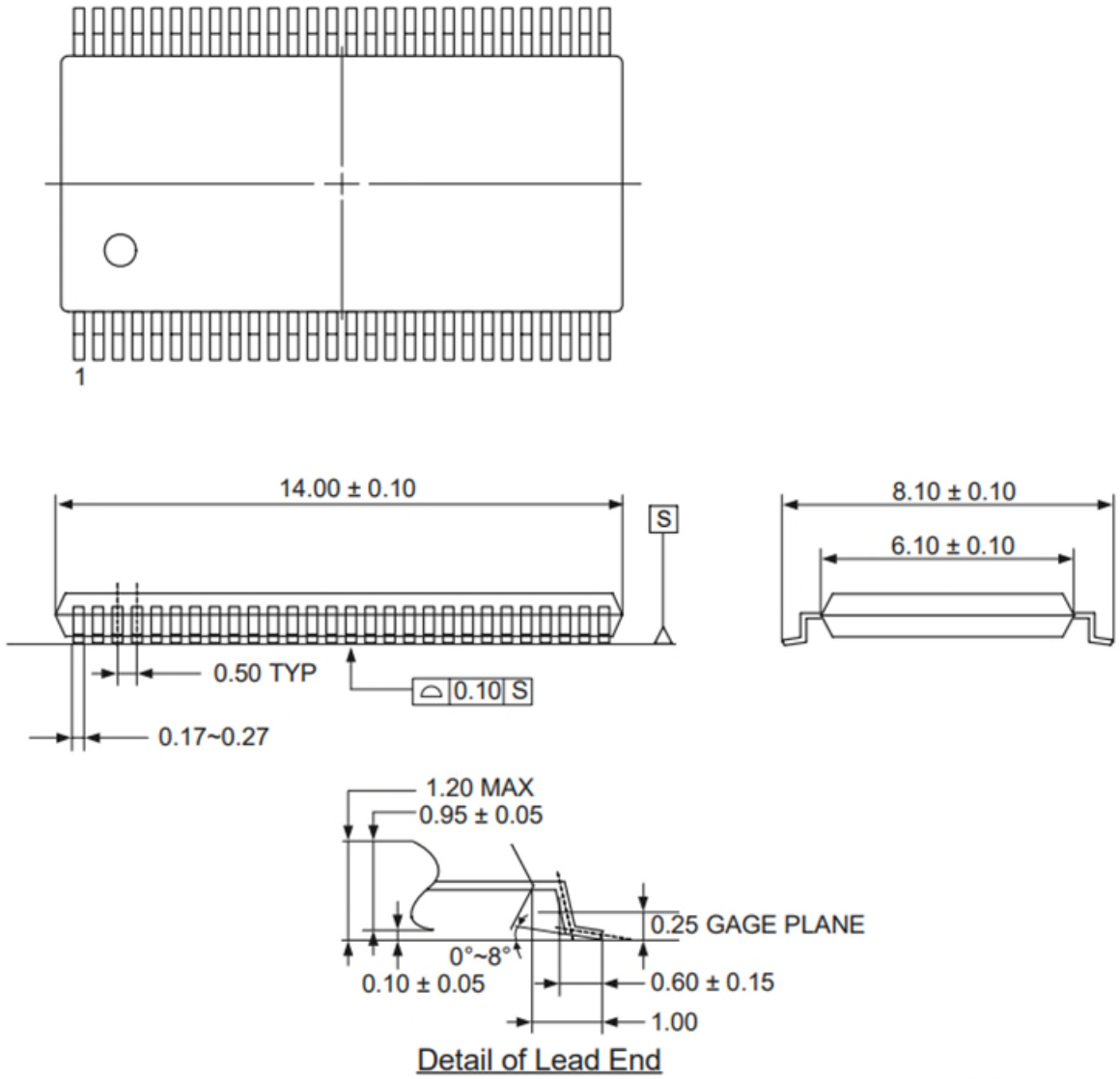
TX Pin	6bit	8bit	RX Pin
TA0	R0	R0	RA0
TA1	R1	R1	RA1
TA2	R2	R2	RA2
TA3	R3	R3	RA3
TA4	R4	R4	RA4
TA5	R5	R5	RA5
TA6	G0	G0	RA6
TB0	G1	G1	RB0
TB1	G2	G2	RB1
TB2	G3	G3	RB2
TB3	G4	G4	RB3
TB4	G5	G5	RB4
TB5	B0	B0	RB5
TB6	B1	B1	RB6
TC0	B2	B2	RC0
TC1	B3	B3	RC1
TC2	B4	B4	RC2
TC3	B5	B5	RC3
TC4	Hsync	Hsync	RC4
TC5	Vsync	Vsync	RC5
TC6	DE	DE	RC6
TD0	-	R6	RD0
TD1	-	R7	RD1
TD2	-	G6	RD2
TD3	-	G7	RD3
TD4	-	B6	RD4
TD5	-	B7	RD5
TD6	-	N/A	RD6

Typical Connection Diagram



Typical Connection Diagram with JEIDA Format

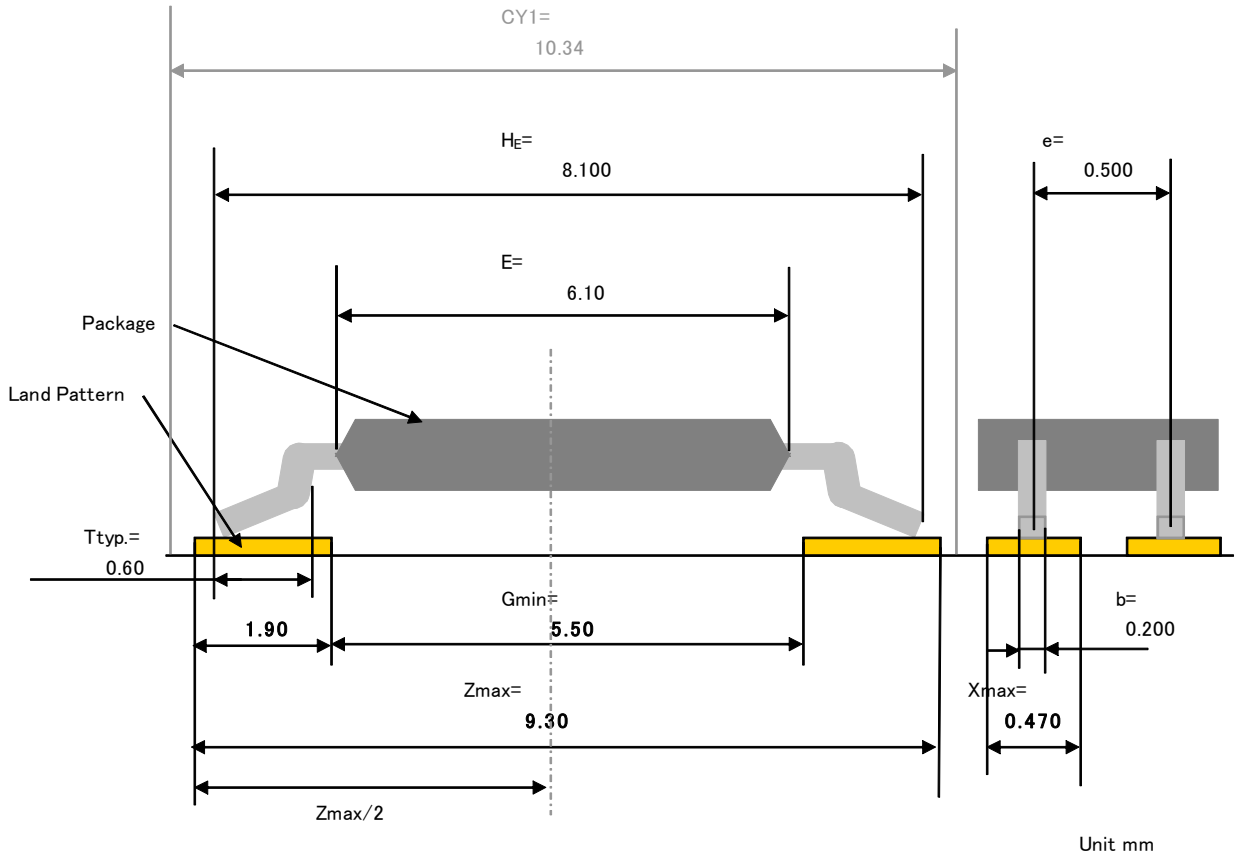
Package



Detail of Lead End

Unit:mm

Reference Land Pattern



The recommendation mounting method of THine device is reflow soldering.
The reference pattern is using the calculation result on condition of reflow soldering.

Notes
This land pattern design is a calculated value based on JEITA ET-7501.
Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc… The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.

Notes

1) Cable Connection and Disconnection

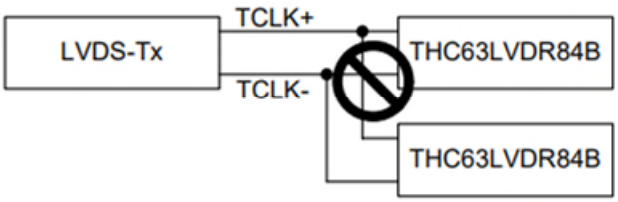
Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which LVDS Tx device and THC63LVDR84B on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

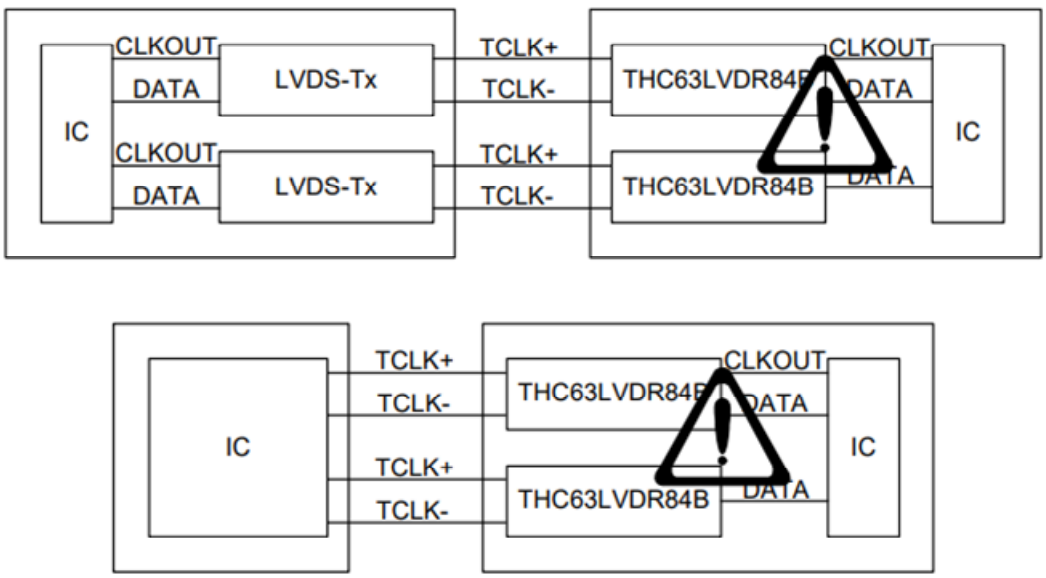
3) Multi Drop Connection

Multi drop connection is not recommended.



4) Asynchronous use

Asynchronous using such as following systems is not recommended.



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