THC63LVDF84C

24bit Color LVDS Receiver (Falling Edge Strobe Output)

General Description

The THC63LVDF84C receiver supports wide temperature range as -40 to +85°C, and wide frequency range as 8 to 112MHz.
The THC63LVDF84C converts the four LVDS data streams back into 24bits of LVCMOS data with falling edge clock. At a transmit clock frequency of 112MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, etc.) are transmitted at an effective rate of 3.1Gbps.

Application

- Medium and Small Size Panel
- Security Camera
- Multi Function Printer
- Machine Vision (Frame Grabber Board)
- Medical Equipment Monitor

Features

- 1:7 LVDS to LVCMOS Deserializer
- Operating Temperature Range : -40 to +85°C
- No Special Start-up Sequence Required
- Spread Spectrum Clocking Tolerant up to 100kHz Frequency Modulation and +/-2.5% Deviations
- Pixel Clock Range: 8 to 112MHz
- 56pin TSSOP Package
- Power Down Mode
- Falling Edge Strobe Output
- EU RoHS Compliant

Recommended LVDS Transmitter ICs

- THC63LVDM83D
- THC63LVDM87

Block Diagram

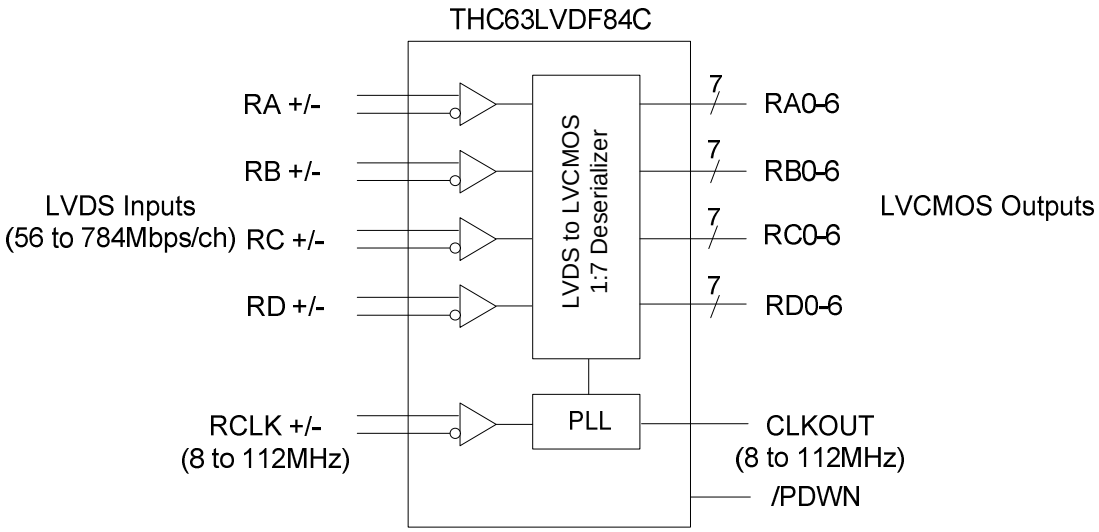


Figure 1. Block Diagram

Pin Diagram

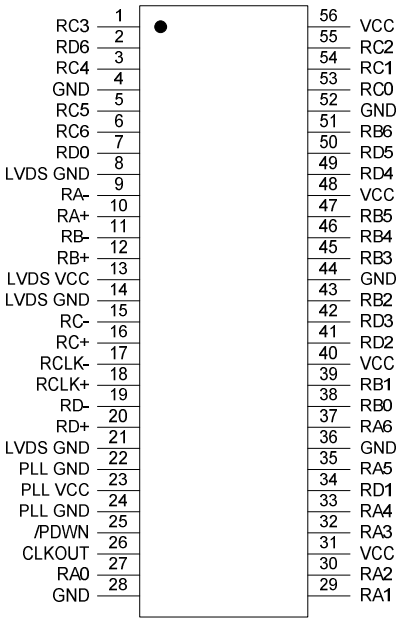


Figure 2. Pin Diagram

Pin Description

Pin Name	Pin #	Direction	Type	Description
RA+, RA-	10, 9	Input	LVDS	LVDS Data Inputs
RB+, RB-	12, 11			
RC+, RC-	16, 15			
RD+, RD-	20, 19			
RCLK+, RCLK-	18, 17			LVDS Clock Inputs
RA0 ~ RA6	27, 29, 30, 32, 33, 35, 37	Output	LVCMOS	Pixel Data Outputs
RB0 ~ RB6	38, 39, 43, 45, 46, 47, 51			
RC0 ~ RC6	53, 54, 55, 1, 3, 5, 6			
RD0 ~ RD6	7, 34, 41, 42, 49, 50, 2			
CLKOUT	26			Pixel Clock Output
/PDWN	25	Input		H : Normal Operation L : Power Down (All outputs are pulled to ground)
VCC	31, 40, 48, 56	-	Power	Power Supply Pins for LVCMOS outputs and digital circuitry
GND	4, 28, 36, 44, 52			Ground Pins for LVCMOS outputs and digital circuitry
LVDS VCC	13			Power Supply Pins for LVDS inputs
LVDS GND	8, 14, 21			Ground Pins for LVDS inputs
PLL VCC	23			Power Supply Pins for PLL circuitry
PLL GND	22, 24			Ground Pins for PLL circuitry

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (VCC, LVDS VCC, PLL VCC)	-0.3	+4.0	V
LVCMOS Input Voltage	-0.3	VCC + 0.3	V
LVCMOS Output Voltage	-0.3	VCC + 0.3	V
LVDS Input Pin	-0.3	VCC + 0.3	V
Junction Temperature	-	+125	°C
Storage Temperature	-55	+150	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.9	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC33	All Supply Voltage(VCC, LVDS VCC, PLL VCC)	3.0	-	3.6	V
Ta	Operating Ambient Temperature	-40	+25	+85	°C
PCLK	RCLK and CLKOUT Clock Frequency	8	-	112	MHz

“Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics Table4, 5, 6, 7” specify conditions for device operation.
“Absolute Maximum Rating” value also includes behavior of overshooting and undershooting.

Equivalent LVDS Input Schematic Diagram

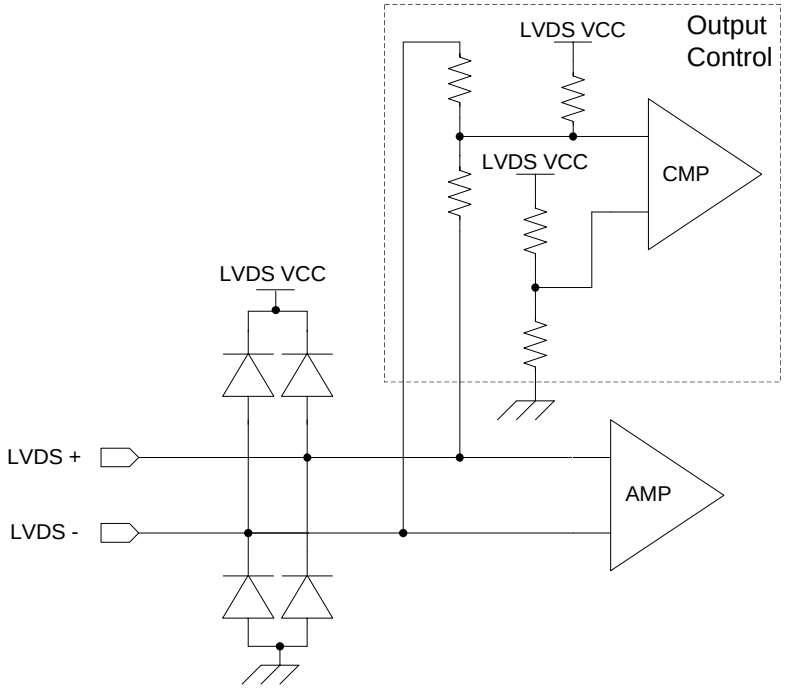


Figure 3. LVDS Input Schematic Diagram

Output Control

/PDWN	RCLK +/- Input	LVCMOS Output
H	Valid Clock	Active Clock & Data
H	Invalid Clock	Unfixed Clock & Data
H	Open or Hi-z	All Low
L	Don't Care	All Low

Power Consumption

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Typ*	Max	Unit
I_{RCCG}	LVDS Receiver Operating Current Gray Scale Pattern 16 (Fig.4)	CL=8pF, PCLK=65MHz, VCC33=3.3V	55	70	mA
		CL=8pF, PCLK=112MHz, VCC33=3.3V	90	110	mA
I_{RCCW}	LVDS Receiver Operating Current Worst Case Pattern(Fig.5)	CL=8pF, PCLK=65MHz, VCC33=3.3V	90	110	mA
		CL=8pF, PCLK=112MHz, VCC33=3.3V	130	160	mA
I_{RCCS}	LVDS Receiver Power Down Current	/PDWN=L	-	500	µA

*Typ values are at the conditions of Ta = +25ºC

16 Grayscale Pattern

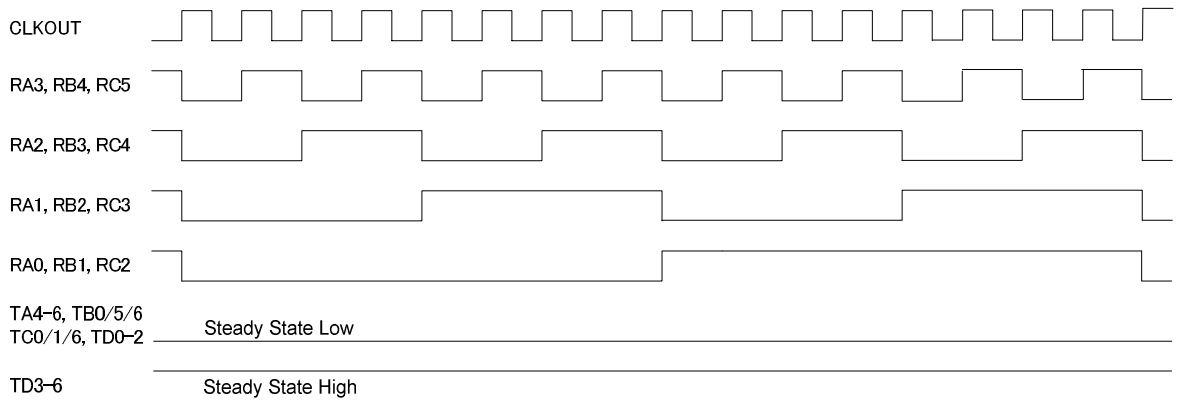


Figure 4. 16 Grayscale Pattern

Worst Case Pattern

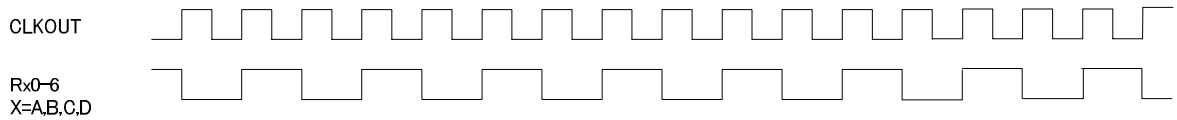


Figure 5. Worst Case Pattern

Electrical Characteristics

LVDS Receiver DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{TH}	Differential Input High Threshold	RL=100Ω, VIC=+1.2V	-	-	100	mV
V_{TL}	Differential Input Low Threshold		-100	-	-	mV
I_{IN}	Input Current	V_{IN}=+2.4 / 0V LVDS VCC=3.6V	-	-	±30	μA

LVCMOS DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	-	2.0	-	VCC	V
V_{IL}	Low Level Input Voltage	-	GND	-	0.8	V
V_{OH}	High Level Output Voltage	I_{OH}=-4mA (Data) I_{OH}=-8mA (Clock)	2.4	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL}=4mA (Data) I_{OL}=8mA (Clock)	-	-	0.4	V
I_{IN}	Input Current	GND ≤ V_{IN} ≤ VCC	-	-	±10	μA

LVCMOS Output Load Limitation

The output load is limited so that the junction temperature does not exceed 125°C.

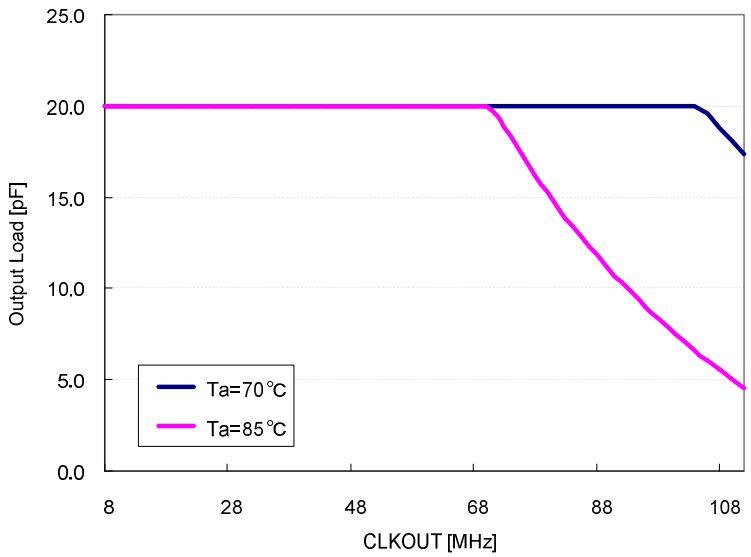


Figure 6. LVCMOS Output Load Limitation

Switching Characteristics

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter		Min	Typ*	Max	Unit
t_{RCP}	RCLK and CLKOUT Transition Time		8.92	T	125	ns
t_{RCH}	LVCMOS CLKOUT High Time		-	T/2	-	ns
t_{RCL}	LVCMOS CLKOUT Low Time		-	T/2	-	ns
t_{RCD}	RCLK IN to CLKOUT Delay		-	(3/14+3) × T	-	ns
t_{RS}	LVCMOS Data Setup to CLKOUT		0.35 × T - 0.3	-	-	ns
t_{RH}	LVCMOS Data Hold from CLKOUT		0.45 × T - 1.6	-	-	ns
t_{TLH}	LVCMOS Low to High Transition Time		-	0.7	1.0	ns
t_{THL}	LVCMOS High to Low Transition Time		-	0.7	1.0	ns
t_{SK}	LVDS Receiver Skew Margin	PCLK=65MHz	-0.55	-	0.55	ns
		PCLK=112MHz	-0.25	-	0.25	
t_{RIP1}	LVDS Input Data Position0		- t_{SK}	0.0	+ t_{SK}	ns
t_{RIP0}	LVDS Input Data Position1		T/7- t_{SK}	T/7	T/7+ t_{SK}	ns
t_{RIP6}	LVDS Input Data Position2		2T/7- t_{SK}	2T/7	2T/7+ t_{SK}	ns
t_{RIP5}	LVDS Input Data Position3		3T/7- t_{SK}	3T/7	3T/7+ t_{SK}	ns
t_{RIP4}	LVDS Input Data Position4		4T/7- t_{SK}	4T/7	4T/7+ t_{SK}	ns
t_{RIP3}	LVDS Input Data Position5		5T/7- t_{SK}	5T/7	5T/7+ t_{SK}	ns
t_{RIP2}	LVDS Input Data Position6		6T/7- t_{SK}	6T/7	6T/7+ t_{SK}	ns
t_{RPLL}	Phase Lock Loop Set		-	-	10.0	ms

*Typ values are at the conditions of VCC33=3.3V and Ta = +25ºC

AC Timing Diagrams

LVDS Input

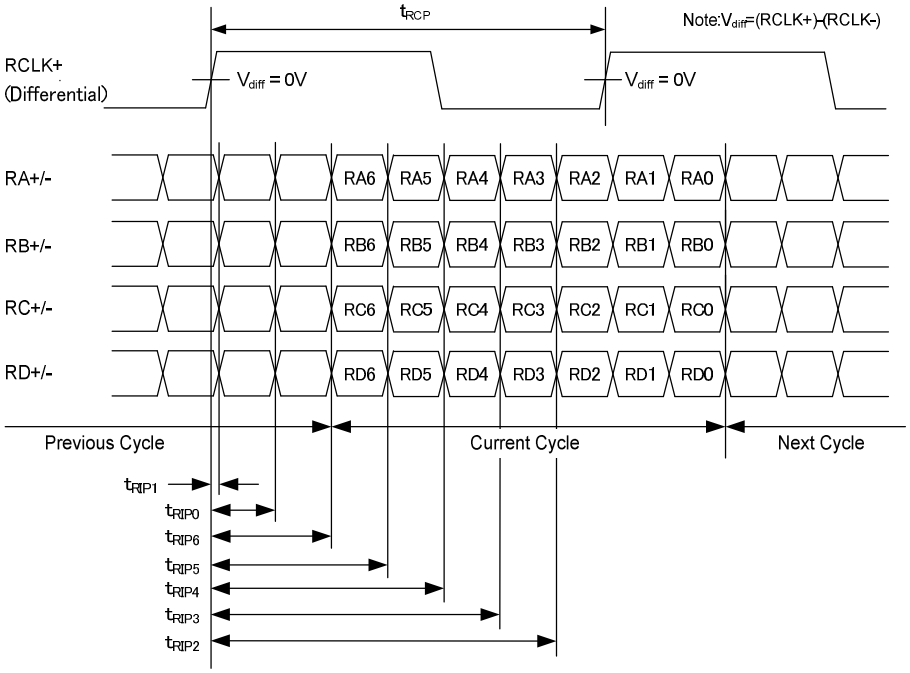


Figure 7. LVDS Input Data Position

LVCMOS Output

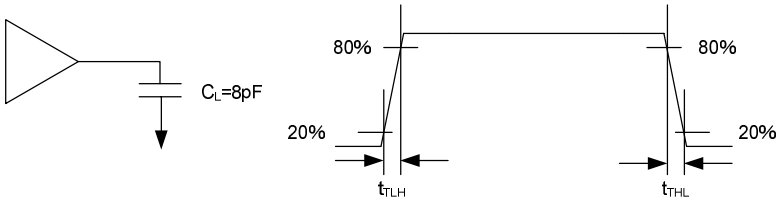


Figure 8. LVCMOS Output Load and Transition Time

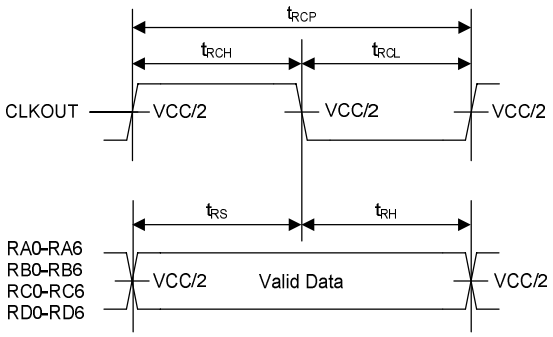


Figure 9. LVCMOS Output Setup and Hold Time

Input to Output Delay

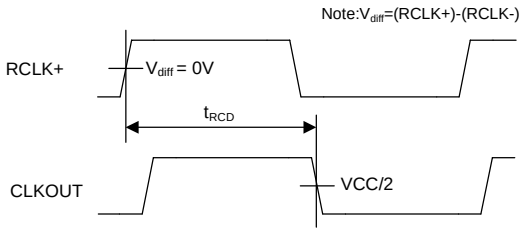


Figure 10.Input Clock to Output Clock Delay Time

Phase Lock Loop Set Time

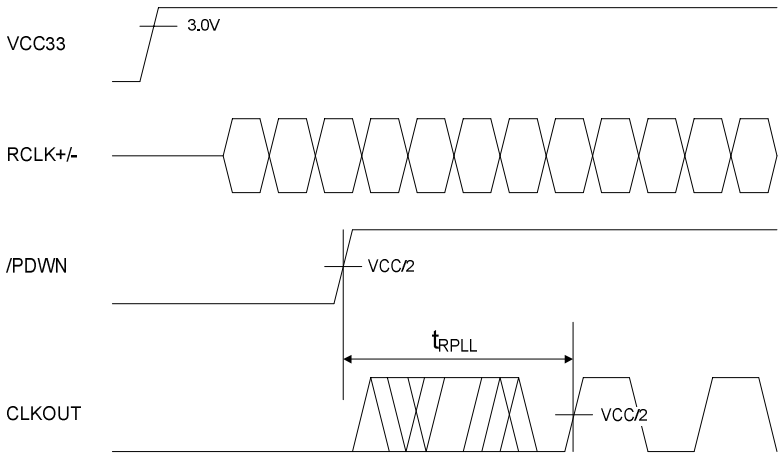


Figure 11. PLL Lock Loop Set Time

Application note

Display Data Mapping Example

Transmitter Pin	VESA format		JEIDA format		Receiver Pin
	6bit(18bpp)	8bit(24bpp)	6bit(18bpp)	8bit(24bpp)	
TA0	R0	R0	R2	R2	RA0
TA1	R1	R1	R3	R3	RA1
TA2	R2	R2	R4	R4	RA2
TA3	R3	R3	R5	R5	RA3
TA4	R4	R4	R6	R6	RA4
TA5	R5	R5	R7	R7	RA5
TA6	G0	G0	G2	G2	RA6
TB0	G1	G1	G3	G3	RB0
TB1	G2	G2	G4	G4	RB1
TB2	G3	G3	G5	G5	RB2
TB3	G4	G4	G6	G6	RB3
TB4	G5	G5	G7	G7	RB4
TB5	B0	B0	B2	B2	RB5
TB6	B1	B1	B3	B3	RB6
TC0	B2	B2	B4	B4	RC0
TC1	B3	B3	B5	B5	RC1
TC2	B4	B4	B6	B6	RC2
TC3	B5	B5	B7	B7	RC3
TC4	Hsync	Hsync	Hsync	Hsync	RC4
TC5	Vsync	Vsync	Vsync	Vsync	RC5
TC6	DE	DE	DE	DE	RC6
TD0	-	R6	-	R0	RD0
TD1	-	R7	-	R1	RD1
TD2	-	G6	-	G0	RD2
TD3	-	G7	-	G1	RD3
TD4	-	B6	-	B0	RD4
TD5	-	B7	-	B1	RD5
TD6	-	N/A	-	N/A	RD6

Note : Use TA to TC channels and open TD channel for 6bit application.

System Connection Example

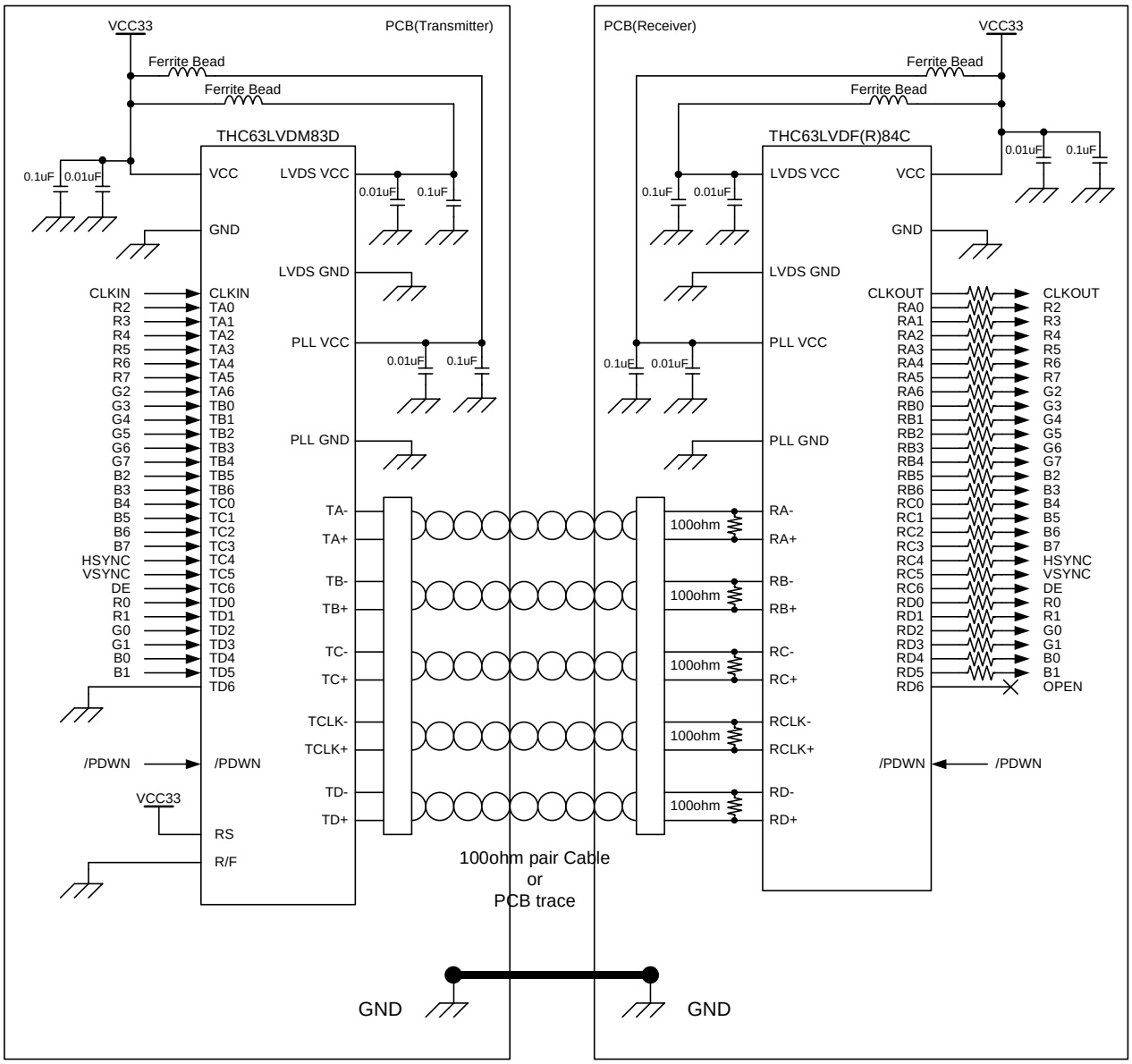


Figure 12. Connection Example with JEIDA Format

Notes

1) Cable Connection and Disconnection

Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which LVDS-Tx and THC63LVDF84C on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

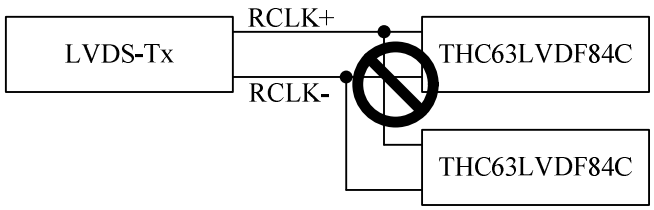


Figure 13. Multi Drop Connection

4) Asynchronous use

Asynchronous using such as following systems is not recommended.

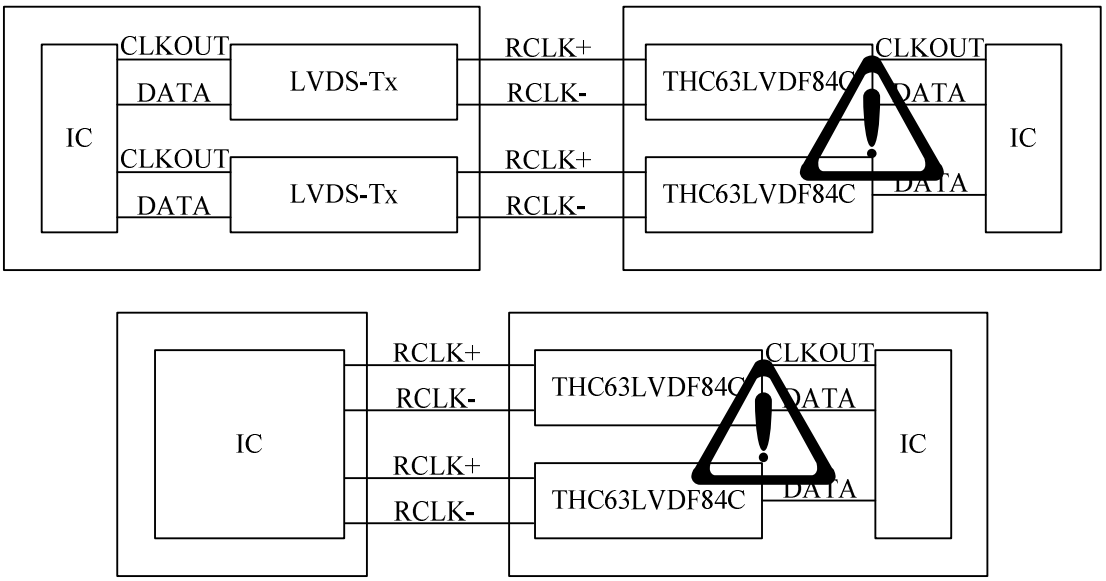
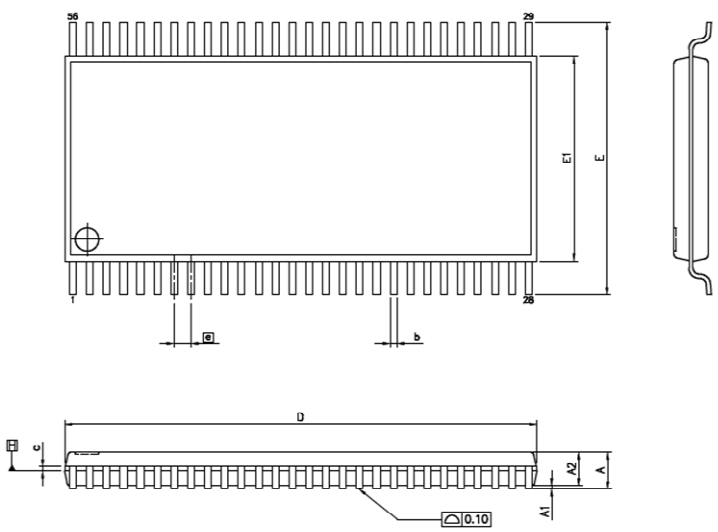


Figure 14. Asynchronous Use

Package



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.17	–	0.27
c	0.09	–	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10 BSC		
e	0.50 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1.JEDEC OUTLINE : MO-153 EE REV.F
2.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE H .

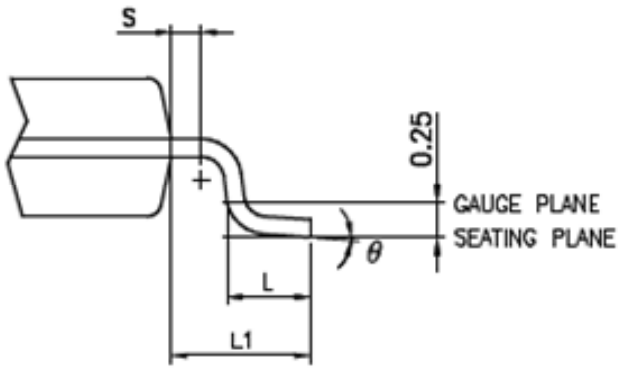
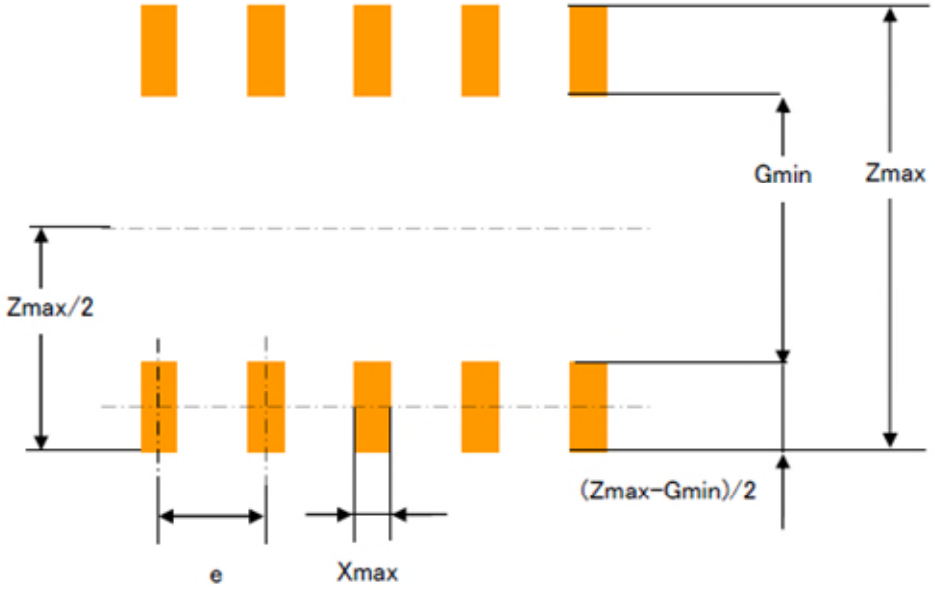


Figure 15. Package Diagram

Reference Land Pattern



Symbol	Calculation method	Units	Calculation Result		
			Level1	Level2	Level3
Zmax	Lmax+ 2JT	mm	9.40	9.00	8.60
Gmin	Smin -2JH	mm	5.40	5.70	6.00
Xmax	Wmax +2JS	mm	0.47	0.370	0.27
-	(Zamx-Gmin)/2	mm	2.00	1.65	1.30

* We calculate the value based on Reflow Soldering Method.
(Printed Manufacturing Tolerance and Mounted Tolerance = 0mm)

Figure 16. Reference of Land Pattern

The recommendation mounting method of THine device is reflow soldering.
The reference pattern is using the calculation result on condition of reflow soldering.

Notes
This land pattern design is a calculated value based on JEITA ET-7501.
Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc… The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

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