THC63LVD827-Z

LOW POWER / SMALL PACKAGE / 24Bit COLOR LVDS TRANSMITTER

General Description

The THC63LVD827-Z transmitter is designed to support pixel data transmission between Host and Flat Panel Display and Dual Link transmission between Host and Flat Panel Display up to 1080p/1920x1200 resolutions.

The THC63LVD827-Z converts 27bits (RGB 8 bits + Hsync, Vsync, DE) of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

For dual LVDS out, LVDS clock frequency of 87MHz, 51bits of RGB data are transmitted at an effective rate of 609Mbps per LVDS channel.

For single LVDS out, LVDS clock frequency of 174MHz, 27bits of RGB data are transmitted at an effective rate of 1218Mbps per LVDS channel.

21bits (RGB 6 bits + Hsync, Vsync, DE) mode is also selectable for 6bit color transmission with lower power.

Features

- Low power 1.8V CMOS design
- 7mm x 7mm/72pin/0.65mm pitch/TFBGA package applicable to non-HDI PCB.
- Wide dot clock range, 10-174MHz, suited for
  TV Signal: up to 1080p(74.25MHz dual)
  PC Signal: up to 1920x1200(77MHz dual)
- Supports 1.8V single power supply
- 1.8V/2.5V/3.3V TTL/CMOS inputs are supported by setting IOVCC=1.8V/2.5V/3.3V
- LVDS swing reducible by RS-pin to reduce both EMI and power consumption
- PLL requires No external components
- Flexible Input / Output mode
  1. Single in / Dual LVDS out
  2. Single in / Single LVDS out
  3. Double edge Single in / Dual LVDS out
- 2 LVDS data mapping to simplify PCB layout
- Power down mode
- Input clock triggering edge selectable by R/F pin
- 6bit / 8bit modes selectable by 6B/8B pin

Block Diagram

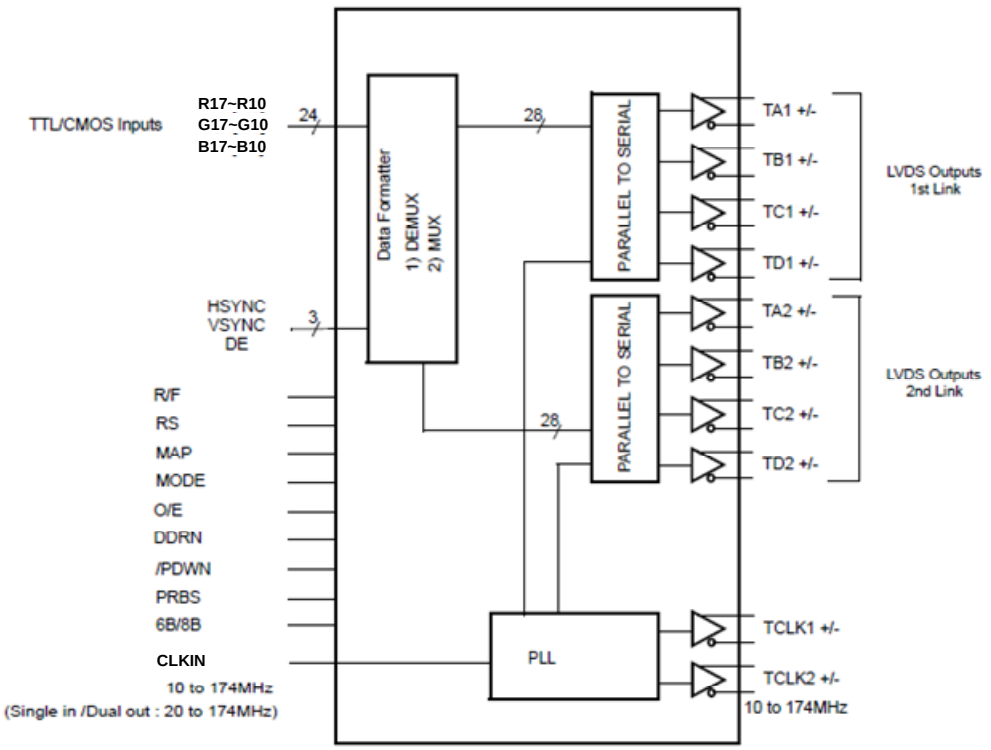


Figure 1. Block Diagram

Pin Diagram (top view)

TOP VIEW

	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	PRBS	N/C	Reserved1	GND	LVDS VCC	GND	PLL VCC	TD2-	TD2+	C
D	R11	R10	LVDS VCC				GND	/PDWN	O/E	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B/8B	RS	CLKIN	F
G	R17	R16	VCC	GND	VCC	GND	IOVCC	R/F	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	

Figure 2. Pin Diagram

Pin Description

Table 1. Pin Description

Pin Name	Pin #	Type	Description
TA1+,TA1-	A1,B1	LVDS OUT	**The 1st Link.** **The 1st pixel output data when Dual out.** **Output data when Single out.**
TB1+,TB1-	A2,B2		
TC1+,TC1-	A3,B3		
TD1+, TD1-	A5,B5		
TCLK1+, TCLK1-	A4,B4		**LVDS Clock Out for 1st Link.**
TA2+,TA2-	A6,B6		**The 2nd Link.** **The 2nd pixel output data when Dual out.**
TB2+,TB2-	A7,B7		
TC2+,TC2-	A8,B8		
TD2+, TD2-	C9,C8		
TCLK2+, TCLK2-	A9,B9		**LVDS Clock Out for 2nd Link.**
R17~R10	G1,G2,F1,F2 E1,E2,D1,D2	IN	**Pixel Data Inputs.**
G17~G10	J4,H4,J3,H3 J2,H2,J1,H1		
B17~B10	J8,H8,J7,H7 J6,H6,J5,H5		
DE	G9	IN	**Data Enable Input.**
VSYNC	H9	IN	**Vsync Input.**
HSYNC	J9	IN	**Hsync Input.**
CLKIN	F9	IN	**Clock Input.**
R/F	G8	IN	**Input Clock Triggering Edge Select.** H: Rising edge, L: Falling edge
RS	F8	IN	**LVDS swing mode select.** RS: H → LVDS Swing(V_{OD}, see Fig.7 and Fig.8) 350mV; L → 200mV
MAP	E8	IN	**LVDS mapping table select. See Fig.12 and Fig.13.** MAP: H → Mapping MODE1; L → Mapping MODE2
MODE	E7	IN	**Pixel data mode. See Fig.10 and Fig.11.** MODE: H → Single out (Single-in / Single-out); L → Dual out (Single-in / Dual-out)
O/E	D9	IN	**Output enable** H: Output enable. L: Output disable (all outputs are Hi-Z).
/PDWN	D8	IN	**Power Down enable** H: Normal operation. L: Power down (all outputs are Hi-Z and all circuits are stand-by mode with minimum current (I_{TCCS})).
PRBS (*a)	C1	IN	**Must be tied to GND.**

Pin Description (Continued)

Pin Name	Pin #	Type	Description
Reserved1	C3	IN	**Must be tied to GND.**
6B/8B	F7	IN	**6bit / 8bit mode select.** H: 6bit mode (21bit mode), L: 8bit mode (27bit mode).
DDRN	E9	IN	**DDR function is active when MODE=L (Dual-out mode)** H: DDR (Double Edge input) function disable (Fig.7). L: DDR (Double Edge input) function enable (Fig.8).
N/C	C2	-	**Must be Open.**
VCC	G3,G5	Power	**Power Supply Pins for digital circuitry.**
IOVCC	G7		**Power Supply Pins for IO inputs circuitry.**
LVDSVCC	C5,D3		**Power Supply Pins for LVDS Outputs.**
PLLVCC	C7		**Power Supply Pins for PLL circuitry.**
GND	F3,G4,G6,C4, E3,C6,D7	Ground	**Ground Pins.**

(*a) : Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2^{23}-1.
The generated PRBS is fed into input data latches, encoded and serialized into LVDS OUT.
This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

Absolute Maximum Ratings

Table 2. Absolute Maximum Rating

Parameter	Min	Max	Unit
Power Supply Voltage (IOVCC)	-0.3	+4.0	V
Power Supply Voltage (VCC,PLLVCC,LVDSVCC)	-0.3	+2.1	V
CMOS/TTL Input Voltage	-0.3	IOVCC+0.3	V
LVDS Transmitter Output Voltage	-0.3	LVDSVCC+0.3	V
Output Current	-50	+50	mA
Junction Temperature	-	+125	°C
Storage Temperature Range	-55	+125	°C
Reflow Peak Temperature / Time	-	+260 / 10sec	°C
Maximum Power Dissipation @+25°C	-	1.3	W

Recommended Operating Conditions

Table 3. Operating Condition

Symbol	Parameter				Min	Typ	Max	Unit
Ta	Operating Ambient Temperature				-40	25	+105	°C
IOVCC	Power Supply Voltage				1.62	1.8 2.5 3.3	3.6	V
PLLVCC **LVDSVCC** **VCC**	Power Supply Voltage				1.62	1.8	1.98	V
F_{clk}	Clock Frequency	MODE = L Dual - out	Single Edge Input (DDRN=H)	Input	20	-	174	MHz
				LVDS Output	10	-	87	
			Double Edge Input (DDRN=L)	Input	10	-	174	
				LVDS Output	10	-	174	
		MODE=H Single - out		Input	10	-	174	
				LVDS Output	10	-	174	

Electrical Characteristics

CMOS/TTL (Pin type "IN") DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Table 4. CMOS/TTL DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH18}	High Level Data Input Voltage	IOVCC=1.62V~1.98V	0.65*IOVCC	-	IOVCC	V
V_{IL18}	Low Level Data Input Voltage		GND	-	0.35*IOVCC	V
V_{IH25}	High Level Data Input Voltage	IOVCC=2.3V~2.7V	1.7	-	IOVCC	V
V_{IL25}	Low Level Data Input Voltage		GND	-	0.7	V
V_{IH33}	High Level Data Input Voltage	IOVCC=3.0V~3.6V	2.0	-	IOVCC	V
V_{IL33}	Low Level Data Input Voltage		GND	-	0.8	V
I_{INC}	Input Current	VIN=GND~IOVCC	-10	-	+10	μA

LVDS Transmitter (Pin type "LVDS OUT") DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

Table 5. LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OD}	Differential Output Voltage	R_L = 100Ω	Normal swing RS=H	250	350	450	mV
			Reduced swing RS=L	140	200	300	
ΔV_{OD}	Change in V_{OD} between complementary output states	R_L = 100Ω		-	-	35	
V_{OC}	Common Mode Voltage			1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between complementary output states			-	-	35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, R_L = 100Ω		-	-	100	mA
I_{OZ}	Output TRI-State Current	/PDWN=L, V_{OUT} = GND ~ LVDSVCC		-20	-	+20	μA

Electrical Characteristics (Continued)

Power Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

Table 6. Power Supply Current

Symbol	Parameter	Conditions			Typ(a)	Max(b)	Unit
I_{TCCW}	Operating Current	R_L=100Ω CL=5pF RS=H (RS=L)	MODE = H Single - out	CLKIN=37MHz	24 (18)	33 (26)	mA
				CLKIN=65MHz	29 (23)	43 (37)	
				CLKIN=72MHz	30 (24)	46 (40)	
			MODE = L Dual - out DDRN = H DDR Input Off	CLKIN=89MHz	48 (36)	65 (53)	
				CLKIN=119MHz	53 (41)	75 (63)	
				CLKIN=139MHz	56 (44)	82 (70)	
				CLKIN=154MHz	58 (46)	88 (76)	
			MODE = L Dual - out DDRN = L DDR Input On	CLKIN=44.5MHz	47 (35)	64 (52)	
				CLKIN=59.5MHz	51 (39)	74 (62)	
				CLKIN=69MHz	54 (42)	80 (68)	
				CLKIN=77MHz	56 (44)	85 (73)	
I_{TCCS}	Power Down Current	/PDWN = L, All Inputs = Fixed L or H			1	140	μA

(a) All Typ. values are at VCC=1.8V, Ta=25°C . The 256 Grayscale Test Pattern inputs test for a typical display pattern.
(b) All Max. values are at VCC=1.98V, Ta=105°C . Worst Case Test Pattern produces maximum switching frequency for all the LVDS outputs (Fig.3).

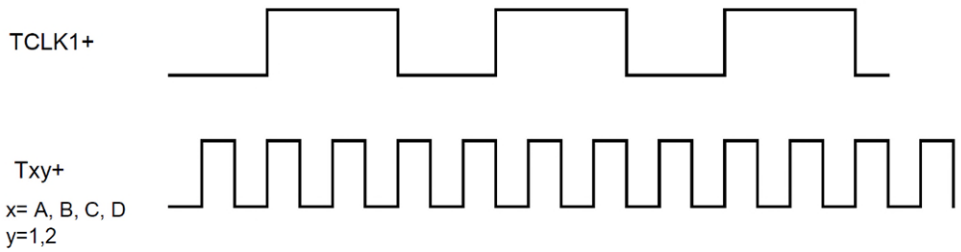


Figure 3. Test Pattern (LVDS Output Full Toggle Pattern)

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Table 7. Switching Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
t_{TCIP}	CLKIN Period (Fig.7,8)		5.75	-	100	ns
t_{TCH}	CLKIN High Time (Fig.7,8)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLKIN Low Time (Fig.7,8)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN (Fig.7,8)		0.8	-	-	ns
t_{TH}	TTL Data Hold to CLK IN (Fig.7,8)		0.8	-	-	ns
t_{TCD}	CLKIN to TCLK+/- Delay (Fig7,8)	MODE=L,DDRN=H	$9t_{TCIP}$ +3.1	-	$9t_{TCIP}$ +8.0	ns
		Others	$5t_{TCIP}$ +3.1	-	$5t_{TCIP}$ +8.0	ns
t_{TCOP}	TCLK1,2 Period (Fig.6)		5.75	-	100	ns
t_{LVT}	LVDS Transition Time (Fig.4)		-	0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig.9)	t_{TCOP} =5.75ns~15ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig.9)		$\frac{t_{TCOP}}{7}$ -0.15	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TOP6}	Output Data Position2 (Fig.9)		$2\frac{t_{TCOP}}{7}$-0.15	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TOP5}	Output Data Position3 (Fig.9)		$3\frac{t_{TCOP}}{7}$ -0.15	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TOP4}	Output Data Position4 (Fig.9)		$4\frac{t_{TCOP}}{7}$ -0.15	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TOP3}	Output Data Position5 (Fig.9)		$5\frac{t_{TCOP}}{7}$ -0.15	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TOP2}	Output Data Position6 (Fig.9)		$6\frac{t_{TCOP}}{7}$ -0.15	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7}$ +0.15	ns
t_{TPLL}	Phase Lock Time (Fig.5)		-	-	10.0	ms
t_{DEINT}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		$4t_{TCIP}$	t_{TCIP} *(2n)[a]	-	ns
t_{DEH}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		$2t_{TCIP}$	t_{TCIP} *(2m)[a]	-	ns
t_{DEL}	DE Input Period (Fig.6) Dual out mode only(MODE=L)		$2t_{TCIP}$	-	-	ns

(a) Refer to Fig.6 for details.

AC Timing Diagrams

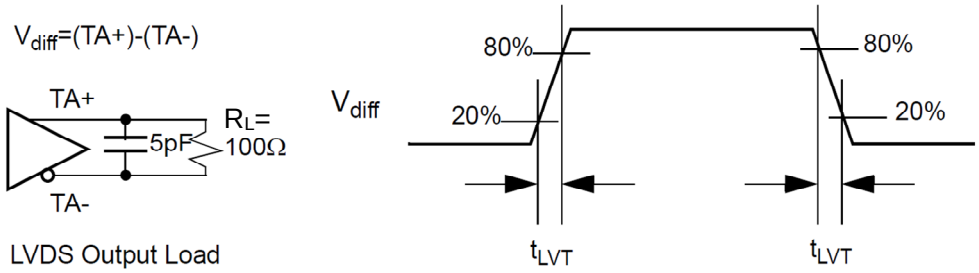


Figure 4. LVDS Output Load and Transition Time

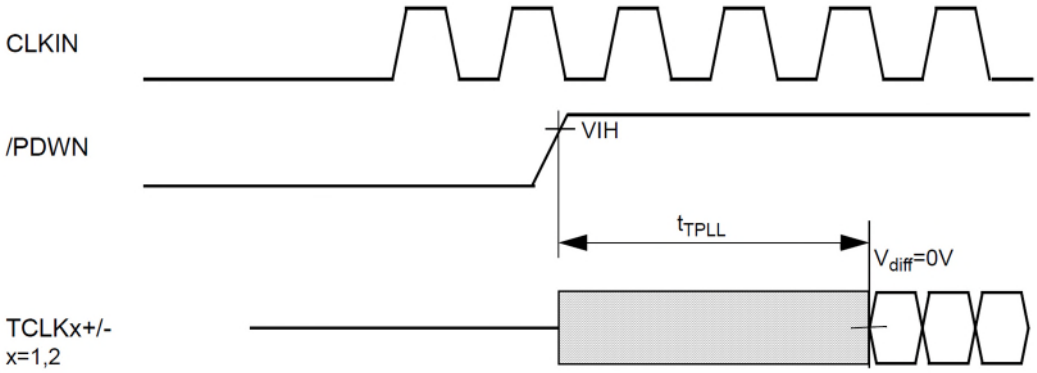
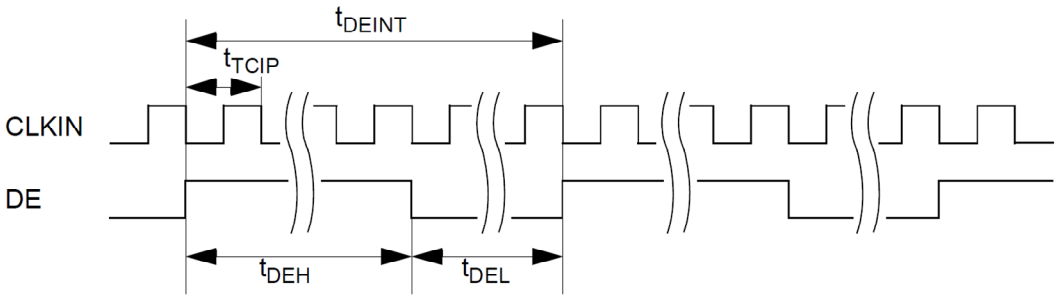


Figure 5. PLL Lock Time



Note: **Dual-out mode(MODE=L)**

The period between rising edges of DE (t_{DEINT}), high time of DE (t_{DEH}) should always satisfy following equations.

$$t_{DEH} = t_{TCIP} * (2m)$$

$$t_{DEINT} = t_{TCIP} * (2n)$$

m, n = integer

Figure 6. Dual-out mode DE input timing

AC Timing Diagrams(Continued)

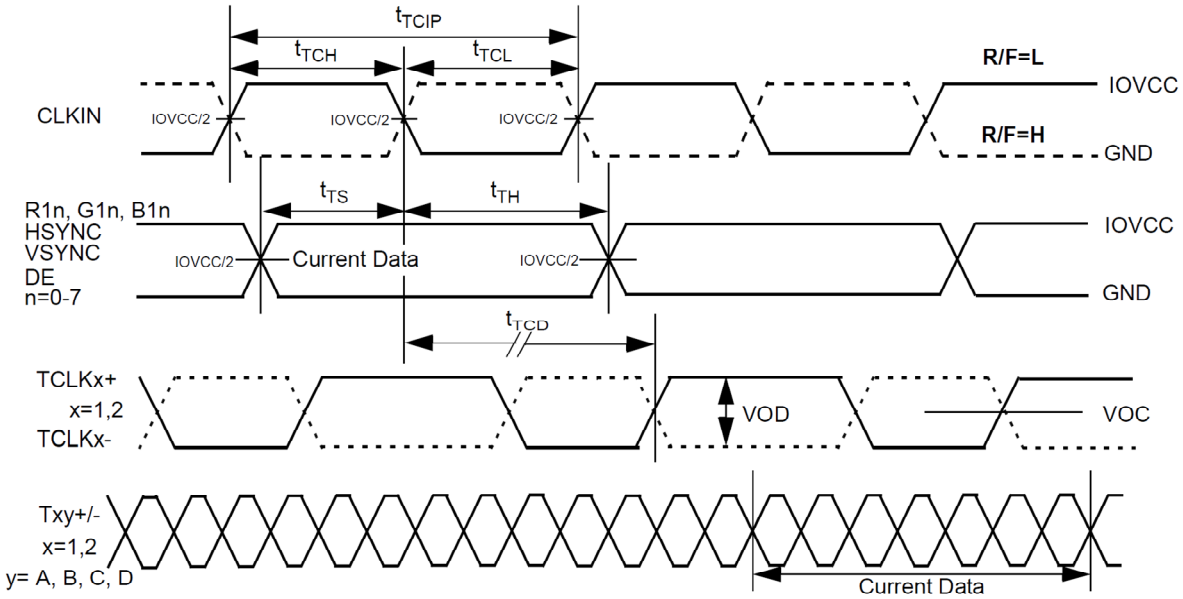


Figure 7. CLKIN Period, High/Low Time, Setup/Hold Timing for Single Edge Input Mode

MODE = H or DDRN = H

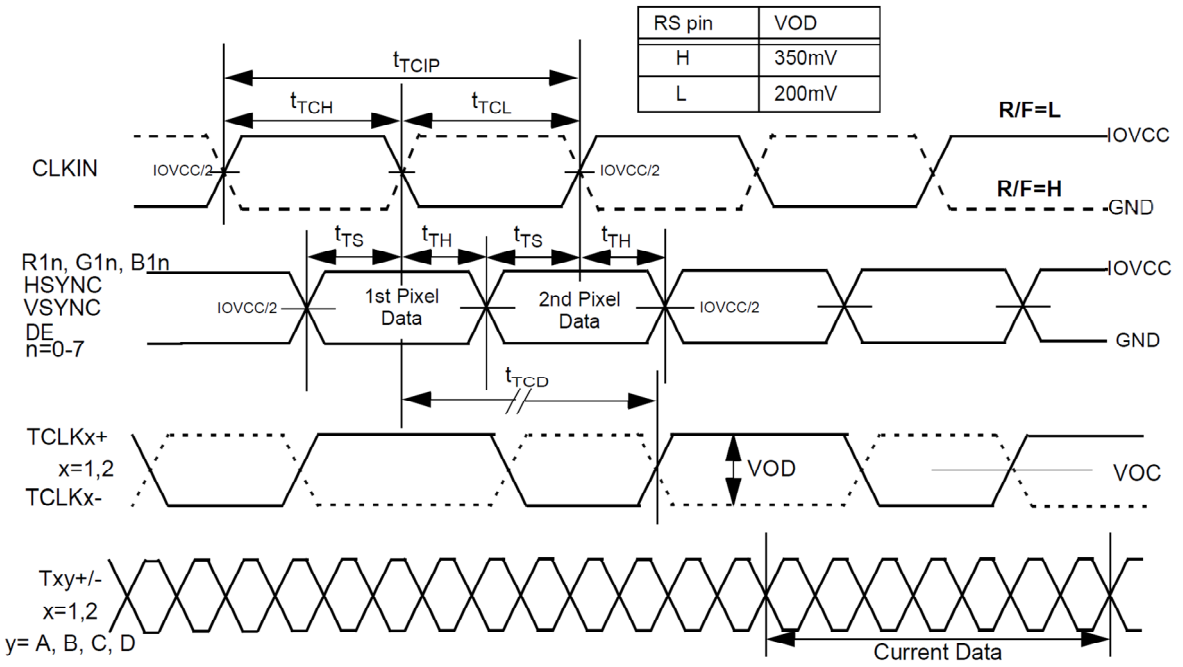


Figure 8. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode(DDR)

MODE = L, DDRN = L

AC Timing Diagrams(Continued)

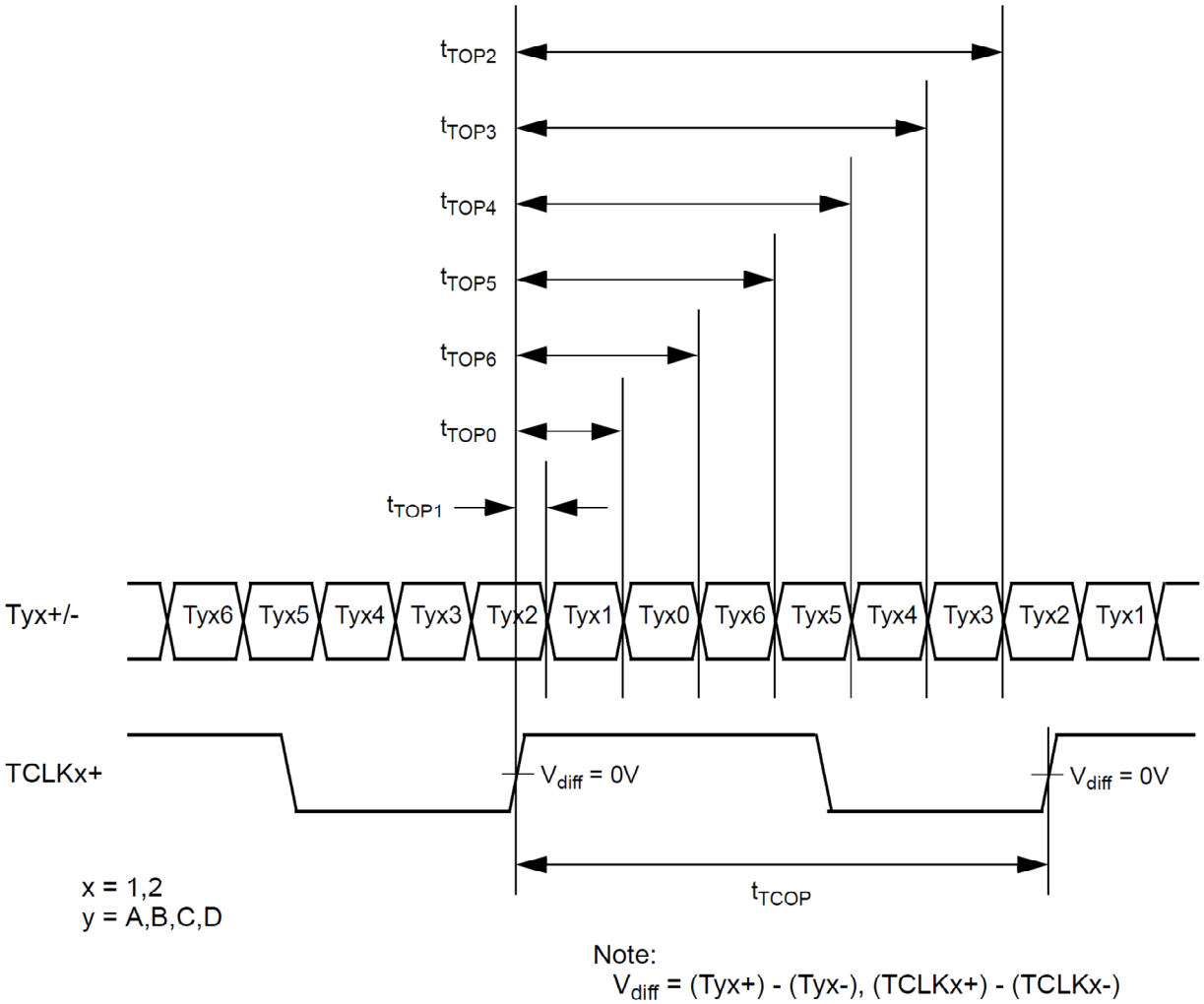


Figure 9. LVDS Output Data Position

Single-In / Dual-Out Mode (MODE = L)

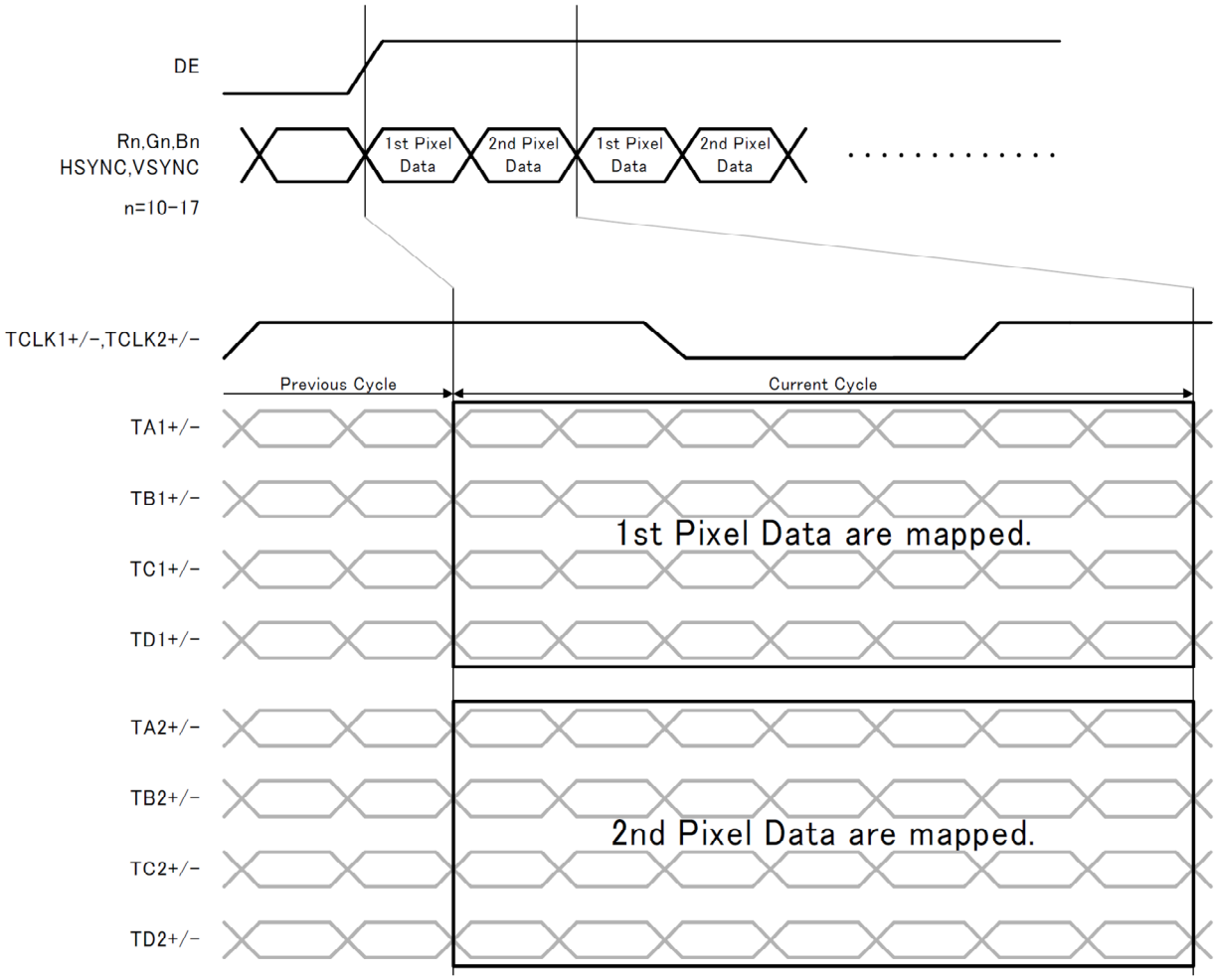


Figure 10. Single-In / Dual-Out Mode (MODE = L)

Single-In / Single-Out Mode (MODE = H)

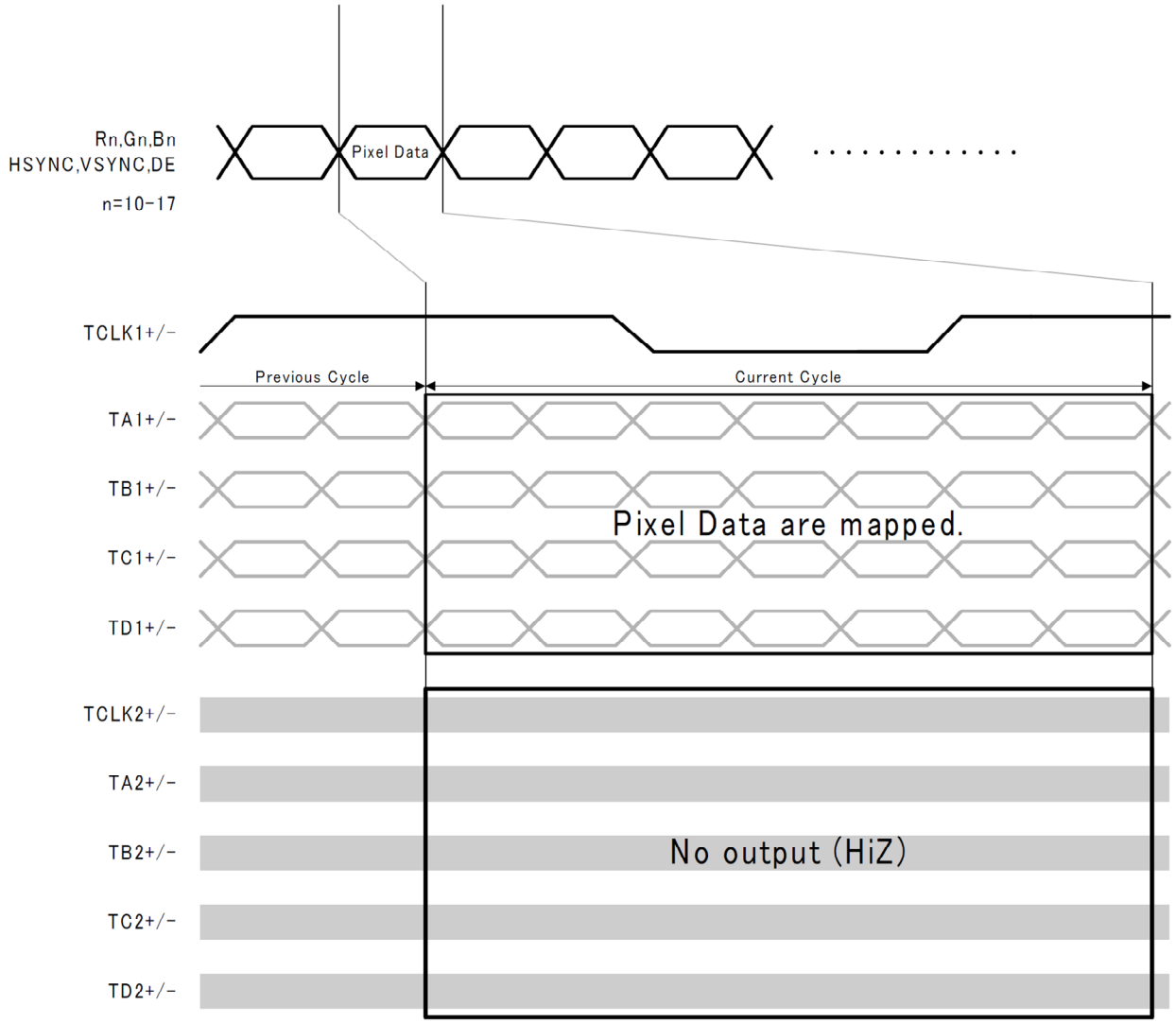
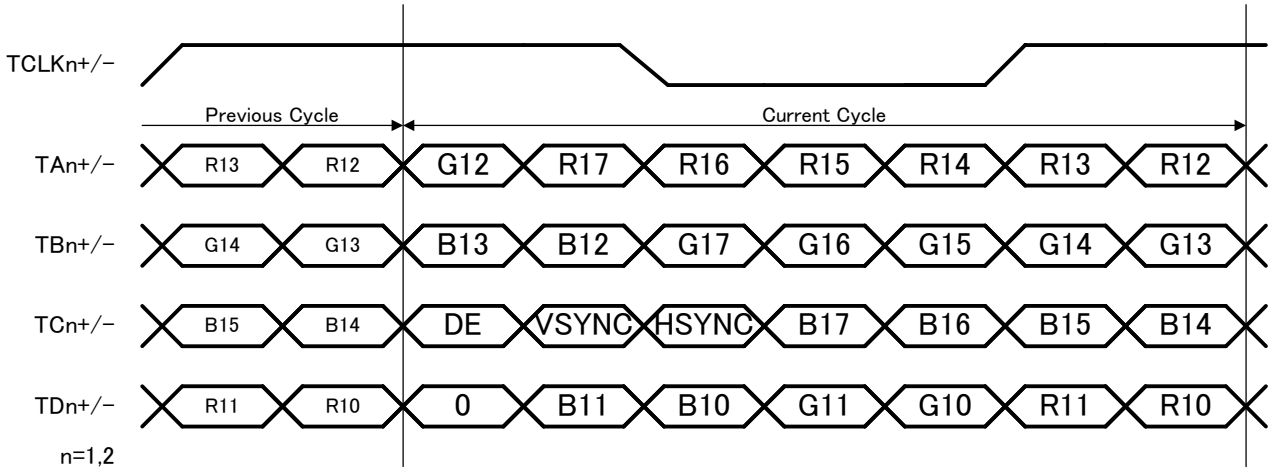
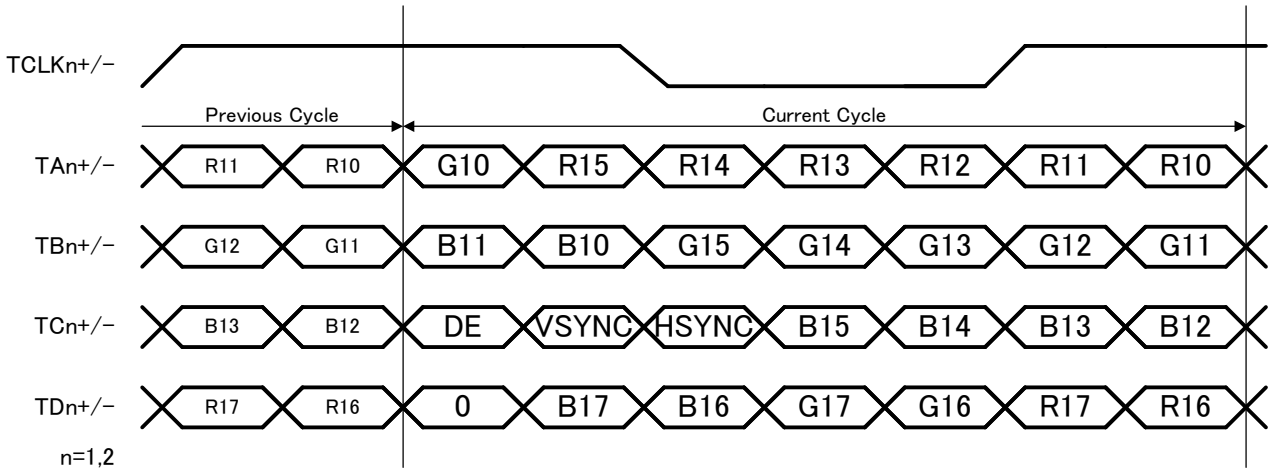


Figure 11. Single-In / Single-Out Mode (MODE = H)

LVDS Data Mapping for 8 bit Mode (6B/8B = L)



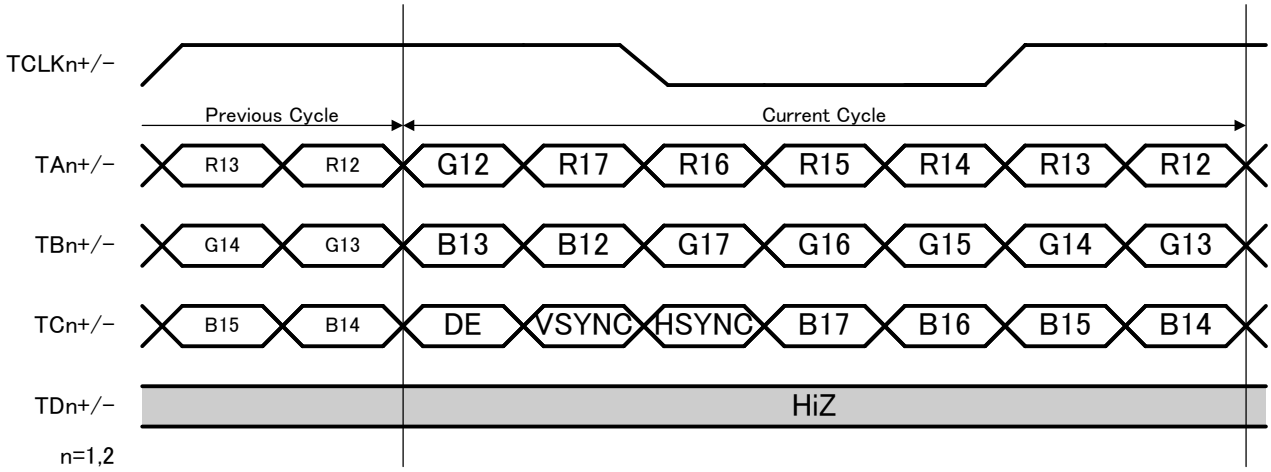
(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



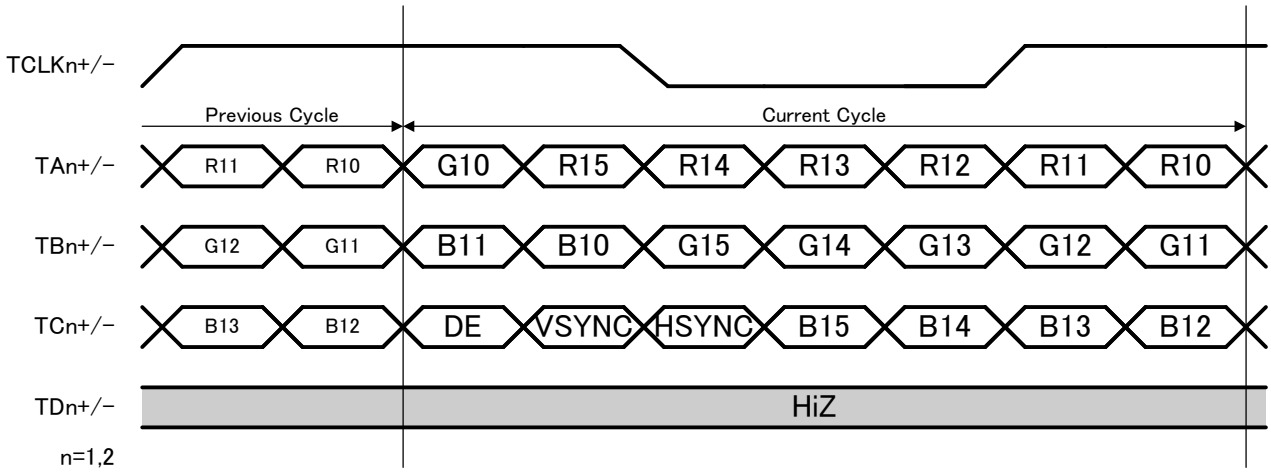
(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Figure 12. LVDS Data Mapping for 8 bit Mode (6B/8B = L)

LVDS Data Mapping for 6 bit Mode (6B/8B = H)



(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Figure 13. LVDS Data Mapping for 6 bit Mode (6B/8B = H)

Note: Input pins which are not used in 6 bit Mode (R10-11,G10-11,B10-11 on Mapping Mode 1, R16-17,G16-17,B16-17 on Mapping Mode 2) can be H, L, or Open.

Note

1) Cable Connection and Disconnection
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection
Connect the each GND of the PCB which THC63LVD827-Z and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection
Multi drop connection is not recommended.

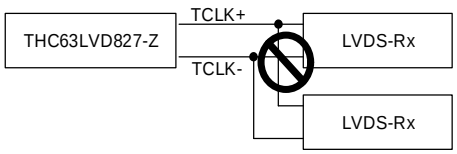


Figure 14. Multi Drop Connection

4) Asynchronous Use
Asynchronous use such as following systems are not recommended.

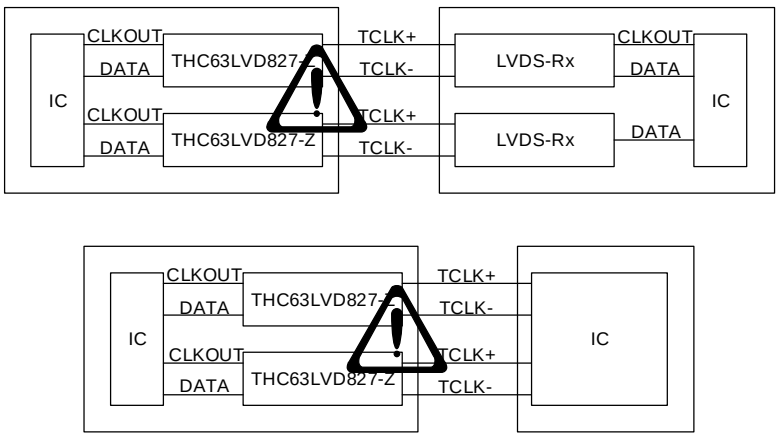


Figure 15. Asynchronous Use

Package

TFBGA

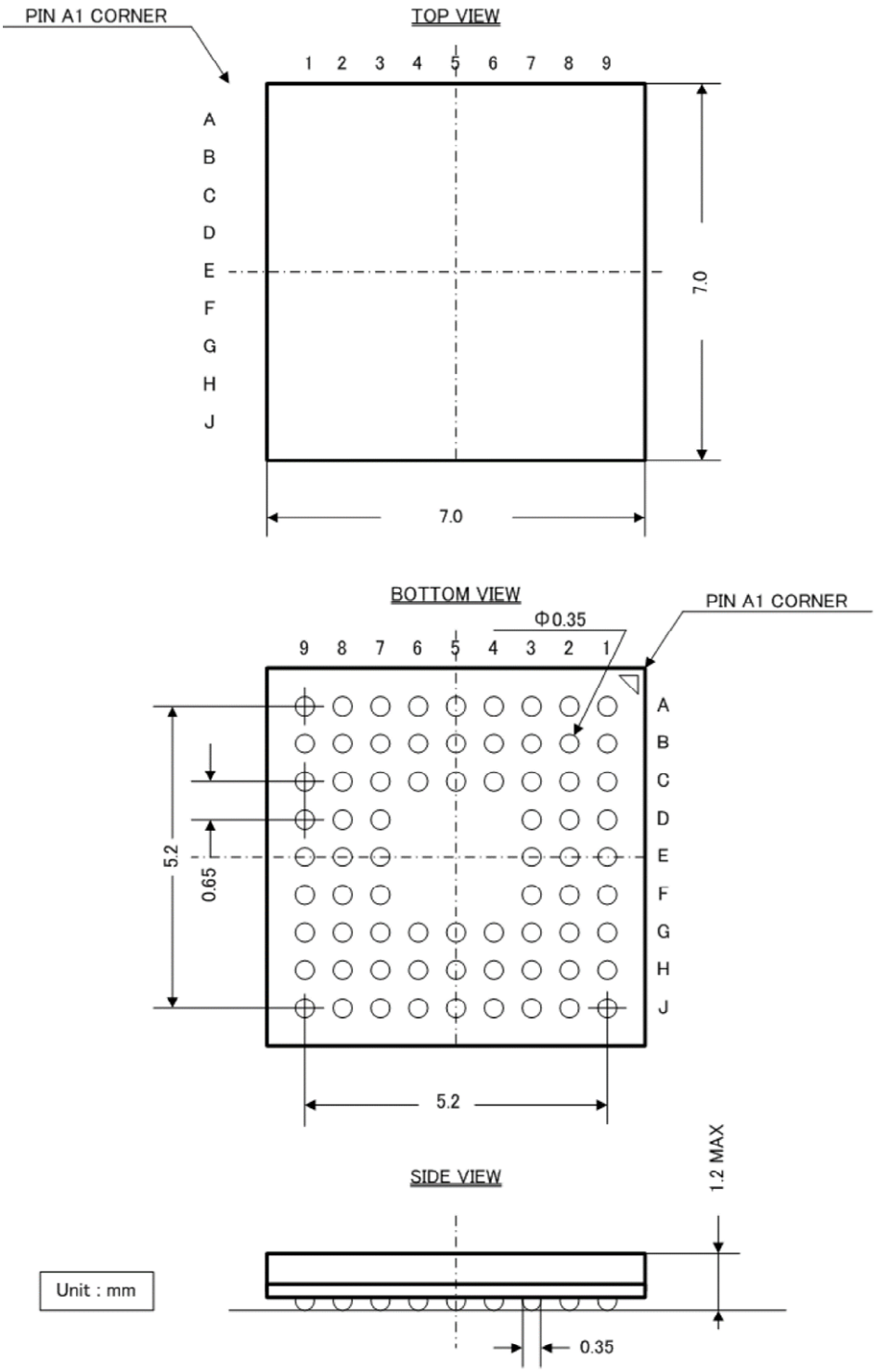


Figure 16. Package Diagram

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

3. This material contains THine's copyright, know-how or other intellectual property rights. Copying, reverse-engineer or disclosing to third parties the contents of this material without THine's prior written permission is prohibited.

4. THINE ACCEPTS NO LIABILITY FOR ANY DAMAGE OR LOSS IN CONNECTION WITH ANY DISPUTE RELATING TO INTELLECTUAL PROPERTY RIGHTS BETWEEN THE USER AND ANY THIRD PARTY, ARISING OUT OF THIS PRODUCT, EXCEPT FOR SUCH DAMAGE OR LOSS IN CONNECTION WITH DISPUTES SUCCESSFULLY PROVED BY THE USER THAT SUCH DISPUTES ARE DUE SOLELY TO THINE. NOTE, HOWEVER, EVEN IN THE AFOREMENTIONED CASE, THINE ACCEPTS NO LIABILITY FOR SUCH DAMAGE OR LOSS IF THE DISPUTE IS CAUSED BY THE USER'S INSTRUCTION.

5. This product is not designed for applications that require extremely high-reliability/safety such as aerospace device, nuclear power control device, or medical device related to critical care, excluding when this product is specified for automotive use by THine and used it for that purpose. THine accepts no liability whatsoever for any damages, claims or losses arising out of the uses set forth above.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently fail-safe design principles such as redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

10. This product must be stored according to storage method which is specified in this specifications. THine accepts no liability whatsoever for any damage or loss caused to the user due to any storage not according to above-mentioned method.

11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

13. All patents or pending patent applications, trademarks, copyrights, layout-design exploitation rights or other intellectual property rights concerned with this product belong to THine or licensor(s) of THine. No license or right is granted to the user for any intellectual property right or other proprietary right now or in the future owned by THine or THine's licensor. The user must enter into a license agreement with THine or THine's licensor to be granted of such license or right.

THine Electronics, Inc.

https://www.thine.co.jp