

# THC63LVDM83D

## 24bit COLOR LVDS TRANSMITTER

### General Description

The THC63LVDM83D transmitter is designed to support pixel data transmission between Host and Flat Panel Display up to 1080p/WUXGA resolutions.

The THC63LVDM83D converts 28bits of LVCMOS data into four OpenLDI(LVDS) data streams. The transmitter can be programmed for rising edge or falling edge clock through a dedicated pin. At a transmit clock frequency of 160MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, CONT1) are transmitted at an effective rate of 1120Mbps per OpenLDI(LVDS) channel.

### Application

- Medium and Small Size Panel
- Tablet PC / Notebook PC
- Security Camera / Industrial Camera
- Multi Function Printer
- Industrial Equipment
- Medical Equipment Monitor

### Features

- Compatible with TIA/EIA-644 LVDS Standard
- 7:1 OpenLDI(LVDS) Transmitter
- Operating Temperature Range : 0 to +70°C
- No Special Start-up Sequence Required
- Spread Spectrum Clocking Tolerant up to 100kHz Frequency Modulation and +/-2.5% Deviations.
- Wide Dot Clock Range: 8 to 160MHz Suited for  
TV Signal : NTSC(12.27MHz) - 1080p(148.5MHz)  
PC Signal : QVGA(8MHz) - WUXGA(154MHz)
- 56pin TSSOP Package
- 1.2V to 3.3V LVCMOS/ inputs are supported.
- LVDS swing is reducible as 200mV by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- Power Down Mode.
- Input clock triggering edge is selectable by R/F-pin
- EU RoHS Compliant.

### Block Diagram

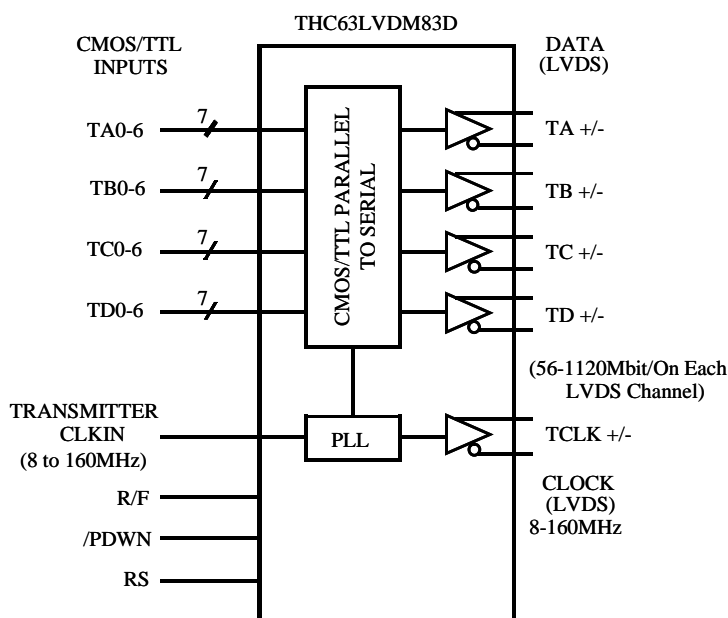
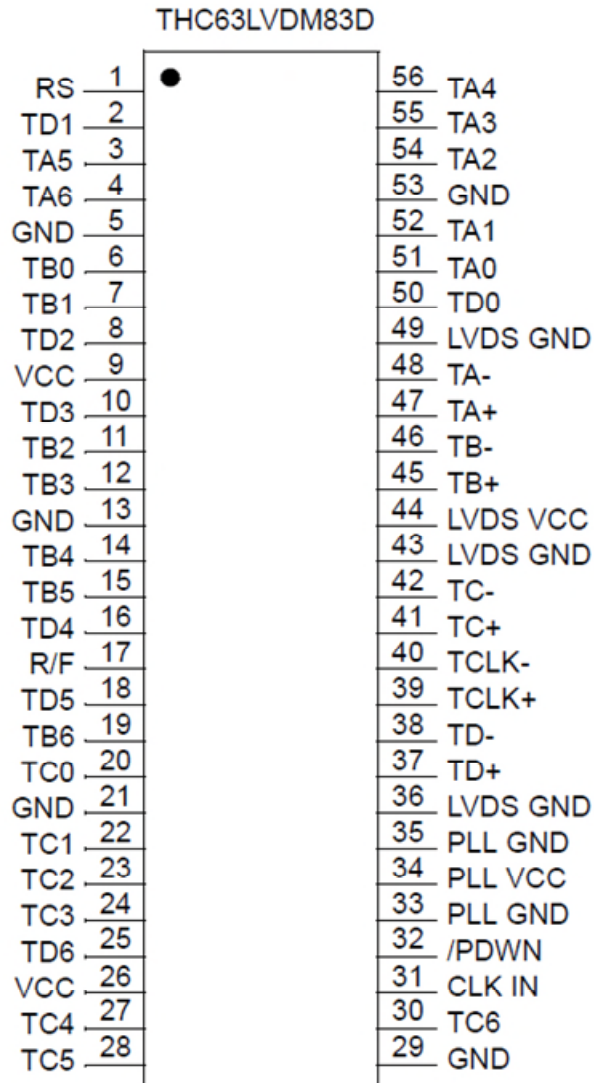


Figure 1. Block Diagram

Pin Diagram



**Figure 2. Pin Diagram**

Pin Description

Pin Name	Pin #	Direction	Type	Description										
TA+, TA-	47, 48	Output	LVDS	LVDS Data Out										
TB+, TB-	45, 46													
TC+, TC-	41, 42													
TD+, TD-	37, 38													
TCLK+, TCLK-	39, 40			LVDS Clock Out										
TA0 ~ TA6	51, 52, 54, 55, 56, 3, 4	Input	LVCMOS	Pixel Data Input										
TB0 ~ TB6	6, 7, 11, 12, 14, 15, 19													
TC0 ~ TC6	20, 22, 23, 24, 27, 28, 30													
TD0 ~ TD6	50, 2, 8, 10, 16, 18, 25													
/PDWN	32			H : Normal Operation L : Power Down (All outputs are Hi-Z)										
RS	1			LVDS Swing Mode, VREF Select See Fig.7, 8										
		<table border="1"> <thead> <tr> <th>RS Pin</th> <th>LVDS Swing</th> <th>Small Swing Input Support</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>350mV</td> <td>N/A</td> </tr> <tr> <td>0.6 to 1.4V</td> <td>350mV</td> <td>RS=VREF</td> </tr> <tr> <td>GND</td> <td>200mV</td> <td>N.A</td> </tr> </tbody> </table>	RS Pin	LVDS Swing	Small Swing Input Support	VCC	350mV	N/A	0.6 to 1.4V	350mV	RS=VREF	GND	200mV	N.A
RS Pin	LVDS Swing	Small Swing Input Support												
VCC	350mV	N/A												
0.6 to 1.4V	350mV	RS=VREF												
GND	200mV	N.A												
R/F	17	VREF : is Input Reference Voltage												
CLKIN	31	Input Clock Triggering Edge Select H : Rising Edge L : Falling Edge												
VCC	9, 26	Power Supply Pins for LVCMOS inputs and digital circuit.												
GND	5, 13, 21, 29, 53	Ground Pins for LVCMOS Inputs and Digital Circuitry.												
LVDS VCC	44	Power Supply Pins for LVDS Outputs.												
LVDS GND	36, 43 49	Ground Pins for LVDS Outputs.												
PLL VCC	34	Power Supply Pin for PLL Circuitry.												
PLL GND	33, 35	Ground Supply Pin for PLL Circuitry.												

**Table 1. Pin Description**

**Absolute Maximum Ratings**

Parameter	Min	Max	Unit
All Supply Voltage (VCC, LVDS VCC, PLL VCC)	-0.3	+4.0	V
LVC MOS Input Voltage	-0.3	VCC + 0.3	V
LVDS Output Pin	-0.3	VCC + 0.3	V
Output Current	-30	30	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+150	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.8	W

**Table 2. Absolute Maximum Ratings**

**Recommended Operating Conditions**

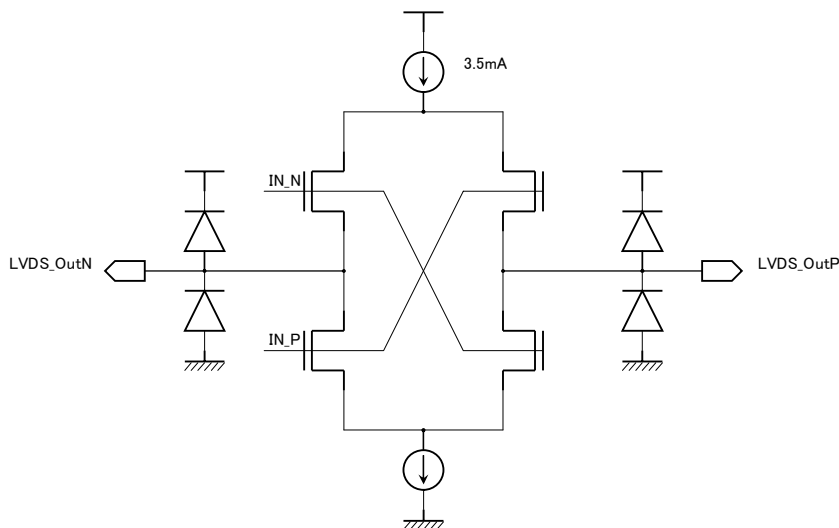
Symbol	Parameter	Min	Typ	Max	Unit
VCC, LVDS VCC PLL VCC	All Supply Voltage	3.0	3.3	3.6	V
Ta	Operating Ambient Temperature	0	25	+70	°C
-	Clock Frequency	8	-	160	MHz

**Table 3. Recommended Operating Conditions**

“Absolute Maximum Ratings” are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics Table4, 5, 6, 7” specify conditions for device operation.

“Absolute Maximum Rating” value also includes behavior of overshooting and undershooting.

**Equivalent LVDS Output Schematic Diagram**



**Figure 3. LVDS Output Schematic Diagram**

**Power Consumption**

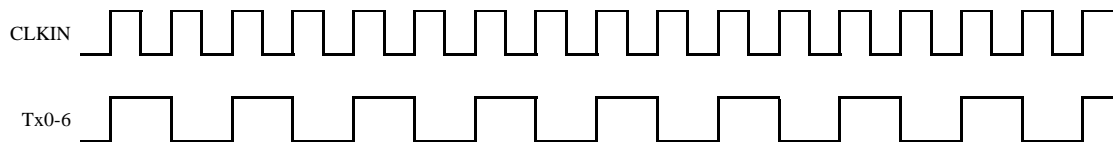
Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Typ*	Max	Unit
I <sub>TCCW</sub>	LVDS Transmitter Operating Current Worst Case Pattern (Fig.4)	RL=100Ω, CL=5pF, f=85MHz, RS=VCC	61	67	mA
		RL=100Ω, CL=5pF, f=135MHz, RS=VCC	77	83	mA
		RL=100Ω, CL=5pF, f=160MHz, RS=VCC	84	92	mA
		RL=100Ω, CL=5pF, f=85MHz, RS=GND	50	56	mA
		RL=100Ω, CL=5pF, f=135MHz, RS=GND	65	71	mA
		RL=100Ω, CL=5pF, f=160MHz, RS=GND	73	80	mA
I <sub>TCCS</sub>	LVDS Transmitter Power Down Current	/PDWN=L, All Inputs=L or H	-	10	μA

\*Typ values are at the conditions of VCC=3.3V and Ta = +25°C

**Table 4. Power Consumption**

**Worst Case Pattern**



x=A,B,C,D

**Figure 4. Worst Case Pattern**

**Electrical Characteristics**

**LVC MOS DC Specifications**

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V <sub>IH</sub>	High Level Input Voltage	RS=VCC or GND	2.0	-	VCC	V
V <sub>IL</sub>	Low Level Input Voltage	RS=VCC or GND	GND	-	0.8	V
V <sub>DDQ</sub> <sup>1</sup>	Small Swing Voltage		1.2	-	2.8	V
V <sub>REF</sub>	Input Reference Voltage	Small Swing (RS=V <sub>DDQ</sub> /2)	-	V <sub>DDQ</sub> /2	-	
V <sub>SH</sub> <sup>2</sup>	Small Swing High Level Input Voltage	V <sub>REF</sub> = V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 +100mV	-	-	V
V <sub>SL</sub> <sup>2</sup>	Small Swing Low Level Input Voltage	V <sub>REF</sub> = V <sub>DDQ</sub> /2	-	-	V <sub>DDQ</sub> /2 -100mV	V
I <sub>INC</sub>	Input Current	GND ≤ V <sub>IN</sub> ≤ VCC	-	-	±10	μA

\*Typ values are at the conditions of VCC=3.3V and Ta= +25°C

Notes : <sup>1</sup> V<sub>DDQ</sub> voltage defines the max voltage of small swing inputs at RS=VREF. It is not an actual input voltage.

<sup>2</sup> Small swing signals are applied to TA0-6, TB0-6, TC0-6, TD0-6 and CLKIN.

**Table 5. LV-CMOS DC Specifications**

**LVDS Transmitter DC Specifications**

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
VOD	Differential Output Voltage	RL=100Ω Normal swing RS=VCC	250	350	450	mV
		RL=100Ω Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω	-	-	35	mV
VOC	Common Mode Voltage		1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states		-	-	35	mV
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT</sub> =GND, RL=100Ω	-	-	-24	mA
I <sub>OZ</sub>	Output TRI-STATE Current	/PDWN=GND, V <sub>OUT</sub> =GND to VCC	-	-	±10	μA

\*Typ values are at the conditions of VCC=3.3V and Ta= +25°C

**Table 6. LVDS Transmitter DC Specifications**

### LVC MOS & LVDS Transmitter AC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
$t_{TCIT}$	CLK IN Transition Time	-	-	5.0	ns
$t_{TCP}$	CLK IN Period	6.25	T	125	ns
$t_{TCH}$	CLK IN High Time	0.35T	0.5T	0.65T	ns
$t_{TCL}$	CLK IN Low Time	0.35T	0.5T	0.65T	ns
$t_{TCD}$	CLK IN to TCLK+/- Delay	-	3T	-	ns
$t_{TS}$	LVC MOS Data Setup to CLK IN	2.0	-	-	ns
$t_{TH}$	LVC MOS Data Hold from CLK IN	0.0	-	-	ns
$t_{LVT}$	LVDS Transition Time	-	0.6	1.5	ns
$t_{TOP1}$	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
$t_{TOP0}$	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
$t_{TOP6}$	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
$t_{TOP5}$	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
$t_{TOP4}$	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
$t_{TOP3}$	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
$t_{TOP2}$	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns
$t_{TPLL}$	Phase Lock Loop Set	-	-	10.0	ms

\*Typ values are at the conditions of VCC=3.3V and Ta = +25°C

Table 7. LVC MOS & LVDS Transmitter AC Specifications

#### LVC MOS Input

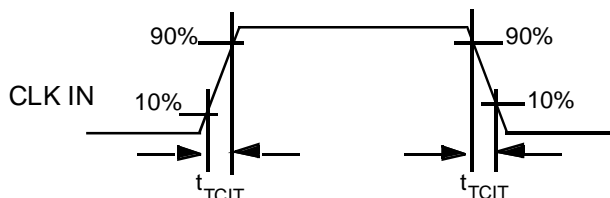
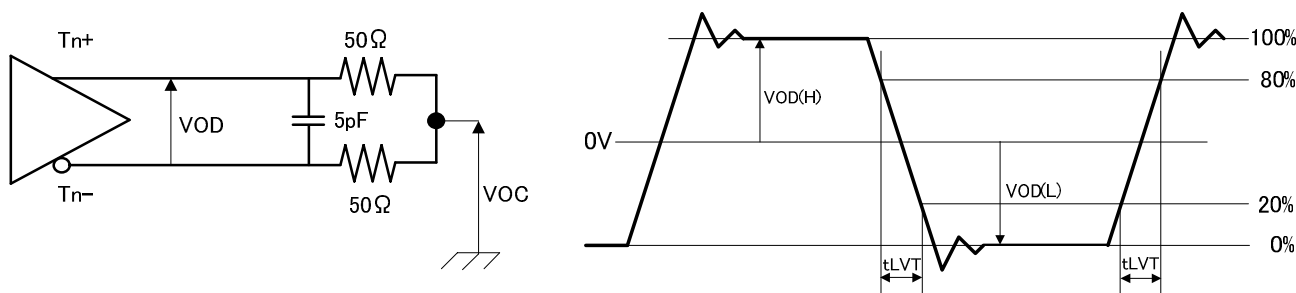


Figure 5. CLKIN Transmission Time

#### LVDS Output



#### LVDS Output Load

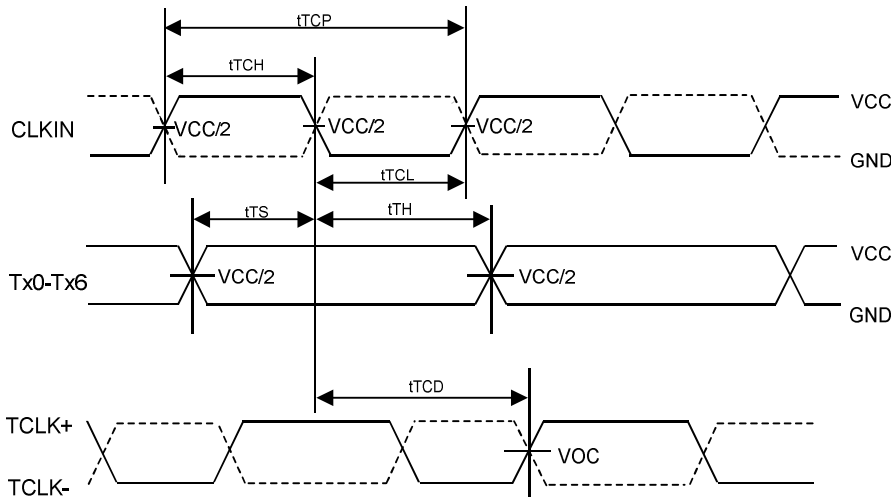
Figure 6. LVDS Output Load and Transmission Time

AC Timing Diagrams

LVC MOS Inputs

Normal Swing Input

RS	VOD
VCC	350mV
0.6 ~ 1.4V	
GND	200mV

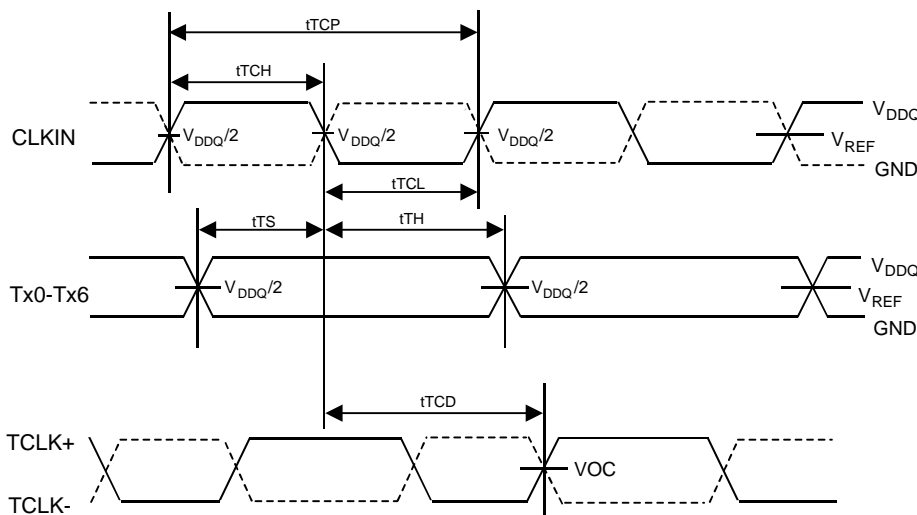


Note :  
 CLKIN : Solid line denotes the setting of R/F=GND  
 Dashed line denotes the setting of R/F = VCC

Figure 7. LVC MOS Inputs and LVDS Clock Output Timing 1

Small Swing Inputs

RS	VREF
VCC	---
0.6 ~ 1.4V	V <sub>DDQ</sub> /2
GND	---

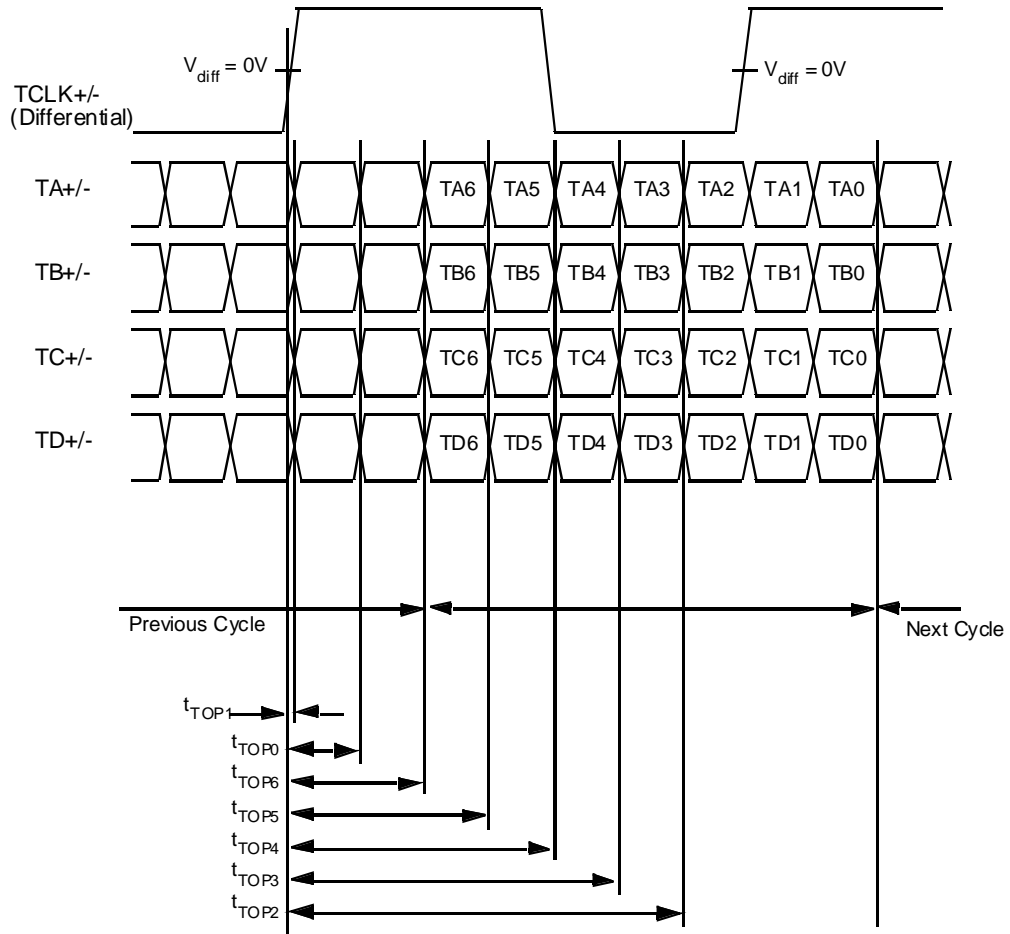


Note :  
 CLKIN : Solid line denotes the setting of R/F=GND  
 Dashed line denotes the setting of R/F = VCC

Figure 8. LVC MOS Inputs and LVDS Output Timing 2

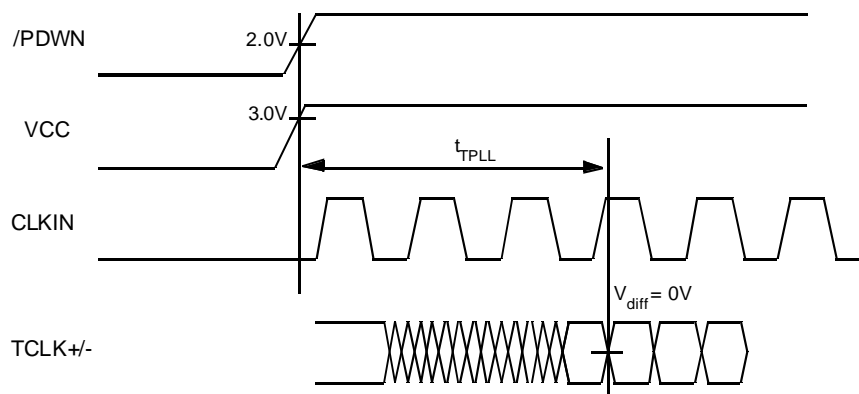


### LVDS Output Data Position



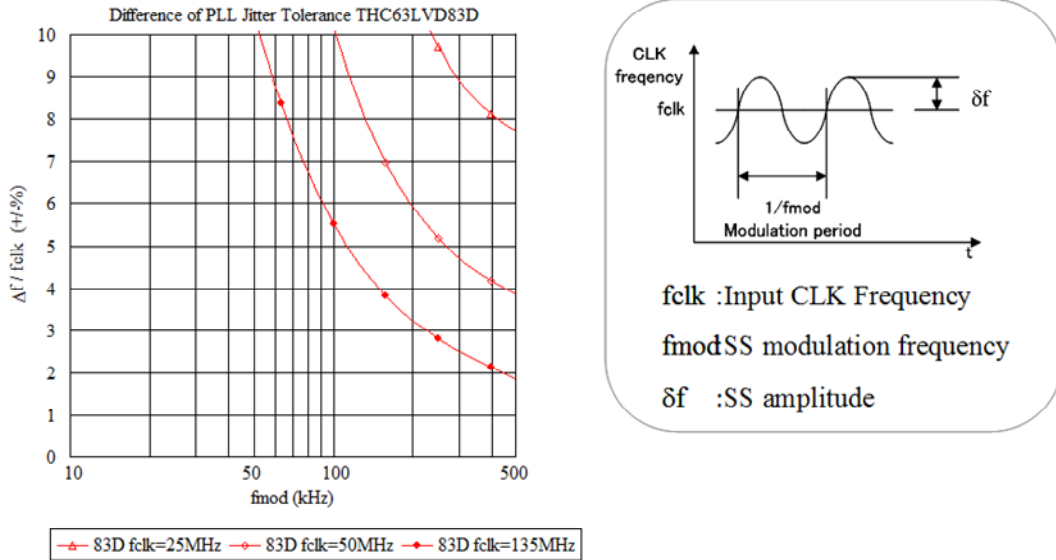
**Figure 9. LVDS Output Data Position**

### Phase Lock Loop Set Time



**Figure 10. PLL Lock Loop Set Time**

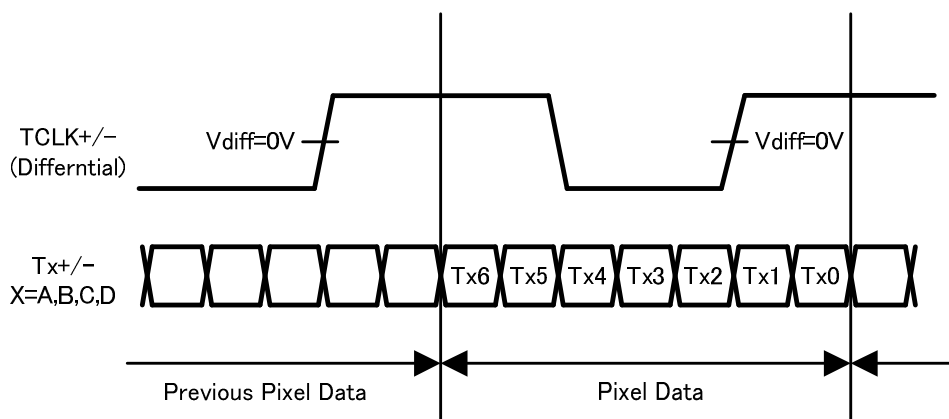
### Spread Spectrum Clocking Tolerant



**Figure 11. Spread Spectrum Clocking Tolerant**

The graph indicates the range that the IC works normally under SS clock input operation. The results are measured with a typical sample on condition of +25C° and 3.3V, therefore these values are for reference and do not guarantee the performance of a product under other circumstance.

### LVDS Data Timing Diagram



**Figure 12. LVDS Data Timing Diagram**

**For Display Application**

THC63LVDM83D Pixel Data Mapping for JEIDA Format (6bit, 8bit Application)

	6bit	8bit
TA0	R2	R2
TA1	R3	R3
TA2	R4	R4
TA3	R5	R5
TA4	R6	R6
TA5	R7	R7
TA6	G2	G2
TB0	G3	G3
TB1	G4	G4
TB2	G5	G5
TB3	G6	G6
TB4	G7	G7
TB5	B2	B2
TB6	B3	B3
TC0	B4	B4
TC1	B5	B5
TC2	B6	B6
TC3	B7	B7
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	-	R0
TD1	-	R1
TD2	-	G0
TD3	-	G1
TD4	-	B0
TD5	-	B1
TD6	-	N/A

Note : Use TA to TC channels and open TD channel for 6bit application.

**Table 8. Data Mapping for JEIDA Format**

THC63LVDM83D Pixel Data Mapping for VESA Format (6bit, 8bit Application)

	6bit	8bit
TA0	R0	R0
TA1	R1	R1
TA2	R2	R2
TA3	R3	R3
TA4	R4	R4
TA5	R5	R5
TA6	G0	G0
TB0	G1	G1
TB1	G2	G2
TB2	G3	G3
TB3	G4	G4
TB4	G5	G5
TB5	B0	B0
TB6	B1	B1
TC0	B2	B2
TC1	B3	B3
TC2	B4	B4
TC3	B5	B5
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	-	R6
TD1	-	R7
TD2	-	G6
TD3	-	G7
TD4	-	B6
TD5	-	B7
TD6	-	N/A

Note : Use TA to TC channels and open TD channel for 6bit application.

**Table 9. Data Mapping for VESA Format**

Typical Connection

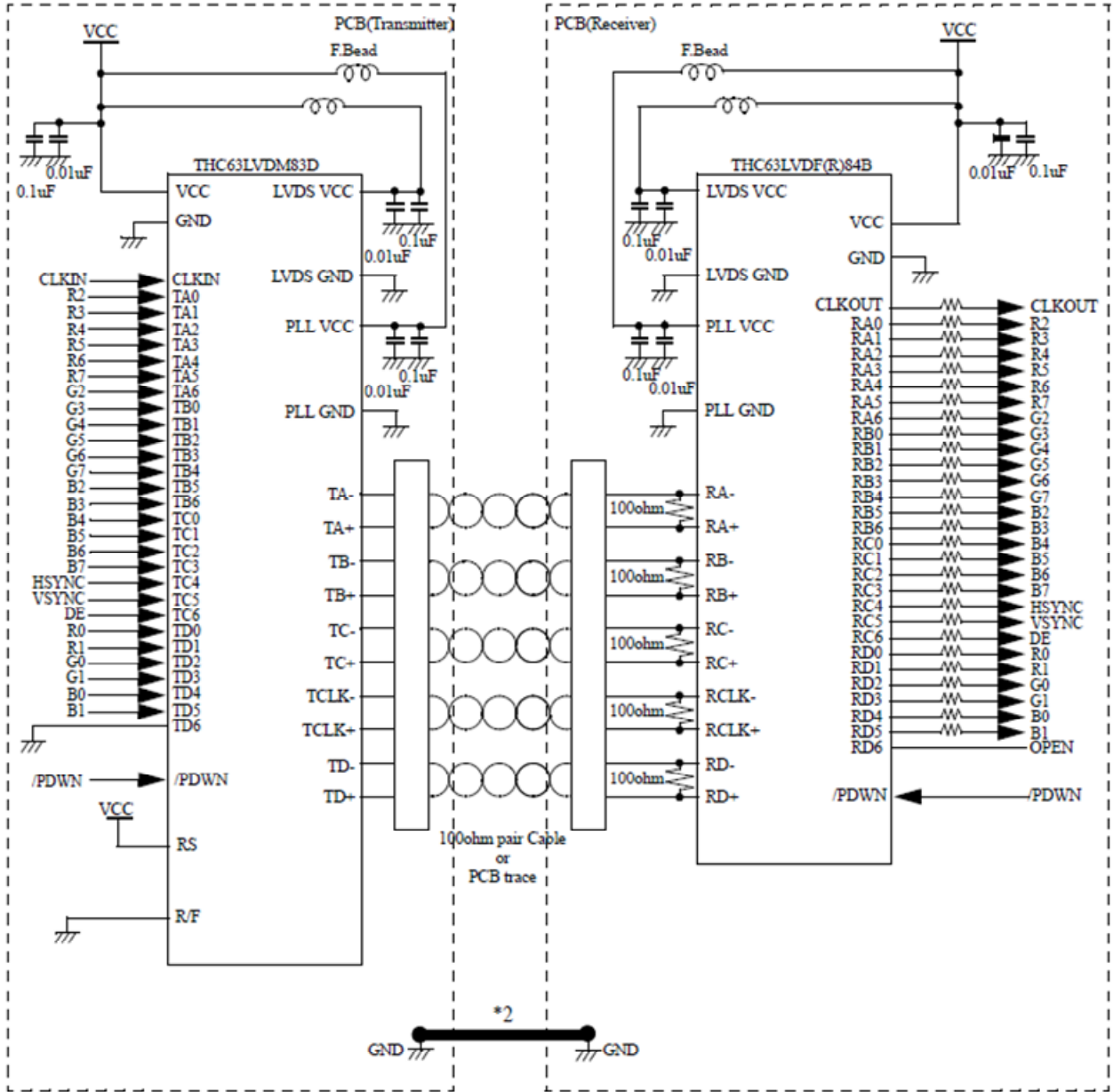


Figure 13. Typical Connection Diagram

Notes

1) Cable Connection and Disconnection

Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which THC63LVDM83D and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

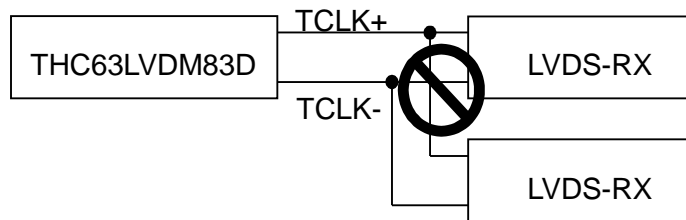


Figure 14. Multi Drop Connection

4) Asynchronous use

Asynchronous using such as following systems is not recommended.

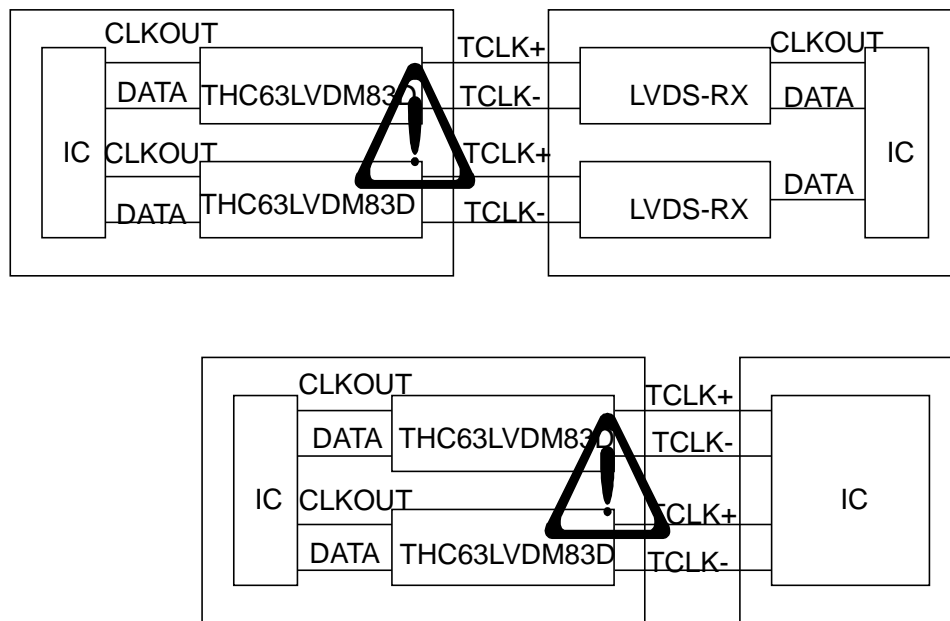


Figure 15. Asynchronous Use

Package

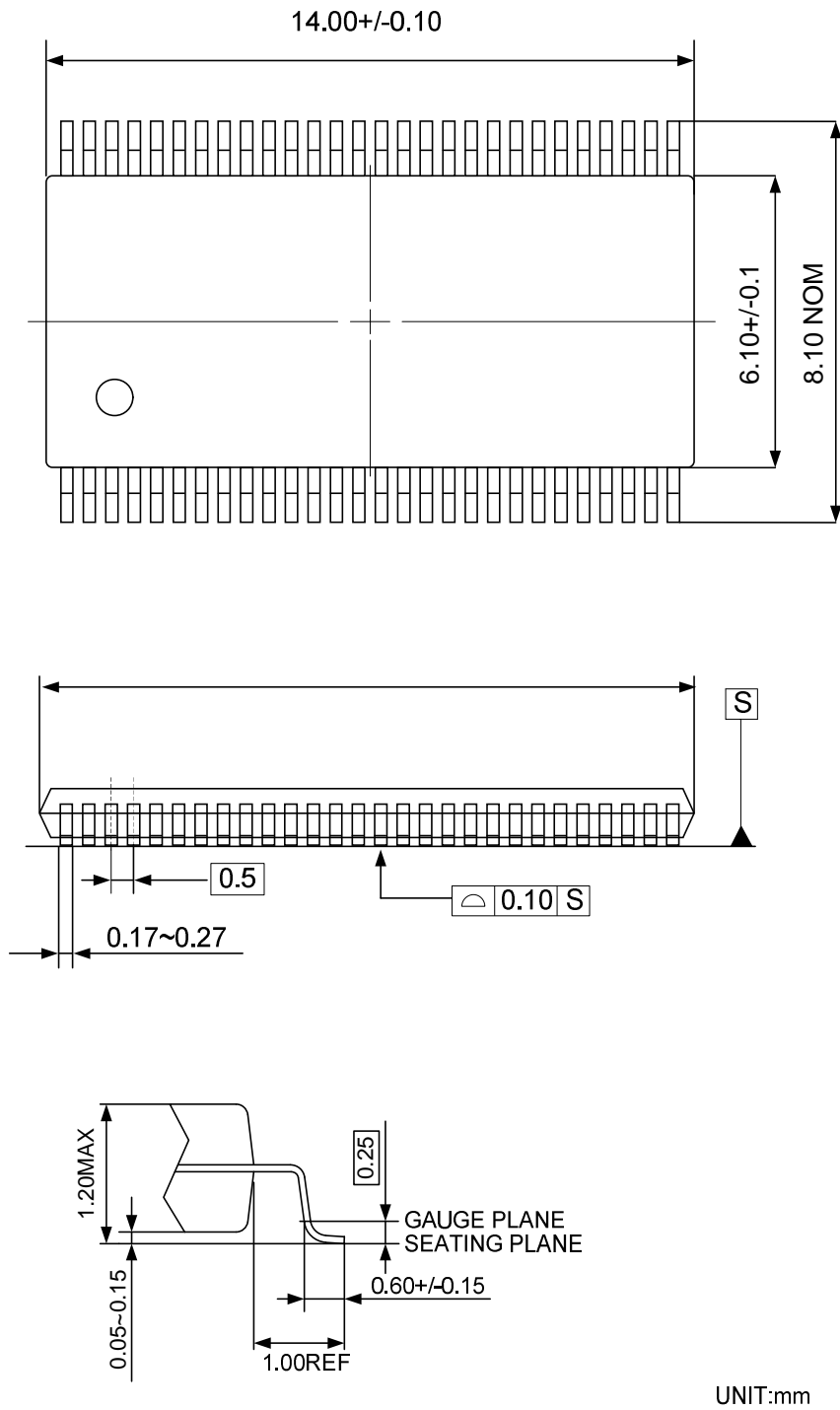
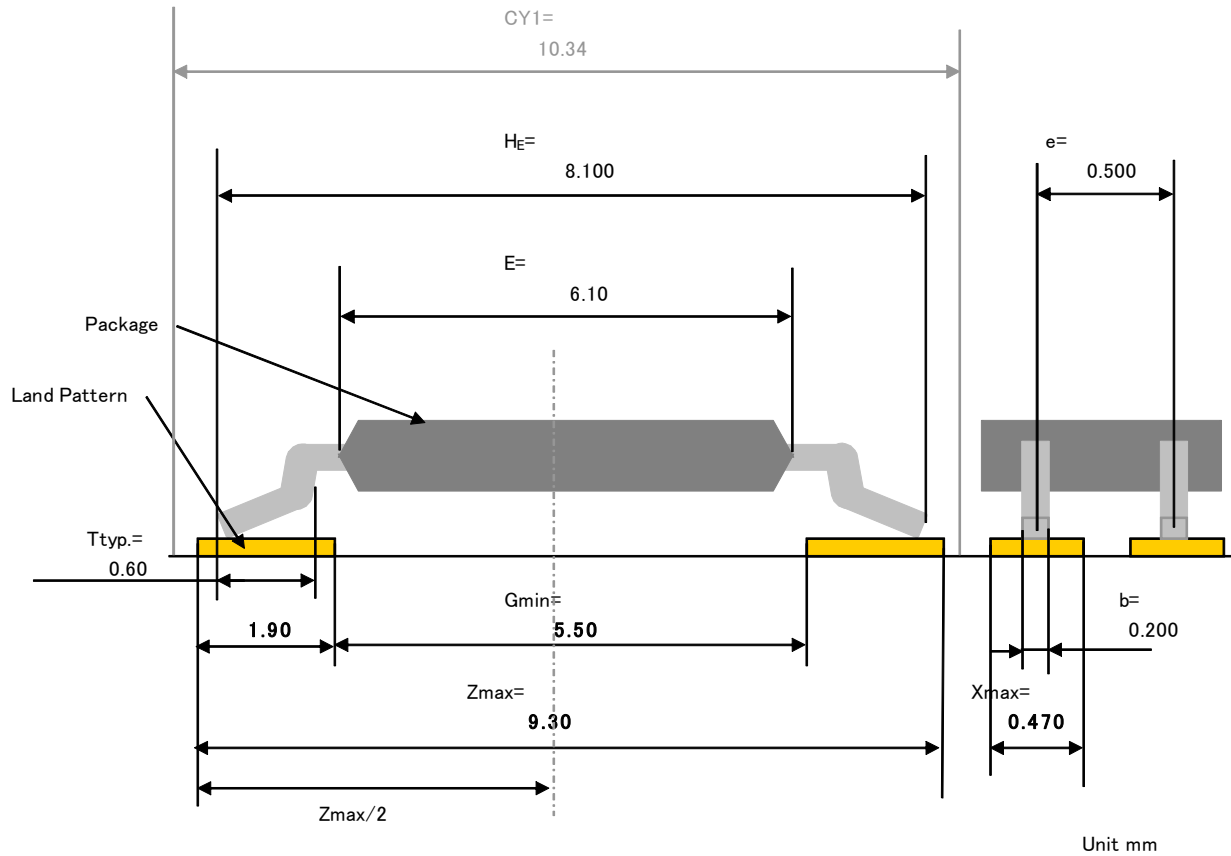


Figure 16. Package Diagram

Reference Land Pattern



**Figure 17. Reference of Land Pattern**

The recommendation mounting method of THine device is reflow soldering.  
 The reference pattern is using the calculation result on condition of reflow soldering.

Notes

This land pattern design is a calculated value based on JEITA ET-7501.  
 Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc... The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.



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