

THC7984

10-bit 3-channel Video Signal Digitizer

General Description

The THC7984 integrates all the functions to digitize analog video signals on a single chip.

Acceptable Signals

PC Graphics (RGB) : VGA-UXGA

- Separate Sync
- Composite Sync
- Sync on Green

Component Video (YPbPr) :

- SDTV (480i / 480p) 2-level Sync
- HDTV (1080i / 720p / 1080p) 3-level Sync
- Protection Signal

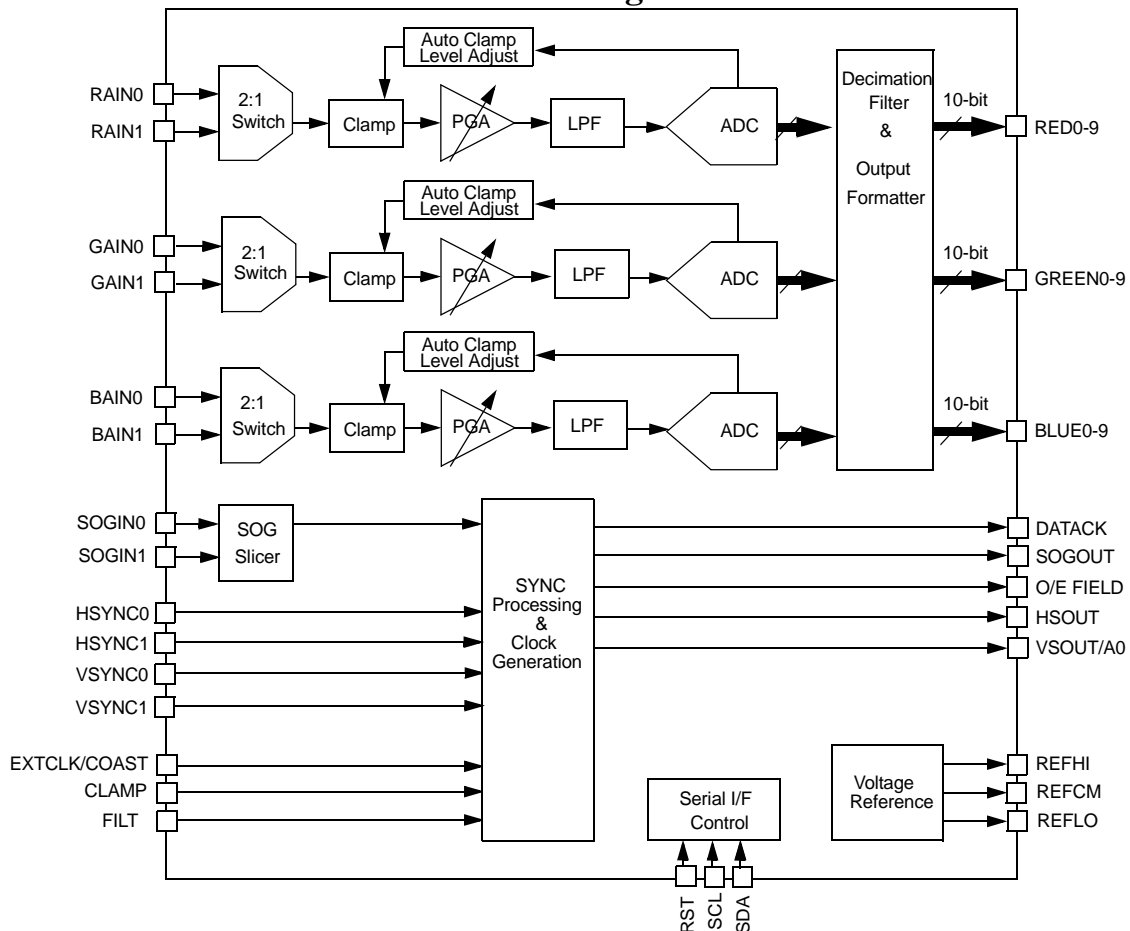
Applications

- LCD TV / PDP TV
- Rear-Projection TV
- LCD Display / PDP Display
- Front Projector etc.

Features

- 170 MSPS 10-bit ADC
- Internal 14-bit ADCs
- Oversampling functions (2x, 4x, and 8x)
- Line-locked PLL with low jitter
- Phase adjustment: 64 steps
- Fine clamp / preamp
- Pedestal / center clamp
- Clamp level auto adjust
- Very low gain mismatch
- Gain adjustment: 2048 steps
- Video Filter (LPF)
- Bandwidth adjustment: 28 steps (6MHz - 310MHz)
- Sync Processor
- 2-level / 3-level sync slicer
- Advanced sync detection / measurement
- Automatic sync processing mode
- IRQ Output
- 2-wire serial interface
- TQFP 80-pin package

Block Diagram



Specifications

VD=1.8V, VDD=3.3V, PVD=1.8V, DAVDD=1.8V, ADC Clock=Maximum Conversion Rate, Full Temperature Range=0° C to 70° C
Analog Input Voltage=0.5 to 1.0Vpp

Parameter	Temp	Test Level	THC7984-17			Unit		
			Min	Typ	Max			
RESOLUTION	Number of Bits			10		Bits		
	LSB Size			0.098		%FS		
DC ACCURACY	25° C	I	Differential Nonlinearity		± 0.75	± 1	LSB	
			Integral Nonlinearity			-1.0/+1.25	LSB	
	Full	VI	Integral Nonlinearity		± 1.5	± 3	LSB	
			No Missing Code		Guaranteed		LSB	
ANALOG INPUT	Full	VI	Minimum Input Voltage			0.5	V p-p	
	Full	VI	Maximum Input Voltage		1.0		V p-p	
	25° C	V	Gain Tempco		100		ppm/° C	
	25° C	IV	Input Bias Current*1			1	µA	
						1	µA	
	Full	VI	Input Offset Voltage		± 1		LSB	
	Full	VI	Input Full-Scale Matching Between Channels		0.2	0.8	%	
	Full	VI	Offset Adjustment Range		50		%FS	
SWITCHING PERFORMANCE	Full	VI	Maximum Conversion Rate		170		MSPS	
	Full	IV	Minimum Conversion Rate			10	MSPS	
	Full	IV	Data Setup Time to Clock*2		0.48Tpixel-2.1		ns	
	Full	IV	Data Hold Time to Clock*2		0.48Tpixel-0.4		ns	
	Full	IV	Duty Cycle, DATA*2		40	50	60	%
	Full	IV	HSYNC Input Frequency		15		110	kHz
	Full	VI	Maximum PLL Clock Rate		170		MHz	
	Full	IV	Minimum PLL Clock Rate				10	MHz
	25° C	V	PLL Jitter*3		500		ps p-p	
	Full	IV	Sampling Phase Tempco		15		ps/° C	
2-WIRE SERIAL INTERFACE	Full	IV	SCL Clock Frequency (fSCL)			100	kHz	
	Full	IV	tBUFF		4.7		µs	
	Full	IV	tSTAH		4.0		µs	
	Full	IV	tDHO		0	3.45	µs	
	Full	IV	tDAL		4.7		µs	
	Full	IV	tDAH		4.0		µs	
	Full	IV	tDSU		250		ns	
	Full	IV	tSTASU		4.7		µs	
	Full	IV	tSTOSU		4.0		µs	
	Full	IV	Tr			1000	ns	
	Full	IV	Tf			150	ns	
	Full	IV	Capacitive Load (Cb)			400	pF	
	Full	IV	Noise margin at the LOW level (VnL)		0.2		V	
	Full	IV	Noise margin at the HIGH level (VnH)		0.25		V	
	DIGITAL INPUTS	Full	VI	Input Voltage, High (VIH)		1.4		V
Full		VI	Input Voltage, Low (VIL)			0.8	V	
Full		V	Input Current, High (IIH)			10	µA	
Full		V	Input Current, Low (IIL)			10	µA	
25° C		V	Input Capacitance			2	pF	
DIGITAL OUTPUTS	Full	VI	Output Voltage, High (VOH)		VDD-0.2		V	
	Full	VI	Output Voltage, Low (VOL)			0.2	V	
	Output Coding				Binary			
POWER SUPPLY	Full	IV	VD Supply Voltage		1.7	1.8	1.9	V
	Full	IV	VDD Supply Voltage		2.3	3.3	3.45	V
	Full	IV	PVD Supply Voltage		1.7	1.8	1.9	V
	Full	IV	DAVDD Supply Voltage		1.7	1.8	1.9	V
	25° C	V	ID Supply Current (VD)				295	mA
	25° C	V	IDD Supply Current (VDD)*4				180	mA
	25° C	V	IPVD Supply Current (PVD)				30	mA
	25° C	V	IDAVDD Supply Current (DAVDD)				65	mA
	Full	VI	Total Power Dissipation				1350	mW
	Full	VI	Power-Down Supply Current			10	20	mA
	Full	VI	Power-Down Dissipation			20	40	mW
THERMAL CHARACTERISTICS	Operating Ambient Temperature		IV	0		70	° C	
	25° C	V	θ JC Junction-to-Case Thermal Resistance		4		° C/W	
	25° C	V	θ JA Junction-to-Ambient Thermal Resistance		37		° C/W	

*1 Input Bias Voltage: 0.05V to VD-0.05V

*2 See "Data/Clock Output Test Condition".

*3 THC7984-17: UXGA@60Hz

*4 Output Load Capacitance per Pin: 15pF

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at +25° C and sample tested at specified temperatures.

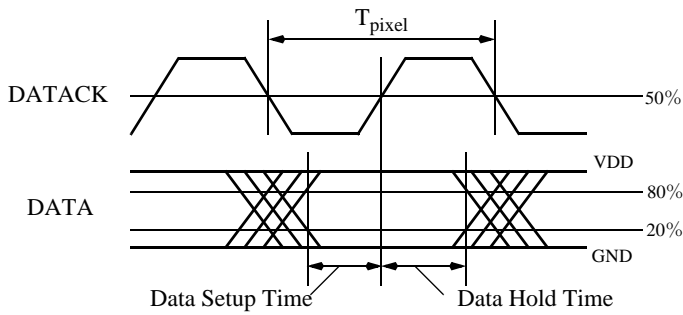
III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

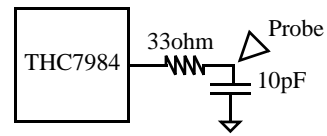
V. Parameter is a typical value only.

VI. 100% production tested at +25° C; guaranteed by design and characterization testing.

< Data Setup/Hold Time to Clock >



< Data /Clock Output Test Condition >



DATAACK: Pixel Clock
 DATAACK Phase: 4
 Output Format: Normal (not DDR)
 Output Drive Strength (VDD=3.3V) : Medium

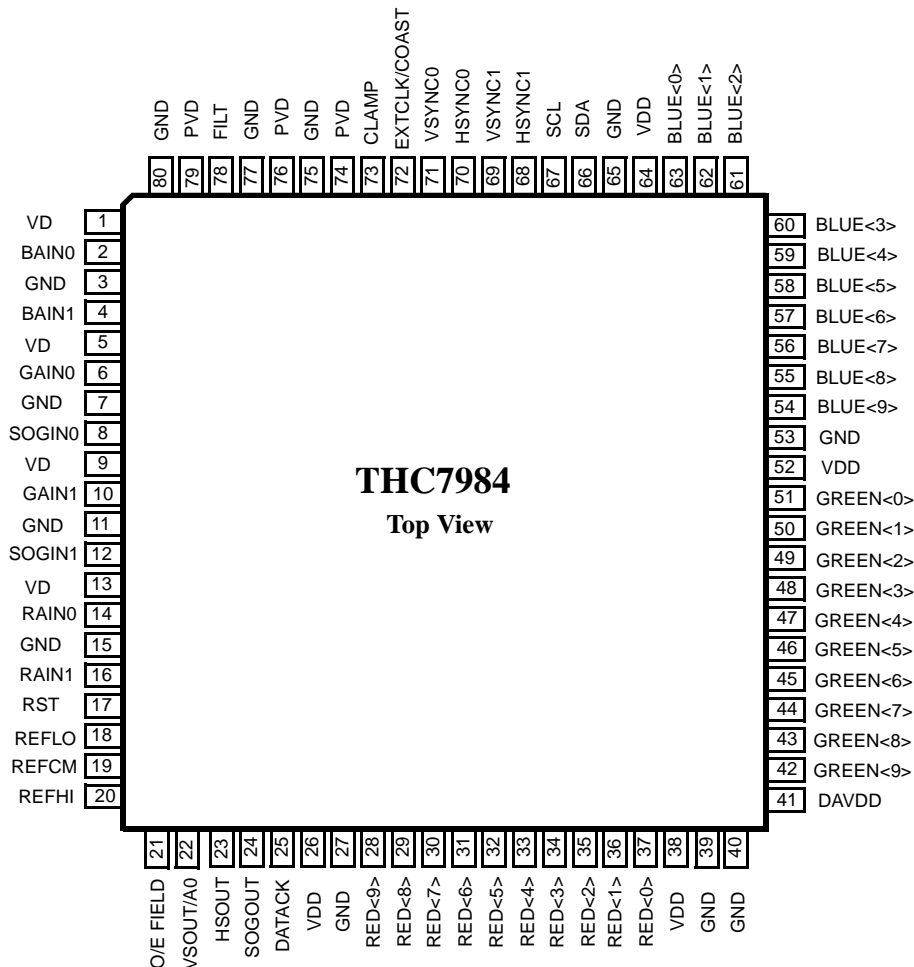
*DATAACK output phase is register programmable.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
VD		2.1	V
VDD		3.8	V
PVD		2.1	V
DAVDD		2.1	V
Analog Inputs	-0.2	VD+0.2 or 2.1*1	V
Digital Inputs	-0.3	PVD+3.6 or 5.5V*1	V
Storage Temperature	-55	150	° C
Maximum Junction Temperature		125	° C

*1 Smaller Value is adopted.

Pin Configuration



Pin List

Pin Name	Type	Function
VD	P	Analog Power Supply
VDD	P	Output Power Supply
PVD	P	PLL Power Supply
DAVDD	P	Digital Core Power Supply
GND	P	Ground
BAIN0	AI	B-ch Analog Input, Port 0
BAIN1	AI	B-ch Analog Input, Port 1
GAIN0	AI	G-ch Analog Input, Port 0
SOGIN0	AI	Sync on Green Input, Port 0
GAIN1	AI	G-ch Analog Input, Port 1
SOGIN1	AI	Sync on Green Input, Port 1
RAIN0	AI	R-ch Analog Input, Port 0
RAIN1	AI	R-ch Analog Input, Port 1
RST	DI	Reset Input Low: Normal Operation High: Power Down (Stand-by) High → Low: Chip Reset
REFLO	-	Connection for External Capacitor
REFCM	-	Connection for External Capacitor
REFHI	-	Connection for External Capacitor
O/E FIELD	DO	Field Parity Output for Interlaced Video <Other Function> Data Enable (DE) Output Sync Processor IRQ Output
VSOUT/A0	DIO	VSYNC Output / Serial Interface Device Address bit 0 (A0)
HSOUT	DO	HSYNC Output
SOGOUT	DO	SOG Slicer Output
DATAACK	DO	Data Clock Output
RED<9:0>	DO	R-ch Data Output
GREEN<9:0>	DO	G-ch Data Output
BLUE<9:0>	DO	B-ch Data Output
SCL	DI	Serial Port Data Clock Input
SDA	DIO	Serial Port Data I/O
HSYNC1	DI	HSYNC Input, Port 1
VSYNC1	DI	VSYNC Input, Port 1
HSYNC0	DI	HSYNC Input, Port 0
VSYNC0	DI	VSYNC Input, Port 0
EXTCLK/COAST	DI	External Clock Input / Coast Signal Input
CLAMP	DI	External Clamp Pulse Input <Other Function> Reference Clock Input for HSYNC Period Measure
FILT	-	Connection for PLL Loop Filter

P:Power AI:Analog Input DI:Digital Input DO:Digital Output DIO:Digital Input/Output

Functional Description

Digital Input

- All digital inputs are 5V tolerant during power-on.

Analog Input

- The THC7984 has two ports that each include three analog inputs for RGB or YPbPr. The input port can be selected by register.
- In case input signals are YPbPr, Y may be input into GAIN0 (or GAIN1) and SOGIN0 (or SOGIN1), Pr into RAIN0 (or RAIN1), and Pb into BAIN0 (or BAIN1).
- The THC7984 accommodates analog signals ranging from 0.5 V_{pp} to 1.0 V_{pp}.

Video Filter (LPF)

The THC7984 has 2 kinds of low-pass filters.

- 5th-order LPF for YPbPr, whose bandwidth is adjustable from 6 MHz to 92 MHz in 24 steps.
- 2nd-order LPF for RGB, whose bandwidth is adjustable in 4 steps (40 MHz, 90 MHz, 170 MHz, and 310 MHz).

Serial Interface

- The THC7984 is controlled by 2-wire serial interface.
- Serial clock SCL supports up to 100 kHz.

Sync Input

- The THC7984 has two ports that each include two digital inputs for the separate sync (HSYNC and VSYNC). The input port can be selected by register.
- The THC7984 can process composite sync (CSYNC). CSYNC may be input into HSYNC0 or HSYNC1.

Digital Output

- The digital outputs can operate from 2.5 V to 3.3 V (VDD).
- The output drive strength is programmable by 2-bit registers (except SDA).

Clamp

- Pedestal clamp for RGB and Y (luminance) clamps black level to 0 with automatic offset cancel.
- Midscale clamp for PbPr clamps to 512 with automatic offset cancel.
- 256-level clamp for Y (luminance) clamps to 256 with automatic offset cancel. It can be used for A/D conversion of Y including sync signal. In this case, input signal needs to be attenuated to put it within the input range of A/D converter.
- Clamp pulses can be input from CLAMP pin when external clamp is selected.

Gain, Offset

- Gain is programmable by 11-bit registers (2048 steps).
- Offset from -256 to +255 can be added to the output code.
- Gain and offset can be adjusted independently.

Reference Voltage

- The THC7984 has Band Gap Reference inside and doesn't require external voltage reference.
- The internal reference voltages (REFHI, REFCM, and REFLO) must be bypassed to stabilize. Each pin (REFHI, REFCM, and REFLO) is connected to ground through a 10 μ F capacitor.

Sampling Clock Generation

- The THC7984 has PLL to generate the sampling clock from HSYNC. The sampling clock frequency range is from 10MHz to 170 MHz.
- PLL divider ratio (the number of horizontal total pixels per line) can be set to the value between 200 to 8191.
- The sampling clock Phase can be adjusted in 64 steps of T/64.
- The external clock can be used as the sampling clock.
- It is required to set VCO Frequency Range and Charge Pump Current according to the input signal format (resolution) .

Oversampling

- Oversampling is the function that enables sampling analog signals with higher rate than the pixel clock and downsampling to the pixel clock rate with decimation filter, which is effective for improving S/N ratio.
- Oversampling ratio can be selected among 1x (normal operation) , 2x, 4x, and 8x. Even if any is selected, output frequency of the output clock and data is same as normal operation.

Output Clock (DATAACK)

- The output clock phase can be selected in 8 steps for the data setup/hold adjustment.
- Divide-by-2 clock can be selected as the output clock for the dual edge data clocking at the subsequent stage. It can not be selected when oversampling.

SOG Slicer

- Sync on Green (SOG) is sliced at the threshold level above the sync tip to extract the sync signal. The threshold level can be set by a register ranging from 15 mV to 240 mV in steps of 15mV.
- Low pass filter prior to the slicer can be used to reduce high frequency noise, which can be disabled by a register.
- The slicer also has hysteresis (about 30mV) , which can be disabled by a register.
- 3-level sync signal can be processed by slicing at the pedestal level.

Sync Processor

Sync Processor implements VSYNC separation from CSYNC, vertical timing generation, and detection and measurement of the sync signals. The various automatic sync-processing modes are realized by utilizing the sync detection and measurement.

The THC7984 can process the copy protection signal.

(1) VSYNC Separation

Extracting VSYNC from Composite sync (CSYNC) or Sync on Green (SOG) .

(2) Vertical Timing Generation

- VSYNC Output Generation
- PLL COAST Generation
- Clamp COAST Generation
- V-Blank of DE Generation

(3) Sync Detection/Masurement

- Input Sync Type Detection (Separate sync, Composite sync, Sync on Green, and No input signal)
- HSYNC, VSYNC Input Polarity Detection
- 3-level Sync Detection
- Interlace Detection
- Vertical Total Line Measurement
- VSYNC Input Pulse Width Measurement
- HSYNC Period Measurement (Reference clock needs to be input into CLAMP pin.)
- SYNC Change Detection
- HSYNC Edge Detection
- Sync Processor IRQ Output

(4) Automatic Sync Processing Mode (Manual Setting Modes are also available)

- Auto Output Mode (All outputs are enabled when input signal is active)
- Input Port Auto Select (Selects the port whose input signal is active)
- Input Sync Type Auto Select (HSYNC Input, VSYNC Input)
- HSYNC, VSYNC Input Polarity Auto Select
- HSYNC, VSYNC Output Polarity Auto Select
- VSYNC Output Timing Auto Setting
- PLL COAST Timing Auto Setting

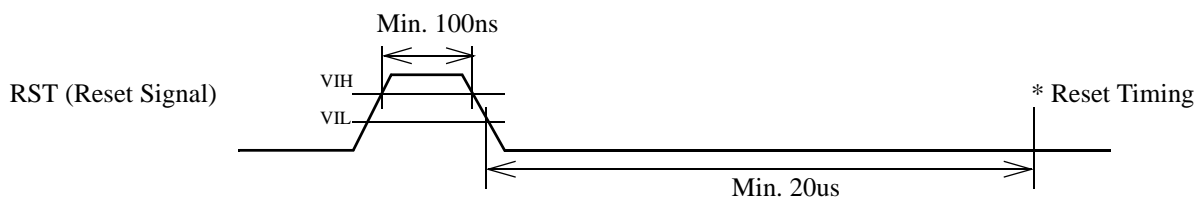
Power Control

- The THC7984 can be set to stand-by mode by a register or RST-pin.
- In stand-by mode, most of the analog circuits are powered down for low power dissipation.
- In stand-by mode, the sync detection and measurement are available nonetheless because SOG Slicer, Sync Processor, and 2-wire serial interface are still power-on.
- The THC7984 is set to stand-by mode when RST-pin is set to High. If unused, RST-pin must be pull-down to ground with a resistor.

Reset

- The logic circuit of the chip is reset when power is applied with RST-pin asserted Low (Power-on Reset) .
 - The reset can be also triggered by RST-pin (Manual Reset) . The reset is triggered when RST-pin falls from High to Low, that means the reset is triggered whenever the THC7984 gets out of stand-by mode by RST-pin.
 - Reset after power-up is necessary to access the serial interface. Please power-up with RST-pin asserted Low or make RST-pin High then Low after power-up. If unused, RST-pin must be pull-down to ground with a resistor.
 - The registers are set to the default values by the reset and the chip becomes stand-by mode and output disable (Hi-Z) .
- For normal operation, the registers must be set to power-on and output enable by the serial interface.

- For Manual Reset, keep RST-pin Low more than 20 us after the transition from High to Low.

**Device Address**

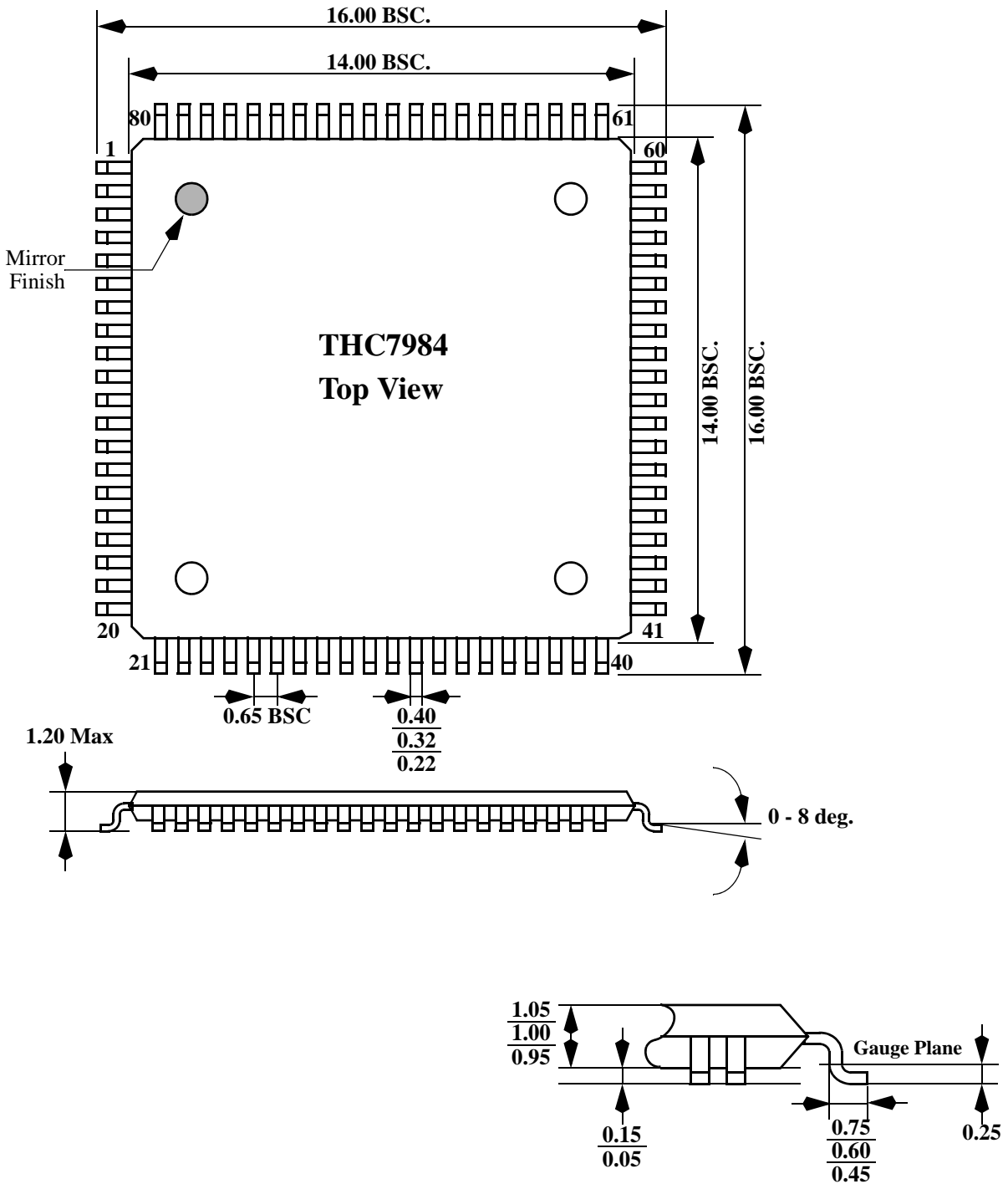
- The LSB of 7-bit device address of serial interface (A0) is obtained from VSOUT/A0-pin at the reset.

Pull-down to ground with a resistor (10 k Ω) , then Device Address is set to 1001100

Pull-up to VDD with a resistor (10 k Ω) , then Device Address is set to 1001101

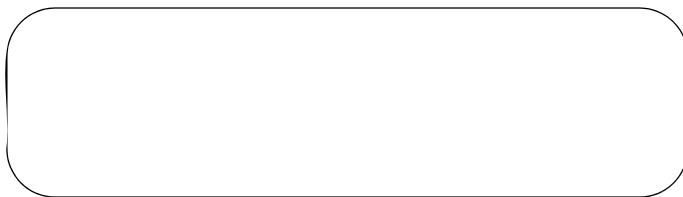
- The pull-up resistor must be connected to VDD.

Package Dimension (Unit: mm)



Other Precautions and Requirements

1. The specification in this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay more particular attention to circuit designing. Even if there are improper expressions in the documents, we are not responsible for any problem due to them. Please note that improper expressions may not be corrected immediately even if found.
3. Our copyright and know-how are included in this data sheet. Duplication of the data sheet and disclosure to the third party are strictly prohibited without our permission.
4. We are not responsible for any problem on industrial proprietorship occurring due to the use of the THC7984, except for those directly related to the product structure, manufacturing methods and functions.
5. The THC7984 is designed on the premise that it should be used for ordinary electronic devices. Therefore, it shall not be used for applications that require extremely high-reliability (space equipment, nuclear control equipment, medical equipment that affects the human life, etc.) . In addition, when the THC7984 is used for traffic signals, safety devices and control/safety units in transportation equipment, etc., appropriate measures should be taken.
6. We are making every effort to improve the quality and reliability of our products. However, a very low probability of failure will occur in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
7. Radiation-resistant design is not incorporated in the THC7984.
8. It is due to user's judgement whether or not the THC7984 pertains to one of the strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law.



THine Electronics, Inc.
sales@thine.co.jp