Application Note	*THAN0084_Rev.1.40_E*

THC63LVD1027 Application Note

Mode setting, System Diagram and PCB Design Guide

Date	Revision	Contents
2008/12/03	Rev.1.00_E	New created
2010/03/03	Rev.1.10_E	Caution for LVDS line connection is added
2010/03/11	Rev.1.20_E	Some descriptions are altered.
2010/06/07	Rev.1.30_E	Some descriptions are altered.
2011/09/13	Rev.1.40_E	Some descriptions are altered.

Contents

1. Mode Setting

Input/Output	RCLK2+/-	MODE1 (Input mode) H: Single L: Dual	MODE0 (Output mode) H: Single L: Dual
Dual-In/Dual-Out (Fig.2-1, 3-1)	CLK in	L	L
Distribution (Fig.2-2, 3-2)	Hi-z	L	L
Single-In/Dual-Out (Fig.2-3, 3-3)	Hi-z	H	L
Dual-In/Single-Out (Fig.2-4, 3-4)	CLK in	L	H
Reserved	--	H	H

2. Signal Flow for Each Setting

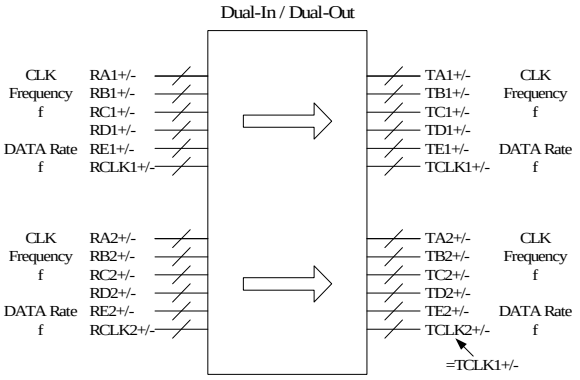


Fig2-1

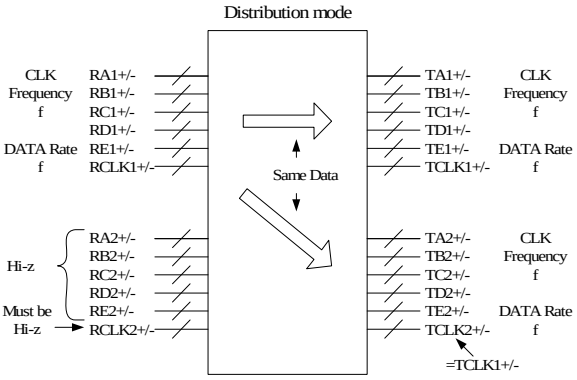


Fig2-2

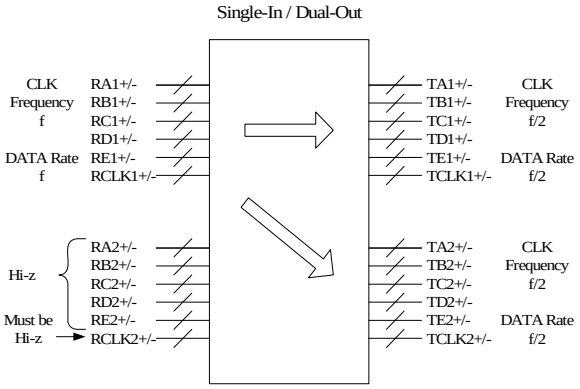


Fig2-3

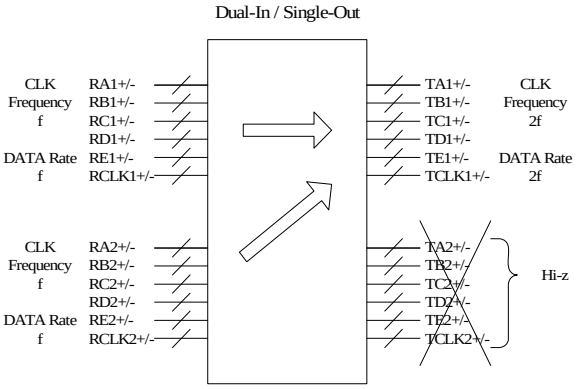


Fig2-4

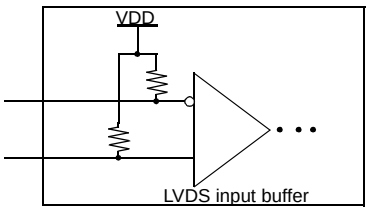
3. Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-z
H	Hi-z	*	All Hi-z
H	CLK in	CLK in	Refer to p.3 Mode Setting #
H	CLK in	Hi-z	Refer to p.3 Mode Setting #

* : Don't care
# : If a particular input data pair is Hi-z, the corresponding output data become L according to LVDS DC spec.

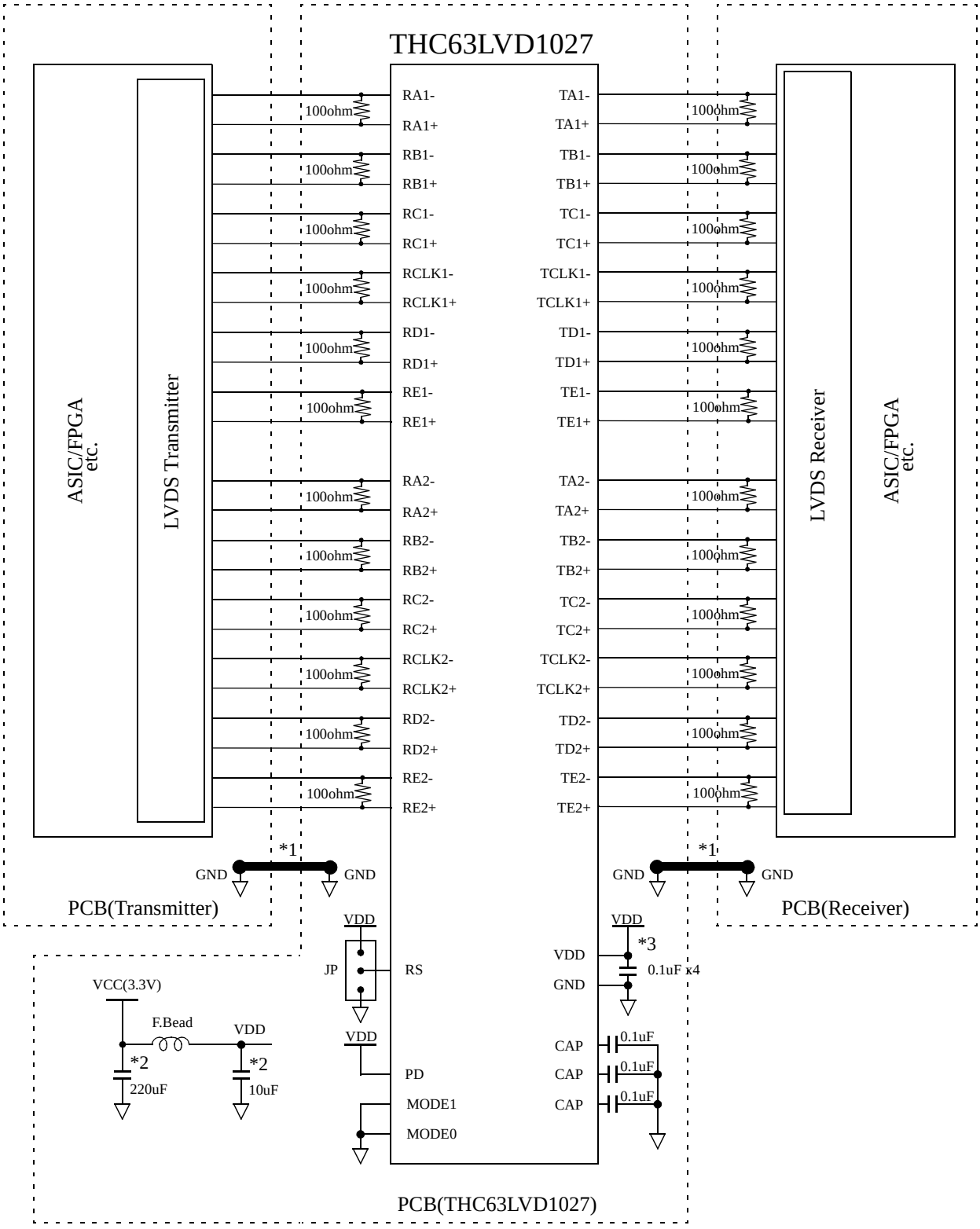
For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting state of Hi-z.



Internal circuit of THC63LVD1027

4. Example of System Diagram

4.1) Dual-In/Dual-Out (LVDS Input: 20~85MHz)



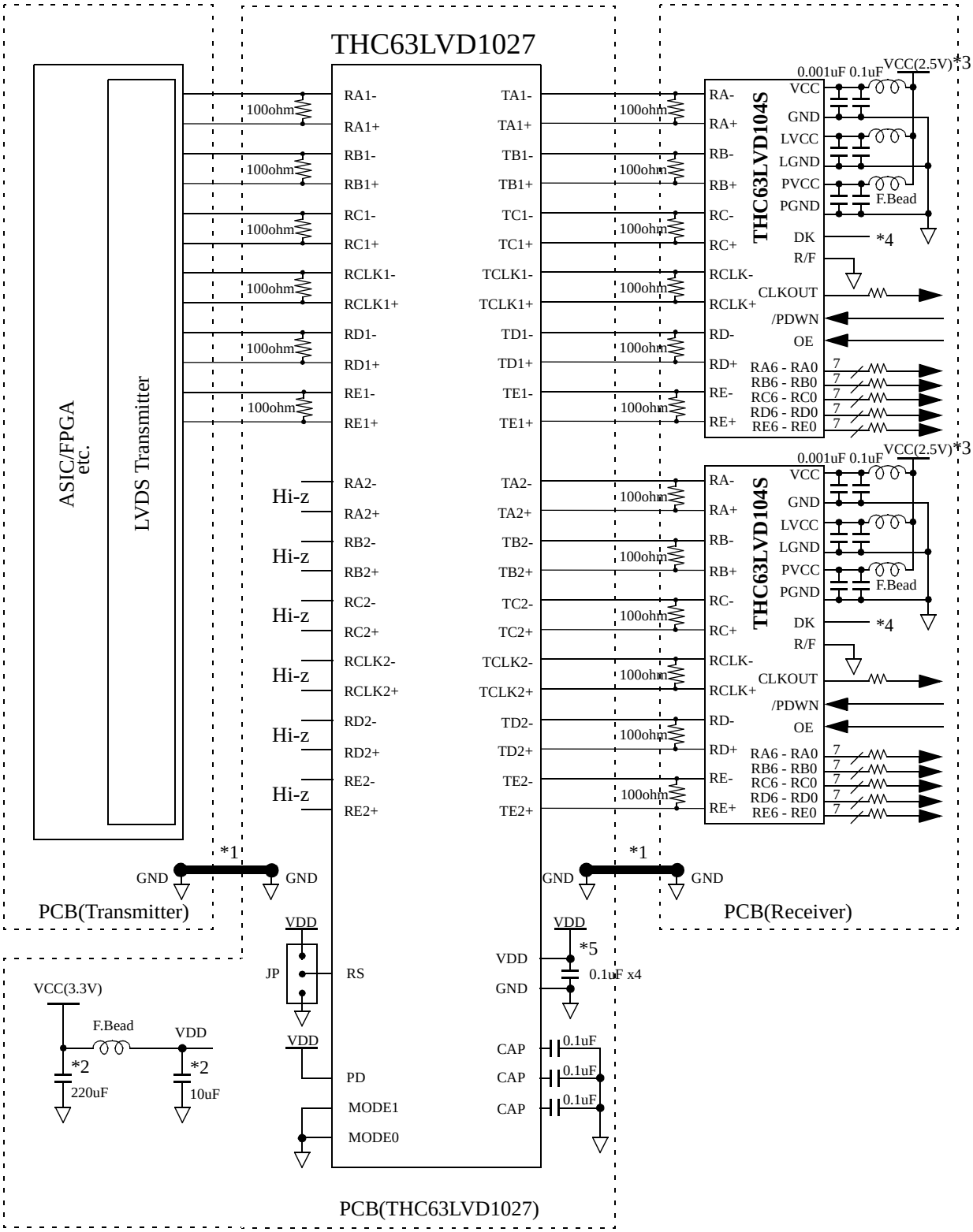
*1 Connect each PCB GND with low impedance cable.

*2 Select the suitable value for the system.

*3 Place 4 de-coupling capacitors close to each VDD pin one by one.

Fig3-1

4.2) Distribution (LVDS Input: 20~85MHz)



*1 Connect each PCB GND with low impedance cable.

*2 Select the suitable value for the system.

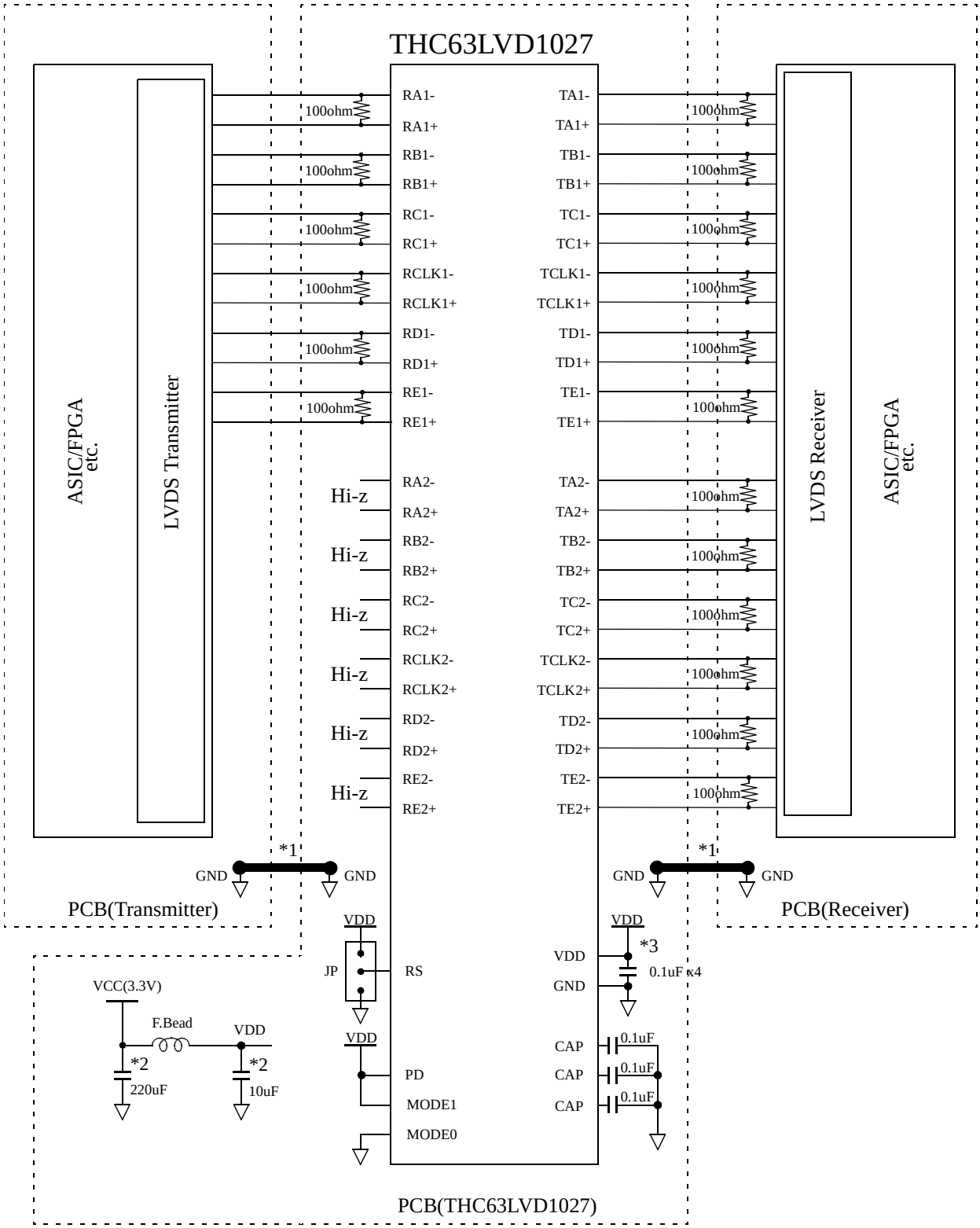
*3 Supply voltage of THC63LVD104S is 2.5V(Typ).

*4 Refer to datasheet.

*5 Place 4 de-coupling capacitors close to each VDD pin one by one.

Fig3-2

4.3) Single-In/Dual-Out (LVDS Input: 40~85MHz)



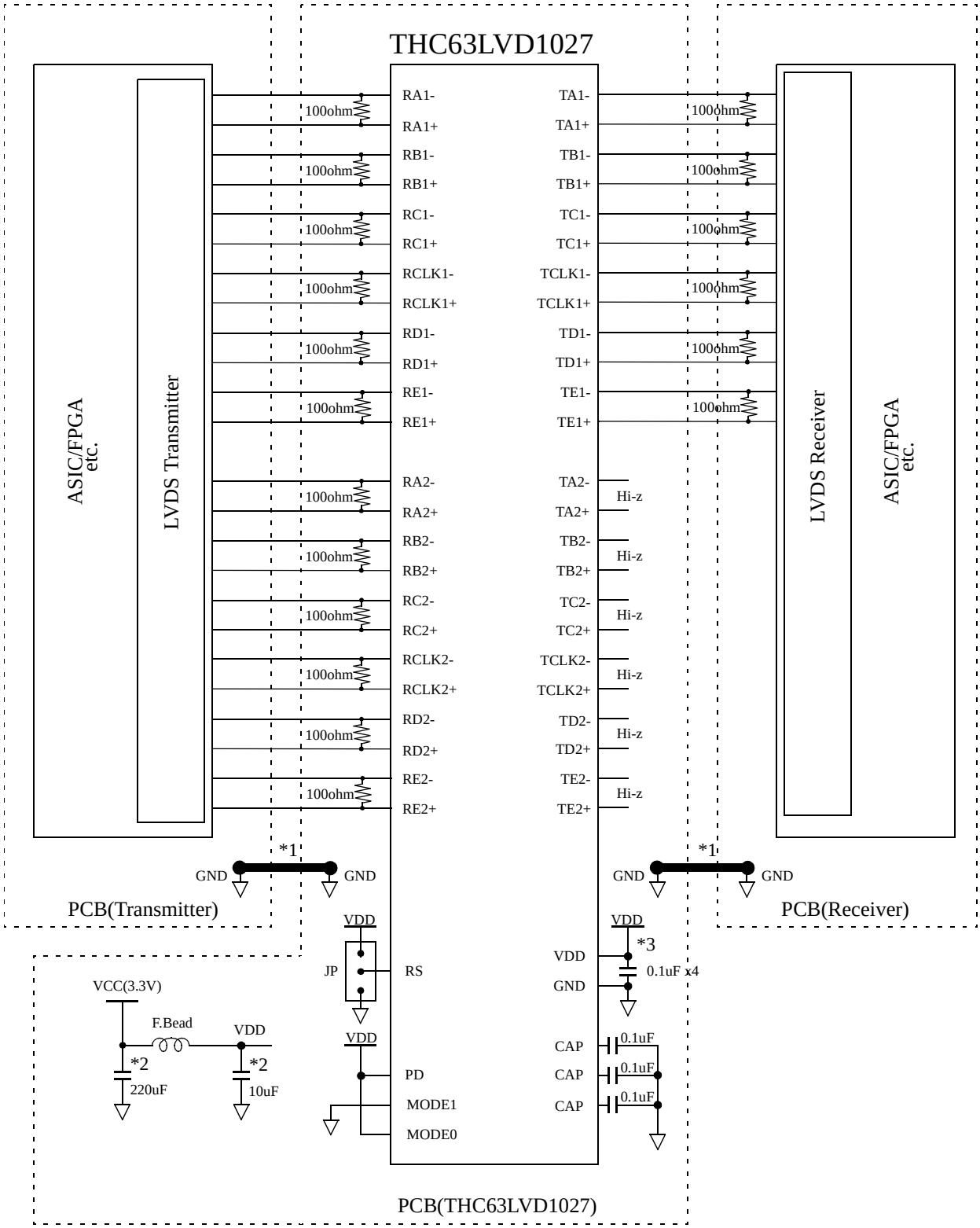
*1 Connect each PCB GND with low impedance cable.

*2 Select the suitable value for the system.

*3 Place 4 de-coupling capacitors close to each VDD pin one by one.

Fig3-3

4.4) Dual-In/Single-Out (LVDS Input: 20~42.5MHz)



*1 Connect each PCB GND with low impedance cable.

*2 Select the suitable value for the system.

*3 Place 4 de-coupling capacitors close to each VDD pin one by one.

Fig3-4

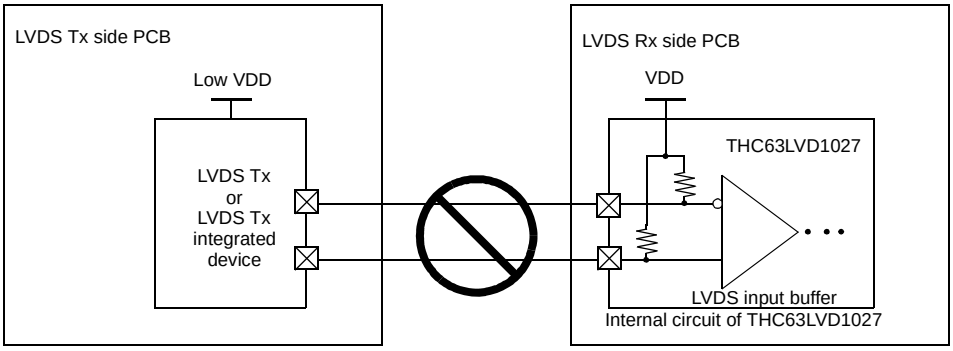
5. Note

5.1)LVDS input pin connection

When LVDS line is not drived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

If this situation is not avoidable and PD=L is hard to apply, there still is several remedy; therefore please contact to

mspsupport@thine.co.jp (for FAE mailing list)



5.2)Power On Sequence

Don't input RCLK#+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.
If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

5.3)Cable Connection and Disconnection

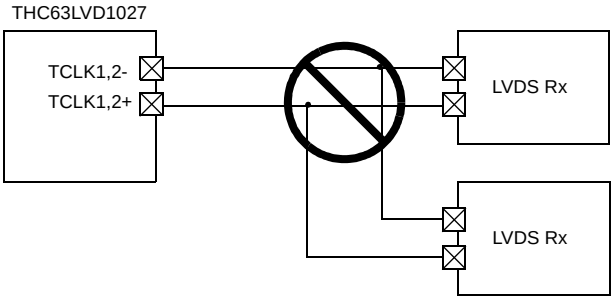
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

5.4)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

5.5)Multi Drop Connection

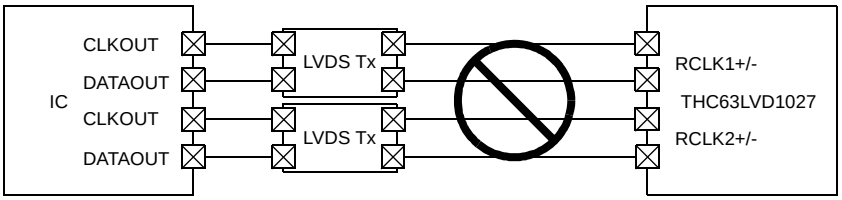
Multiple counterpart use such as following systems are not recommended.



5.6)Asynchronous use

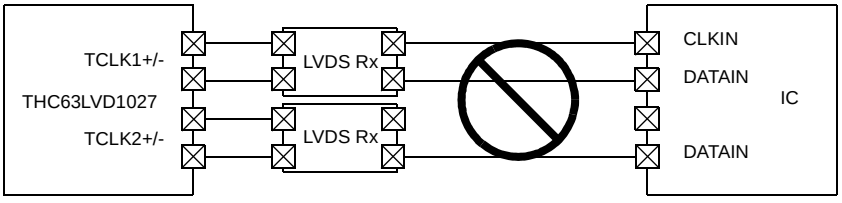
Asynchronous use such as following systems are not recommended.
If it is not avoidable, please check if datasheet p.11 tCK12 spec can be kept or not and more further, please contact to

mspsupport@thine.co.jp (for FAE mailing list)



Asynchronous use such as following systems are not recommended.
If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)



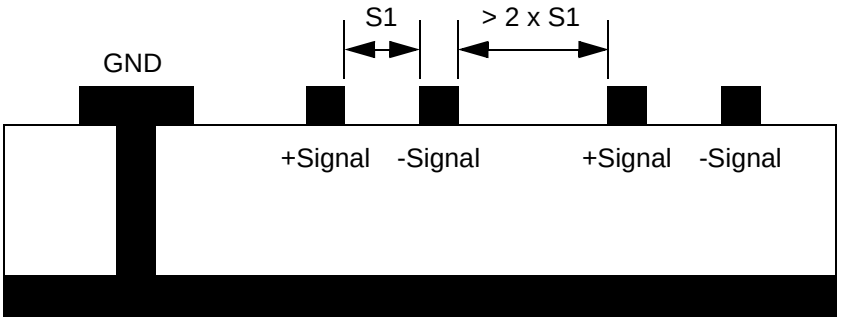
6. PCB Design Guide Line

General Guideline

- Use 4 layer PCB (minimum).
- Locate by-pass capacitors close to the device pins to a maximum extent.
- Make the loop minimum which is consist of Power line and Gnd line
- Use large Gnd plane
- Separate VDD power supply for each block via ferrite bead

LVDS Traces

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as possible.
- Avoid 90 degree bends and sharp angles.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place terminal resister close to the Receiver pins to a maximum extent.
- To plase common mode choke coil is desired for EMI reduction.



Attentions and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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