

V-by-One[®] HS Standard
Version 1.3
July. 7, 2010



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1. Introduction

1.1. Objectives

- V-by-One® HS targets a high speed data transmission of video signals based on internal connection of the equipment.
- V-by-One® HS pursues easier usage and lower power consumption compared with the current internal connection.
- V-by-One® HS supports up to 3.75Gbps data rate (effective data rate 3Gbps).
- V-by-One® HS supports scrambling and Clock Data Recovery (CDR) to reduce EMI.
- V-by-One® HS supports CDR to solve the skew problem between clock and data at conventional transfer system.

1.2. Technical Overview

With V-by-One® HS proprietary encoding scheme and CDR architecture, V-by-One® HS technology enables transmission up to 40bit video data, up to 24bit CTL data, HSYNC, VSYNC and Data Enable (DE) by some differential pair cables with minimal external components.

As shown in Figure 1, V-by-One® HS Link includes Data Lanes, Hot Plug Detect signal (HTPDN), and CDR Lock signal (LOCKN). Number of Data Lanes is decided with the pixel rate and color depth (see Table 1). HTPDN connection between transmitter and receiver can be omitted as an application option.

As optional functions, it is possible to implement transmitter pre-emphasis and receiver equalizer.

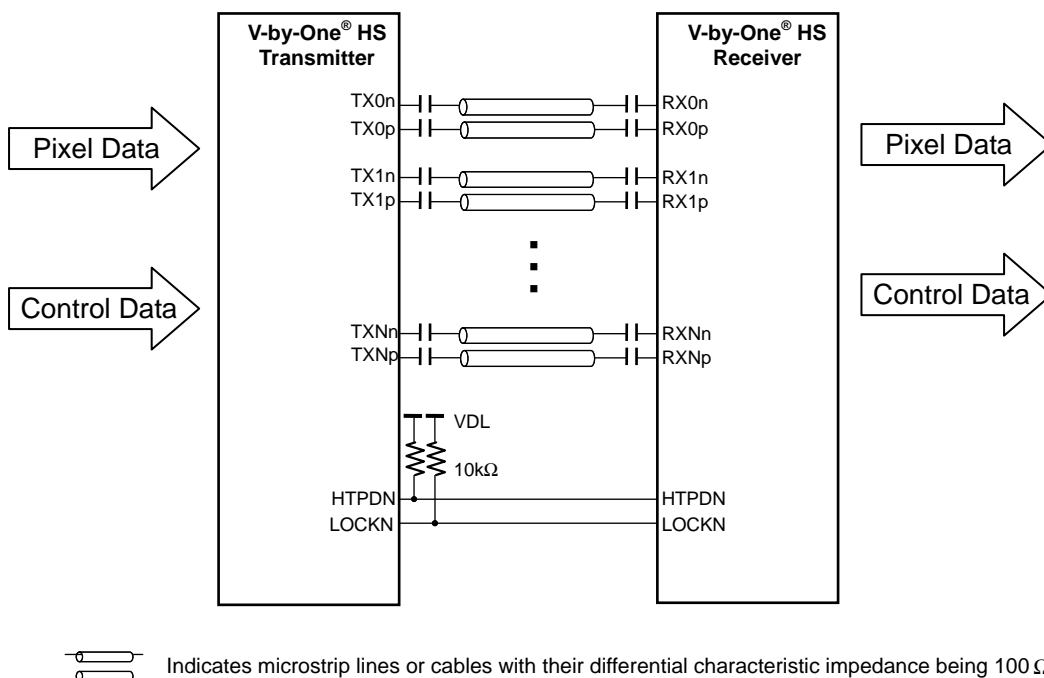


Figure 1 V-by-One® HS Link system Diagram

1.2.1. Transmitter

V-by-One® HS Transmitter consists of packer, scrambler, encoder, serializer, and transmitter link monitor (Figure 3). Transmitter link monitor constantly monitor LOCKN and HTPDN signals. If the LOCKN signal is High, Transmitter executes the CDR training. Transmitter sends the CDR training pattern on the CDR training mode. When CDR locked, Transmitter shifts from CDR training mode to the normal mode, and then it starts to transmit input data from user logic.

1.2.2. Receiver

V-by-One® HS Receiver consists of unpacker, de-scrambler, decoder, de-serializer and receiver link monitor. The Receiver synchronizes the pixel clock while referring to the CDR training pattern on the CDR training mode. After shifting from the CDR training mode to the normal mode, the Receiver aligns byte and bit position using ALN training pattern. About ALN training, please refer to 2.2.5.2 in page 25).

1.2.3. Data Lane

Data Lane is AC-coupled differential pairs with termination.

Transmission rate is able to be set up to 3.75Gbps depend on video pixel clock rate and bit depth.

1.2.3.1. Recommended data lane

Table 1 Video data format vs. No of lane example

| Resolution | Refresh rate (Pixel clock) | color depth | No of data lane* |
|------------------------------------|----------------------------|-----------------|------------------|
| HD ex. 1280 x 720p | 60Hz(74.25MHz) | 18/24/30/36 bit | 1 |
| | 120Hz(148.5MHz) | 18/24/30/36 bit | 2 |
| | 240Hz(297MHz) | 18/24/30/36 bit | 4 |
| Full HD ex. 1920 x 1080p | 60Hz(148.5MHz) | 18/24/30/36 bit | 2 |
| | 120Hz(297MHz) | 18/24/30/36 bit | 4 |
| | 240Hz(594MHz) | 18/24/30/36 bit | 8 |
| | 480Hz(1188MHz) | 18/24/30/36 bit | 16 |
| Cinema Full HD ex. 2560 x 1080p | 60Hz(185MHz) | 18/24/30 bit | 2 |
| | 120Hz(370MHz) | 18/24/30 bit | 4 |
| | 240Hz(740MHz) | 18/24/30 bit | 8 |
| 4K x 2K ex. 3840 x 2160p | 60Hz(594MHz) | 18/24/30/36 bit | 8 |
| | 120Hz(1188MHz) | 18/24/30/36 bit | 16 |
| | 240Hz(2376MHz) | 18/24/30/36 bit | 32 |

* Another lane number could be chosen; however, for the interoperability, those are STRONGLY recommended.

1.2.3.2. Data lane consideration

This chapter is informative only. It shows the procedure to select the minimum and maximum number of lanes necessary for the target application.

As a 1st step, [byte mode] (please refer to 2.1.1.4) is chosen from 3, 4, or 5 depending upon color depth. Literally 3, 4, or 5 byte mode convey nominal 3, 4, or 5byte data. For example, 10bit per color RGB image requires 30 bit data per pixel; therefore, 4 byte mode which conveys 4 byte (32 bit) is enough to carry the data.

As a 2nd step, total bit rate which is physically transmitted on V-by-One® HS line should be estimated. Because V-by-One® HS uses 8b10b encoding scheme, encoded data amount which is physically transmitted is 10bit per nominal decoded 8bit (1 byte) of original data. Multiplying [pixel clock] of the target application by encoded data amount per pixel results into [encoded total bit-rate] of V-by-One® HS transmission.

$$[\text{encoded total bit-rate}] (\text{bps}) = [\text{byte mode}] (\text{byte}) \times 8 \times \frac{10}{8} \times [\text{pixel clock}] (\text{Hz})$$

[encoded bit-rate per lane] can be calculated as [total bit rate] over [number of lanes]
[number of lanes] should be chosen properly so that [encoded bit-rate per lane] is above 600Mbps and below 3.75Gbps.

$$600\text{Mbps} \leq [\text{encoded bit-rate per lane}] (\text{bps}) = \frac{[\text{encoded total bit-rate}] (\text{bps})}{[\text{number of lanes}]} \leq 3.75\text{Gbps}$$

[number of lanes] should be selected appropriate to signal handling in applications. For example, in case of video signal transmission, [number of lanes] is recommended to be divisor of Hactive, Hblank, and Htotal pixel number like 1, 2, 4, 8, etc. in order to help signal processing.

1.2.4. HTPDN signal

HTPDN indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is High when the Receiver is not active or not connected. Then Transmitter can enter into the power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the Transmitter and the Receiver can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as Low.

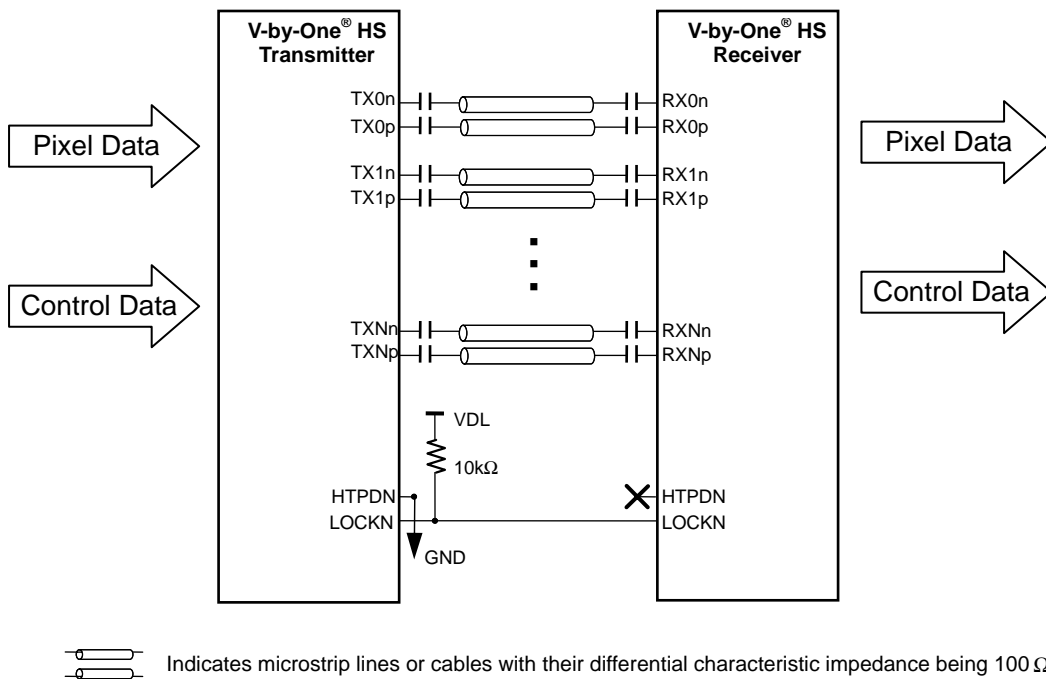


Figure 2 V-by-One® HS Link system without HTPDN connection schematic Diagram

1.2.5. LOCKN signal

LOCKN indicates whether the CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High by pull-up resistor when Receiver is not active or at the CDR PLL training state. LOCKN is set to Low by the Receiver when CDR lock is done. Then the CDR training mode finishes and Transmitter shifts to the normal mode. LOCKN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the Receiver.

4. Color Mapping and Lane Stripping

In this chapter, the color mapping for each pixel is described.

4.1. Byte length and Color mapping

The V-by-One[®] HS can be used to various types of color video format allocating D[39:0] to pixel data in packer and unpacker mapping. The color data mapping should refer to Table 11 and Table 12

Table 11 RGB/YCbCr444/RGBW/RGBY color data mapping

| Mode | | Packer input & Unpacker output | 36bpp RGB /YCbCr444 | 30bpp RGB /YCbCr444 | 24bpp RGB /YCbCr444 | 18bpp RGB /YCbCr444 | 40bpp RGBW / RGBY | 32bpp RGBW / RGBY | | |
|------------|------------|-----------------------------------|------------------------|------------------------|------------------------|------------------------|-------------------------|-------------------------|------|------|
| 5byte mode | 4byte mode | 3byte mode | Byte0 | D[0] | R/Cr[4] | R/Cr[2] | R/Cr[0] | - | R[2] | R[0] |
| | | | | D[1] | R/Cr[5] | R/Cr[3] | R/Cr[1] | - | R[3] | R[1] |
| | | | | D[2] | R/Cr[6] | R/Cr[4] | R/Cr[2] | R/Cr[0] | R[4] | R[2] |
| | | | | D[3] | R/Cr[7] | R/Cr[5] | R/Cr[3] | R/Cr[1] | R[5] | R[3] |
| | | | | D[4] | R/Cr[8] | R/Cr[6] | R/Cr[4] | R/Cr[2] | R[6] | R[4] |
| | | | | D[5] | R/Cr[9] | R/Cr[7] | R/Cr[5] | R/Cr[3] | R[7] | R[5] |
| | | | | D[6] | R/Cr[10] | R/Cr[8] | R/Cr[6] | R/Cr[4] | R[8] | R[6] |
| | | D[7] | R/Cr[11] | R/Cr[9] | R/Cr[7] | R/Cr[5] | R[9] | R[7] | | |
| | | Byte1 | D[8] | G/Y[4] | G/Y[2] | G/Y[0] | - | G[2] | G[0] | |
| | | | D[9] | G/Y[5] | G/Y[3] | G/Y[1] | - | G[3] | G[1] | |
| | | | D[10] | G/Y[6] | G/Y[4] | G/Y[2] | G/Y[0] | G[4] | G[2] | |
| | | | D[11] | G/Y[7] | G/Y[5] | G/Y[3] | G/Y[1] | G[5] | G[3] | |
| | | | D[12] | G/Y[8] | G/Y[6] | G/Y[4] | G/Y[2] | G[6] | G[4] | |
| | | | D[13] | G/Y[9] | G/Y[7] | G/Y[5] | G/Y[3] | G[7] | G[5] | |
| | | | D[14] | G/Y[10] | G/Y[8] | G/Y[6] | G/Y[4] | G[8] | G[6] | |
| | | D[15] | G/Y[11] | G/Y[9] | G/Y[7] | G/Y[5] | G[9] | G[7] | | |
| | | Byte2 | D[16] | B/Cb[4] | B/Cb[2] | B/Cb[0] | - | B[2] | B[0] | |
| | | | D[17] | B/Cb[5] | B/Cb[3] | B/Cb[1] | - | B[3] | B[1] | |
| | | | D[18] | B/Cb[6] | B/Cb[4] | B/Cb[2] | B/Cb[0] | B[4] | B[2] | |
| | | | D[19] | B/Cb[7] | B/Cb[5] | B/Cb[3] | B/Cb[1] | B[5] | B[3] | |
| | | | D[20] | B/Cb[8] | B/Cb[6] | B/Cb[4] | B/Cb[2] | B[6] | B[4] | |
| | D[21] | | B/Cb[9] | B/Cb[7] | B/Cb[5] | B/Cb[3] | B[7] | B[5] | | |
| | D[22] | | B/Cb[10] | B/Cb[8] | B/Cb[6] | B/Cb[4] | B[8] | B[6] | | |
| | D[23] | B/Cb[11] | B/Cb[9] | B/Cb[7] | B/Cb[5] | B[9] | B[7] | | | |
| | Byte3 | D[24] | (3DLR*) | (3DLR*) | - | - | R[0] | - | | |
| | | D[25] | (3DEN*) | (3DEN*) | - | - | R[1] | - | | |
| | | D[26] | B/Cb[2] | B/Cb[0] | - | - | G[0] | - | | |
| | | D[27] | B/Cb[3] | B/Cb[1] | - | - | G[1] | - | | |
| | | D[28] | G/Y[2] | G/Y[0] | - | - | B[0] | - | | |
| | | D[29] | G/Y[3] | G/Y[1] | - | - | B[1] | - | | |
| | | D[30] | R/Cr[2] | R/Cr[0] | - | - | W/Y[0] | - | | |
| | D[31] | R/Cr[3] | R/Cr[1] | - | - | W/Y[1] | - | | | |
| | Byte4 | D[32] | - | - | - | - | W/Y[2] | W/Y[0] | | |
| | | D[33] | - | - | - | - | W/Y[3] | W/Y[1] | | |
| | | D[34] | B/Cb[0] | - | - | - | W/Y[4] | W/Y[2] | | |
| | | D[35] | B/Cb[1] | - | - | - | W/Y[5] | W/Y[3] | | |
| | | D[36] | G/Y[0] | - | - | - | W/Y[6] | W/Y[4] | | |
| | | D[37] | G/Y[1] | - | - | - | W/Y[7] | W/Y[5] | | |
| | | D[38] | R/Cr[0] | - | - | - | W/Y[8] | W/Y[6] | | |
| D[39] | R/Cr[1] | - | - | - | W/Y[9] | W/Y[7] | | | | |

* Implementation specific

Table 12 YCbCr422 color data mapping

| Mode | | Packer input & Unpacker output | 32bpp YCbCr422 | 24bpp YCbCr422 | 20bpp YCbCr422 | 16bpp YCbCr422 | | |
|------------|------------|--------------------------------|----------------|----------------|----------------|----------------|----------|----------|
| 5byte mode | 4byte mode | 3byte mode | Byte0 | D[0] | Cb/Cr[8] | Cb/Cr[4] | Cb/Cr[2] | Cb/Cr[0] |
| | | | | D[1] | Cb/Cr[9] | Cb/Cr[5] | Cb/Cr[3] | Cb/Cr[1] |
| | | | | D[2] | Cb/Cr[10] | Cb/Cr[6] | Cb/Cr[4] | Cb/Cr[2] |
| | | | | D[3] | Cb/Cr[11] | Cb/Cr[7] | Cb/Cr[5] | Cb/Cr[3] |
| | | | | D[4] | Cb/Cr[12] | Cb/Cr[8] | Cb/Cr[6] | Cb/Cr[4] |
| | | | | D[5] | Cb/Cr[13] | Cb/Cr[9] | Cb/Cr[7] | Cb/Cr[5] |
| | | | | D[6] | Cb/Cr[14] | Cb/Cr[10] | Cb/Cr[8] | Cb/Cr[6] |
| | | | | D[7] | Cb/Cr[15] | Cb/Cr[11] | Cb/Cr[9] | Cb/Cr[7] |
| | | Byte1 | D[8] | Y[8] | Y[4] | Y[2] | Y[0] | |
| | | | D[9] | Y[9] | Y[5] | Y[3] | Y[1] | |
| | | | D[10] | Y[10] | Y[6] | Y[4] | Y[2] | |
| | | | D[11] | Y[11] | Y[7] | Y[5] | Y[3] | |
| | | | D[12] | Y[12] | Y[8] | Y[6] | Y[4] | |
| | | | D[13] | Y[13] | Y[9] | Y[7] | Y[5] | |
| | | | D[14] | Y[14] | Y[10] | Y[8] | Y[6] | |
| | | | D[15] | Y[15] | Y[11] | Y[9] | Y[7] | |
| | | Byte2 | D[16] | - | - | - | - | |
| | | | D[17] | - | - | - | - | |
| | | | D[18] | - | - | - | - | |
| | | | D[19] | - | - | - | - | |
| | | | D[20] | - | - | - | - | |
| | | | D[21] | - | - | - | - | |
| | | | D[22] | - | - | - | - | |
| | | | D[23] | - | - | - | - | |
| | | Byte3 | D[24] | Y[2] | - | - | - | |
| | | | D[25] | Y[3] | - | - | - | |
| | | | D[26] | Cb/Cr[2] | - | - | - | |
| | | | D[27] | Cb/Cr[3] | - | - | - | |
| | D[28] | | Y[6] | Y[2] | Y[0] | - | | |
| | D[29] | | Y[7] | Y[3] | Y[1] | - | | |
| | D[30] | | Cb/Cr[6] | Cb/Cr[2] | Cb/Cr[0] | - | | |
| | D[31] | | Cb/Cr[7] | Cb/Cr[3] | Cb/Cr[1] | - | | |
| | Byte4 | D[32] | Y[0] | - | - | - | | |
| | | D[33] | Y[1] | - | - | - | | |
| | | D[34] | Cb/Cr[0] | - | - | - | | |
| | | D[35] | Cb/Cr[1] | - | - | - | | |
| | | D[36] | Y[4] | Y[0] | - | - | | |
| | | D[37] | Y[5] | Y[1] | - | - | | |
| | | D[38] | Cb/Cr[4] | Cb/Cr[0] | - | - | | |
| | | D[39] | Cb/Cr[5] | Cb/Cr[1] | - | - | | |

4.2. Multiple Data Lane combination

4.2.1. Allocation of pixel to Data Lane

Depend on the data rate and pixel color depth, it is permitted to increase the Data Lanes. About the multiple Data Lanes combination, Refers to Figure 27.

The V-by-One® HS compliant components must be implemented with at least one Data Lane. If the data rate of the required color depth and timing is higher than the components maximum supported data rate, additional Data Lane can be used. (The maximum data rate of V-by-One® HS Data Lane is 3.75Gbps per lane and the minimum is 600Mbps.) In this case, total lane count should be even number, under the condition of the fewer lane number.

The pixel number for the horizontal active and blanking term (Hactive, Hblank) should be adjusted to become the multiple number of the lane count.

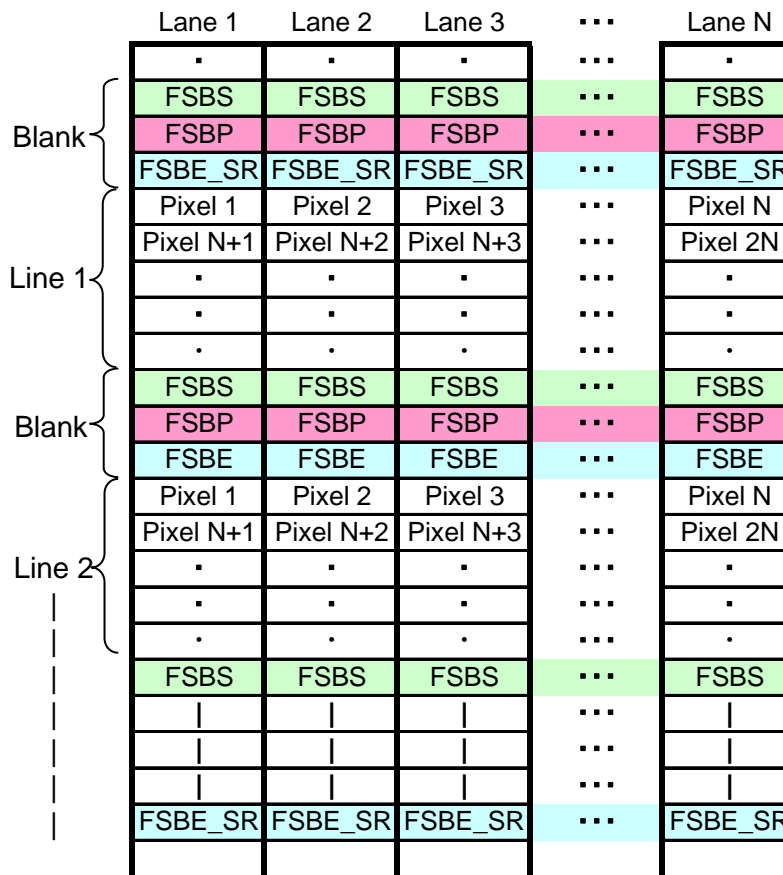


Figure 27 Allocation of pixel to Data Lane

For the DTV application, Data Lane number in Table 1 is STRONGLY recommended for interoperability.

4.2.2. Inter-lane skewing

Allowable Inter-lane skew is defined as tRISK. Refer to Section 3.3.

V-by-One[®] HS Transmitter is not required to make any intentional inter-lane skew between lanes.

4.2.3. RGB+CMY color mode

If the Transmitter and the Receiver adopt the RGB+CMY (6 color mode) transmission, twice of the lanes are used for the RGB and CMY. In the CMY lanes, the positions of the C data, M data, and Y data are mapped at the positions of the R data, G data, and B data in the Table 11, respectively.

4.3. 3D frame identification

3D display may have identification on every frame. Methods to label 3D information on frame are described. The description of 3D data allocation in this chapter is informative. Actual application may be different. 2 possible alternatives are introduced in this chapter; however, to apply both methods at the same time is not recommended. Users have to choose one explicit method for their application.

4.3.1. 3D flag on blanking period

Packer and Unpacker data mapping in Table 2 and Table 3 show that there is a potential to send arbitrary data on V-by-One® HS during blanking period. One way to carry 3D information is to make use of CTL data mapping.

4.3.1.1. CTL data allocation to 3D flag

It is suggested that CTL<0> and CTL<1> be used for 3D signaling. These signals correspond to CTL<1:0> in Table 2 and Table 3.

- CTL<0> = Left/Right Indicator
- CTL<0> = high (1) → the next frame is the Left View
- CTL<0> = low (0) → the next frame is the Right View

- CTL<1> = 3D Mode Enable
- CTL<1> = high (1) → 3D video is being transmitted
- CTL<1> = low (0) → 2D video is being transmitted

4.3.1.2. CTL data timing of 3D flag

CTL<1:0> should update on the first pixel of the FSBP in the Vertical Blanking Period and remain constant for the remainder of the FSBP in the Vertical Blanking Period. CTL<1:0> should only update during the Vertical Blanking period. The first pixel of the FSBP is recommended to be used for processing.

Use of CTL<1:0> is implementation specific. In one case, it may apply to the active video that immediately follows the Vertical Blanking Period. In other applications it may apply to a later frame.

4.3.2. 3D flag on DE active period

The color data mapping in Table 11 and Table 12 show that there are unused bits depending on the colors and byte mode used. It is possible (and allowable) to make use of these unused bits to carry the 3D information.

4.3.2.1. Color data mapping allocation to 3D flag

3D information can be conveyed using the 3DLR and 3DEN bits in Table 11. The 30bpp RGB/CrYCb 4 byte mode and 36bpp RGB/CrYCb 5 byte of Table 11 show the recommended placement of these controls.

3DLR = Left/Right Indicator

3DLR = high (1) → the next frame is the Left View

3DLR = low (0) → the next frame is the Right View

3DEN = 3D Mode Enable

3DEN = high (1) → 3D video is being transmitted

3DEN = low (0) → 2D video is being transmitted

4.3.2.2. Color data mapping timing of 3D flag

3DLR and 3DEN of the first pixel in particular frame is recommended to be used for processing.

Use of 3DLR and 3DEN is implementation specific. In one case, it may apply to the current frame. In other applications it may apply to a later frame.

5. Connector and Cable

This chapter shows the guideline of the connector and the cable to connect the V-by-One® HS Transmitter (ex. video processing unit) and Receiver (ex. Panel module).

For interoperability, the following points are recommended to be paid attention to.

- Pin assignment for “V-by-One HS CML lanes”, HTPDN/LOCKN, and “CML Ground” should be fixed.
- Pins originally assigned to power supply are not supposed to be GND nor signal to devices.
- Pins originally assigned to Ground are not supposed to be power supply.
- Not all but several “Ground” pins beside power supply pins can be turned into user option pins.
- If more option or other power pins are required, use large number connector. (Please refer to chapter5.2)

5.1. Pin assignments

5.1.1. 1 lane connection (HD@60Hz)

Table 13 1 lane Connector Pin Assignment

| Tx | | Description | Rx | |
|---------|--------|------------------------------|--------|--------|
| Pin No. | Symbol | | Symbol | Pin No |
| 11 | Vcc | Supply voltage for module | Vcc | 1 |
| 10 | Vcc | Supply voltage for module | Vcc | 2 |
| 9 | Vcc | Supply voltage for module | Vcc | 3 |
| 8 | GND | Ground* | GND | 4 |
| 7 | GND | Ground* | GND | 5 |
| 6 | HTPDN | Hot plug detect | HTPDN | 6 |
| 5 | LOCKN | Lock detect | LOCKN | 7 |
| 4 | GND | CML Ground | GND | 8 |
| 3 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 9 |
| 2 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 10 |
| 1 | GND | CML Ground | GND | 11 |

* Not all but several “Ground” pins beside power supply pins can be turned into user option pins if needed.

5.1.2. 2 lane connection (HD@120Hz and F-HD@60Hz)

Table 14 2 Lane Connector Pin Assignment

| Tx | | Description | Rx | |
|---------|----------|------------------------------|----------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 21 | Vcc | Supply voltage for module | Vcc | 1 |
| 20 | Vcc | Supply voltage for module | Vcc | 2 |
| 19 | Vcc | Supply voltage for module | Vcc | 3 |
| 18 | Vcc | Supply voltage for module | Vcc | 4 |
| 17 | Vcc | Supply voltage for module | Vcc | 5 |
| 16 | GND | Ground* | GND | 6 |
| 15 | GND | Ground* | GND | 7 |
| 14 | GND | Ground* | GND | 8 |
| 13 | GND | Ground* | GND | 9 |
| 12 | HTPDN | Hot plug detect | HTPDN | 10 |
| 11 | LOCKN | Lock detect | LOCKN | 11 |
| 10 | GND | CML Ground | GND | 12 |
| 9 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 13 |
| 8 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 14 |
| 7 | GND | CML Ground | GND | 15 |
| 6 | GND | CML Ground | GND | 16 |
| 5 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 17 |
| 4 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 18 |
| 3 | GND | CML Ground | GND | 19 |
| 2 | (Option) | (User option) | (Option) | 20 |
| 1 | (Option) | (User option) | (Option) | 21 |

* Not all but several “Ground” pins beside power supply pins can be turned into user option pins if needed.

5.1.3. 4 lane connection (HD@240Hz and F-HD@120Hz)

Table 15 4 Lane Connector Pin Assignment (w/o Power Supply)

| Tx | | Description | Rx | |
|---------|----------|------------------------------|----------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 21 | GND | Ground* | GND | 1 |
| 20 | HTPDN | Hot plug detect | HTPDN | 2 |
| 19 | LOCKN | Lock detect | LOCKN | 3 |
| 18 | GND | CML Ground | GND | 4 |
| 17 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 5 |
| 16 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 6 |
| 15 | GND | CML Ground | GND | 7 |
| 14 | GND | CML Ground | GND | 8 |
| 13 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 9 |
| 12 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 10 |
| 11 | GND | CML Ground | GND | 11 |
| 10 | GND | CML Ground | GND | 12 |
| 9 | Tx2n | V-by-One HS Data Lane2 (CML) | Rx2n | 13 |
| 8 | Tx2p | V-by-One HS Data Lane2 (CML) | Rx2p | 14 |
| 7 | GND | CML Ground | GND | 15 |
| 6 | GND | CML Ground | GND | 16 |
| 5 | Tx3n | V-by-One HS Data Lane3 (CML) | Rx3n | 17 |
| 4 | Tx3p | V-by-One HS Data Lane3 (CML) | Rx3p | 18 |
| 3 | GND | CML Ground | GND | 19 |
| 2 | (Option) | (User option) | (Option) | 20 |
| 1 | (Option) | (User option) | (Option) | 21 |

* Not all but several "Ground" pins can be turned into user option pins if needed.

Table 16 4 Lane Connector Pin Assignment

| Tx | | Description | Rx | |
|---------|----------|------------------------------|----------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 31 | Vcc | Supply voltage for module | Vcc | 1 |
| 30 | Vcc | Supply voltage for module | Vcc | 2 |
| 29 | Vcc | Supply voltage for module | Vcc | 3 |
| 28 | Vcc | Supply voltage for module | Vcc | 4 |
| 27 | Vcc | Supply voltage for module | Vcc | 5 |
| 26 | Vcc | Supply voltage for module | Vcc | 6 |
| 25 | Vcc | Supply voltage for module | Vcc | 7 |
| 24 | GND | Ground* | GND | 8 |
| 23 | GND | Ground* | GND | 9 |
| 22 | GND | Ground* | GND | 10 |
| 21 | GND | Ground* | GND | 11 |
| 20 | HTPDN | Hot plug detect | HTPDN | 12 |
| 19 | LOCKN | Lock detect | LOCKN | 13 |
| 18 | GND | CML Ground | GND | 14 |
| 17 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 15 |
| 16 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 16 |
| 15 | GND | CML Ground | GND | 17 |
| 14 | GND | CML Ground | GND | 18 |
| 13 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 19 |
| 12 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 20 |
| 11 | GND | CML Ground | GND | 21 |
| 10 | GND | CML Ground | GND | 22 |
| 9 | Tx2n | V-by-One HS Data Lane2 (CML) | Rx2n | 23 |
| 8 | Tx2p | V-by-One HS Data Lane2 (CML) | Rx2p | 24 |
| 7 | GND | CML Ground | GND | 25 |
| 6 | GND | CML Ground | GND | 26 |
| 5 | Tx3n | V-by-One HS Data Lane3 (CML) | Rx3n | 27 |
| 4 | Tx3p | V-by-One HS Data Lane3 (CML) | Rx3p | 28 |
| 3 | GND | CML Ground | GND | 29 |
| 2 | (Option) | (User option) | (Option) | 30 |
| 1 | (Option) | (User option) | (Option) | 31 |

* Not all but several "Ground" pins beside power supply pins can be turned into user option pins if needed.

5.1.4. 8 lane connection (F-HD@240Hz and 4Kx2K@60Hz)

Table 17 8 Lane Connector Pin Assignment (w/o Power Supply)

| Tx | | Description | Rx | |
|---------|----------|------------------------------|----------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 41 | GND | Ground* | GND | 1 |
| 40 | GND | Ground* | GND | 2 |
| 39 | GND | Ground* | GND | 3 |
| 38 | GND | Ground* | GND | 4 |
| 37 | GND | Ground* | GND | 5 |
| 36 | HTPDN | Hot plug detect | HTPDN | 6 |
| 35 | LOCKN | Lock detect | LOCKN | 7 |
| 34 | GND | CML Ground | GND | 8 |
| 33 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 9 |
| 32 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 10 |
| 31 | GND | CML Ground | GND | 11 |
| 30 | GND | CML Ground | GND | 12 |
| 29 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 13 |
| 28 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 14 |
| 27 | GND | CML Ground | GND | 15 |
| 26 | GND | CML Ground | GND | 16 |
| 25 | Tx2n | V-by-One HS Data Lane2 (CML) | Rx2n | 17 |
| 24 | Tx2p | V-by-One HS Data Lane2 (CML) | Rx2p | 18 |
| 23 | GND | CML Ground | GND | 19 |
| 22 | GND | CML Ground | GND | 20 |
| 21 | Tx3n | V-by-One HS Data Lane3 (CML) | Rx3n | 21 |
| 20 | Tx3p | V-by-One HS Data Lane3 (CML) | Rx3p | 22 |
| 19 | GND | CML Ground | GND | 23 |
| 18 | GND | CML Ground | GND | 24 |
| 17 | Tx4n | V-by-One HS Data Lane4 (CML) | Rx4n | 25 |
| 16 | Tx4p | V-by-One HS Data Lane4 (CML) | Rx4p | 26 |
| 15 | GND | CML Ground | GND | 27 |
| 14 | GND | CML Ground | GND | 28 |
| 13 | Tx5n | V-by-One HS Data Lane5 (CML) | Rx5n | 29 |
| 12 | Tx5p | V-by-One HS Data Lane5 (CML) | Rx5p | 30 |
| 11 | GND | CML Ground | GND | 31 |
| 10 | GND | CML Ground | GND | 32 |
| 9 | Tx6n | V-by-One HS Data Lane6(CML) | Rx6n | 33 |
| 8 | Tx6p | V-by-One HS Data Lane6(CML) | Rx6p | 34 |
| 7 | GND | CML Ground | GND | 35 |
| 6 | GND | CML Ground | GND | 36 |
| 5 | Tx7n | V-by-One HS Data Lane7(CML) | Rx7n | 37 |
| 4 | Tx7p | V-by-One HS Data Lane7(CML) | Rx7p | 38 |
| 3 | GND | CML Ground | GND | 39 |
| 2 | (Option) | (User option) | (Option) | 40 |
| 1 | (Option) | (User option) | (Option) | 41 |

* Not all but several "Ground" pins can be turned into user option pins if needed.

Table 18 8 Lane Connector Pin Assignment

| Tx | | Description | Rx | |
|---------|----------|------------------------------|----------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 51 | Vcc | Supply voltage for module | Vcc | 1 |
| 50 | Vcc | Supply voltage for module | Vcc | 2 |
| 49 | Vcc | Supply voltage for module | Vcc | 3 |
| 48 | Vcc | Supply voltage for module | Vcc | 4 |
| 47 | Vcc | Supply voltage for module | Vcc | 5 |
| 46 | Vcc | Supply voltage for module | Vcc | 6 |
| 45 | Vcc | Supply voltage for module | Vcc | 7 |
| 44 | Vcc | Supply voltage for module | Vcc | 8 |
| 43 | Vcc | Supply voltage for module | Vcc | 9 |
| 42 | Vcc | Supply voltage for module | Vcc | 10 |
| 41 | GND | Ground* | GND | 11 |
| 40 | GND | Ground* | GND | 12 |
| 39 | GND | Ground* | GND | 13 |
| 38 | GND | Ground* | GND | 14 |
| 37 | GND | Ground* | GND | 15 |
| 36 | HTPDN | Hot plug detect | HTPDN | 16 |
| 35 | LOCKN | Lock detect | LOCKN | 17 |
| 34 | GND | CML Ground | GND | 18 |
| 33 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 19 |
| 32 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 20 |
| 31 | GND | CML Ground | GND | 21 |
| 30 | GND | CML Ground | GND | 22 |
| 29 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 23 |
| 28 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 24 |
| 27 | GND | CML Ground | GND | 25 |
| 26 | GND | CML Ground | GND | 26 |
| 25 | Tx2n | V-by-One HS Data Lane2 (CML) | Rx2n | 27 |
| 24 | Tx2p | V-by-One HS Data Lane2 (CML) | Rx2p | 28 |
| 23 | GND | CML Ground | GND | 29 |
| 22 | GND | CML Ground | GND | 30 |
| 21 | Tx3n | V-by-One HS Data Lane3 (CML) | Rx3n | 31 |
| 20 | Tx3p | V-by-One HS Data Lane3 (CML) | Rx3p | 32 |
| 19 | GND | CML Ground | GND | 33 |
| 18 | GND | CML Ground | GND | 34 |
| 17 | Tx4n | V-by-One HS Data Lane4 (CML) | Rx4n | 35 |
| 16 | Tx4p | V-by-One HS Data Lane4 (CML) | Rx4p | 36 |
| 15 | GND | CML Ground | GND | 37 |
| 14 | GND | CML Ground | GND | 38 |
| 13 | Tx5n | V-by-One HS Data Lane5 (CML) | Rx5n | 39 |
| 12 | Tx5p | V-by-One HS Data Lane5 (CML) | Rx5p | 40 |
| 11 | GND | CML Ground | GND | 41 |
| 10 | GND | CML Ground | GND | 42 |
| 9 | Tx6n | V-by-One HS Data Lane6 (CML) | Rx6n | 43 |
| 8 | Tx6p | V-by-One HS Data Lane6 (CML) | Rx6p | 44 |
| 7 | GND | CML Ground | GND | 45 |
| 6 | GND | CML Ground | GND | 46 |
| 5 | Tx7n | V-by-One HS Data Lane7 (CML) | Rx7n | 47 |
| 4 | Tx7p | V-by-One HS Data Lane7 (CML) | Rx7p | 48 |
| 3 | GND | CML Ground | GND | 49 |
| 2 | (Option) | (User option) | (Option) | 50 |
| 1 | (Option) | (User option) | (Option) | 51 |

* Not all but several “Ground” pins beside power supply pins can be turned into user option pins if needed.

5.1.5. 16 Lane connection (F-HD@480Hz and 4Kx2K@120Hz)

This connection could also be configured with the combination of two 8-Lane connectors.

Table 19 16 Lane Connector Pin Assignment

| Tx | | Description | Rx | |
|---------|--------|------------------------------|--------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 80 | Vcc | Supply voltage for module | Vcc | 1 |
| 79 | Vcc | Supply voltage for module | Vcc | 2 |
| 78 | Vcc | Supply voltage for module | Vcc | 3 |
| 77 | Vcc | Supply voltage for module | Vcc | 4 |
| 76 | Vcc | Supply voltage for module | Vcc | 5 |
| 75 | Vcc | Supply voltage for module | Vcc | 6 |
| 74 | Vcc | Supply voltage for module | Vcc | 7 |
| 73 | Vcc | Supply voltage for module | Vcc | 8 |
| 72 | Vcc | Supply voltage for module | Vcc | 9 |
| 71 | Vcc | Supply voltage for module | Vcc | 10 |
| 70 | GND | Ground* | GND | 11 |
| 69 | GND | Ground* | GND | 12 |
| 68 | GND | Ground* | GND | 13 |
| 67 | GND | Ground* | GND | 14 |
| 66 | HTPDN | Hot plug detect | HTPDN | 15 |
| 65 | LOCKN | Lock detect | LOCKN | 16 |
| 64 | GND | CML Ground | GND | 17 |
| 63 | Tx0n | V-by-One HS Data Lane0 (CML) | Rx0n | 18 |
| 62 | Tx0p | V-by-One HS Data Lane0 (CML) | Rx0p | 19 |
| 61 | GND | CML Ground | GND | 20 |
| 60 | GND | CML Ground | GND | 21 |
| 59 | Tx1n | V-by-One HS Data Lane1 (CML) | Rx1n | 22 |
| 58 | Tx1p | V-by-One HS Data Lane1 (CML) | Rx1p | 23 |
| 57 | GND | CML Ground | GND | 24 |
| 56 | GND | CML Ground | GND | 25 |
| 55 | Tx2n | V-by-One HS Data Lane2 (CML) | Rx2n | 26 |
| 54 | Tx2p | V-by-One HS Data Lane2 (CML) | Rx2p | 27 |
| 53 | GND | CML Ground | GND | 28 |
| 52 | GND | CML Ground | GND | 29 |
| 51 | Tx3n | V-by-One HS Data Lane3 (CML) | Rx3n | 30 |
| 50 | Tx3p | V-by-One HS Data Lane3 (CML) | Rx3p | 31 |
| 49 | GND | CML Ground | GND | 32 |
| 48 | GND | CML Ground | GND | 33 |
| 47 | Tx4n | V-by-One HS Data Lane4 (CML) | Rx4n | 34 |
| 46 | Tx4p | V-by-One HS Data Lane4 (CML) | Rx4p | 35 |
| 45 | GND | CML Ground | GND | 36 |
| 44 | GND | CML Ground | GND | 37 |
| 43 | Tx5n | V-by-One HS Data Lane5 (CML) | Rx5n | 38 |
| 42 | Tx5p | V-by-One HS Data Lane5 (CML) | Rx5p | 39 |
| 41 | GND | CML Ground | GND | 40 |
| 40 | GND | CML Ground | GND | 41 |
| 39 | Tx6n | V-by-One HS Data Lane6 (CML) | Rx6n | 42 |
| 38 | Tx6p | V-by-One HS Data Lane6 (CML) | Rx6p | 43 |
| 37 | GND | CML Ground | GND | 44 |
| 36 | GND | CML Ground | GND | 45 |

* Not all but several "Ground" pins beside power supply pins can be turned into user option pins if needed.

(Continued)

| Tx | | Description | Rx | |
|---------|--------|-------------------------------|--------|---------|
| Pin No. | Symbol | | Symbol | Pin No. |
| 35 | Tx7n | V-by-One HS Data Lane7 (CML) | Rx7n | 46 |
| 34 | Tx7p | V-by-One HS Data Lane7 (CML) | Rx7p | 47 |
| 33 | GND | CML Ground | GND | 48 |
| 32 | GND | CML Ground | GND | 49 |
| 31 | Tx8n | V-by-One HS Data Lane8 (CML) | Rx8n | 50 |
| 30 | Tx8p | V-by-One HS Data Lane8 (CML) | Rx8p | 51 |
| 29 | GND | CML Ground | GND | 52 |
| 28 | GND | CML Ground | GND | 53 |
| 27 | Tx9n | V-by-One HS Data Lane9 (CML) | Rx9n | 54 |
| 26 | Tx9p | V-by-One HS Data Lane9 (CML) | Rx9p | 55 |
| 25 | GND | CML Ground | GND | 56 |
| 24 | GND | CML Ground | GND | 57 |
| 23 | Tx10n | V-by-One HS Data Lane10 (CML) | Rx10n | 58 |
| 22 | Tx10p | V-by-One HS Data Lane10 (CML) | Rx10p | 59 |
| 21 | GND | CML Ground | GND | 60 |
| 20 | GND | CML Ground | GND | 61 |
| 19 | Tx11n | V-by-One HS Data Lane11 (CML) | Rx11n | 62 |
| 18 | Tx11p | V-by-One HS Data Lane11 (CML) | Rx11p | 63 |
| 17 | GND | CML Ground | GND | 64 |
| 16 | GND | CML Ground | GND | 65 |
| 15 | Tx12n | V-by-One HS Data Lane12 (CML) | Rx12n | 66 |
| 14 | Tx12p | V-by-One HS Data Lane12 (CML) | Rx12p | 67 |
| 13 | GND | CML Ground | GND | 68 |
| 12 | GND | CML Ground | GND | 69 |
| 11 | Tx13n | V-by-One HS Data Lane13 (CML) | Rx13n | 70 |
| 10 | Tx13p | V-by-One HS Data Lane13 (CML) | Rx13p | 71 |
| 9 | GND | CML Ground | GND | 72 |
| 8 | GND | CML Ground | GND | 73 |
| 7 | Tx14n | V-by-One HS Data Lane14 (CML) | Rx14n | 74 |
| 6 | Tx14p | V-by-One HS Data Lane14 (CML) | Rx14p | 75 |
| 5 | GND | CML Ground | GND | 76 |
| 4 | GND | CML Ground | GND | 77 |
| 3 | Tx15n | V-by-One HS Data Lane15 (CML) | Rx15n | 78 |
| 2 | Tx15p | V-by-One HS Data Lane15 (CML) | Rx15p | 79 |
| 1 | GND | CML Ground | GND | 80 |

* Not all but several "Ground" pins beside power supply pins can be turned into user option pins if needed.

5.1.6. 32 Lane connection (4Kx2K@240Hz)

This connection is configured with the combination of four 8-Lane connectors.

Note:

Some cable like Flexible Printed Circuits (FPC) does not have the symmetric conductor layout. This means that if users connect the cable at reverse direction, i.e. Rx plug is connected to Transmitter's receptacle and Tx plug to Receiver's receptacle, the correct connection cannot be achieved. Users must take care with the cable direction.

5.2. Option pins

Basically, users can use the "(User Option)" pins freely.

Not all but several "Ground" pins beside power supply pins can be turned into user option pins, if needed.

If more option pins or another power supply are required, use large number connector and follow the below.

- Basic pin assignment whose is for V-by-One HS lanes with power supply should be copied
- Pin of Transmitter side Pin No."MAX" and Receiver side Pin No.1 should be copied supply pin.
- Basic pin assignment should be applied to large number connector stuffed from the above supply pin.
- Remainder pins of large number connector can be used as user option.

Table 20 Example of 8 lane Pin Assignment with Expanded Option Pins for 68 Pins Connector

| Tx | | Description | Rx | |
|---------|----------|-----------------------------------|----------|--------|
| Pin No. | Symbol | | Symbol | Pin No |
| 68 | Vcc | Supply voltage for module | Vcc | 1 |
| 67 | Vcc | Supply voltage for module | Vcc | 2 |
| 66-23 | - | (same pin assignment as Table 18) | - | 3-46 |
| 22 | Tx7n | V-by-One HS Data Lane7 (CML) | Rx7n | 47 |
| 21 | Tx7p | V-by-One HS Data Lane7 (CML) | Rx7p | 48 |
| 20 | GND | CML Ground | GND | 49 |
| 19 | (Option) | (User option) | (Option) | 50 |
| 18 | (Option) | (User option) | (Option) | 51 |
| 17 | (Option) | (User option) | (Option) | 52 |
| 16 | (Option) | (User option) | (Option) | 53 |
| 15-3 | (Option) | (User option) | (Option) | 54-66 |
| 2 | (Option) | (User option) | (Option) | 67 |
| 1 | (Option) | (User option) | (Option) | 68 |

5.3. Connector Characteristics

5.3.1. Electrical

- Operating Current : 0.5A per pin minimum
- Operating Voltage : 150VAC rms, maximum
- Voltage proof : 200 VAC for minimum of 1 minute

5.3.2. Recommended Receptacle Interface Dimensions

0.5mm signal terminal pitch connector is recommended for interoperability.

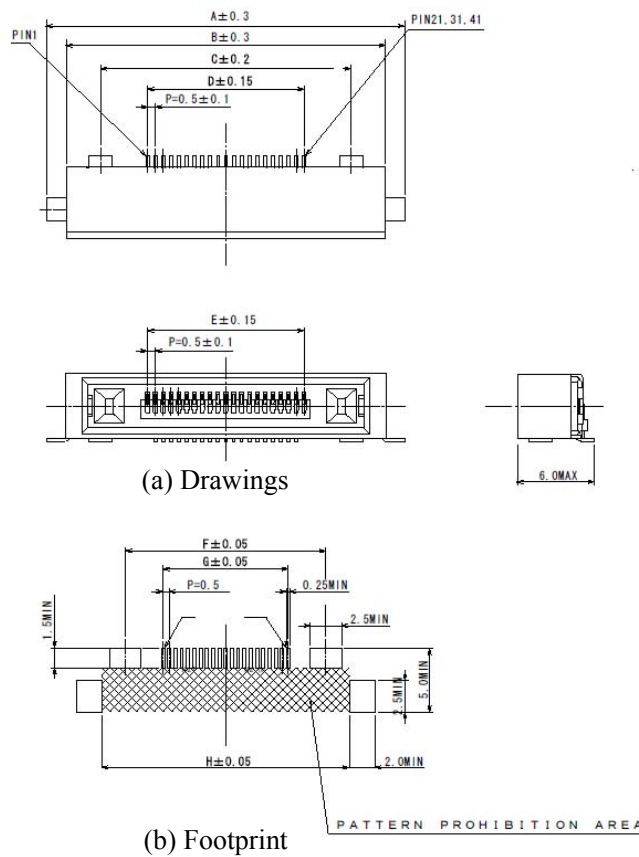


Figure 28 PCB Mount Receptacle drawings (recommended)

Table 21 Form Factor of Receptacle

| No. of CONTACT | A | B | C | D | E | F | G | H |
|----------------|-------|-------|----|----|----|----|----|-------|
| 21 | 22.85 | 20.46 | 16 | 10 | 10 | 16 | 10 | 19.75 |
| 31 | 27.85 | 25.46 | 21 | 15 | 15 | 21 | 15 | 24.75 |
| 41 | 32.85 | 30.46 | 26 | 20 | 20 | 26 | 20 | 29.75 |
| 51 | 37.85 | 35.46 | 31 | 25 | 25 | 31 | 25 | 34.75 |

5.4. PCB Layout Considerations

Use at least 4-layer PCB with signals, GND, power, and signals assigned for each layer. (Refer to figure below.)

PCB traces for the high-speed signals must be single-ended microstrip lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.

Minimize the distance between traces of a differential pair (S1 of Figure 29) to maximize common mode rejection and coupling effect which works to reduce Electro-Magnetic Interference (EMI).

Route differential signal traces symmetrically.

Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity. Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed Lanes.

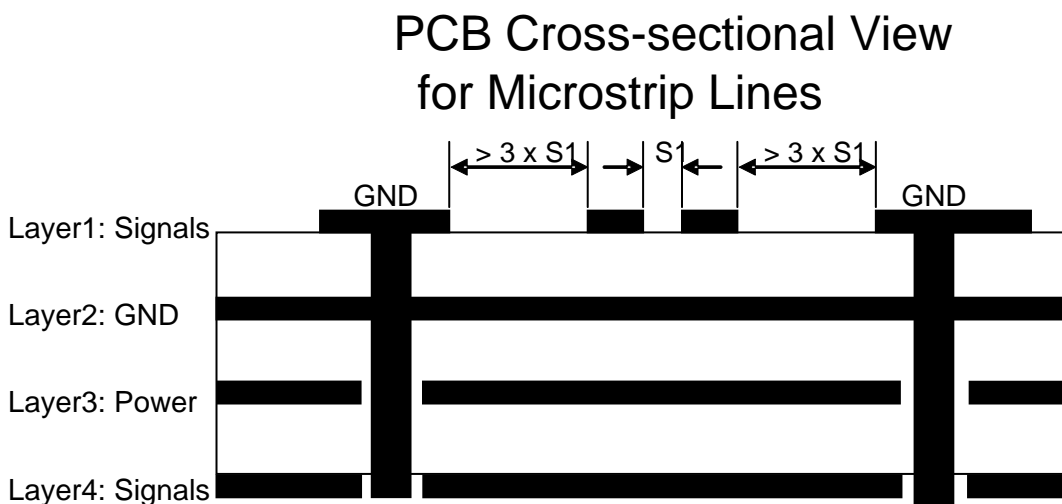


Figure 29 PCB Cross-sectional View for Microstrip Lines

6. Glossary

Table 22 Glossary of Terms

| | |
|----------------|---|
| Data Lane | One differential signal line |
| framing symbol | FSACTIVE, FSBS, FSBP, FSBE, and FSBE_SR are the framing symbols. One framing symbol is transmitted at the one pixel clock The size of framing symbols is decided by the byte mode |
| Byte mode | 3,4, and 5 byte mode is prepared. The byte mode is decided by the color depth and color format (RGB or YCbCr etc.) |
| Character | 8 bit data before 8b/10 encoder and after 10b/8b decoder 10 bit data after 8b/10 encoder and before 10b/8b decoder In addition to the pixel data, special character is assigned. See Table 4. |
| | |

7. Revision history

| Date | Version | |
|------------|----------|--|
| 2008/5/26 | Ver 1.0 | Original (obsolete) |
| 2008/11/22 | Ver 1.1 | <p>The color mapping is changed. The order of the pin assignment is changed. PLL loop bandwidth of the Transmitter is defined. Electrical specifications are described for LOCKN and HTPDN. Clarify the Inter-pair skew and Intra-pair skew specifications. RGBY and RGB+CMY is added to the color mapping. Inter lane skew is specified in the chapter 4.2.2. Collected the Training pattern (D10.2) frequency for link training in chapter 2.4.5.1 CDR training. Organization and Wording correction and clarification. (obsolete)</p> |
| 2009/1/15 | Ver. 1.2 | <p>The range of VDL is extended, and VOL spec. is changed. The behavior of the Scrambler is corrected. Correction of the value in tRISK_INTRA and tRISK_INTER. The Eye Diagram and CML Jitter at Transmitter are relaxed. Clarify the Receiver eye measurement point. Correction of the range of tTBIT and tRBIT. Correction of some typo.</p> |
| 2010/07/07 | Ver.1.3 | <p>Scrambler/descrambler chart is corrected. LFSR proceeds with K code. Vsync "1" in ALN Training allocation is corrected to 4th last pixel. ALN Training period per lane is fixed independent of lane counts. No HTPDN connection option is introduced. Basic receiver Eye-Diagram measurement point is at CML input pins. Transmitter intra-pair skew accuracy definition is conditioned and relaxed. Examples of lane number according to format (2560x1080p, 480Hz) are added. Guideline of frame ID transmission method for 3D display is added Receiver side Eye-Diagram measurement CDR setting explanation is added. Data lane consideration chapter is added. Section "Cable Characteristics" is deleted. Recommended approach to interoperable pin assignment is explained. 16 lane connection pin assignment guideline is added. Discrepancy of pulled up voltage is corrected. Description of FSBE_SR is clarified. Connector form factor of 51 pins receptacle is added. Page numbers on table of contents are corrected. Correction of some typo. Some descriptions are added.</p> |
| | | |
| | | |

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