THCV215 and THCV216

V-by-One® HS High-speed Video Data Transmitter and Receiver

General Description

THCV215 and THCV216 are designed to support video data transmission between the host and display.

The chipset can transmit 39bit video data and 3bit sync data via only a single differential cable at an LVDS clock frequency from 20MHz to 100MHz.

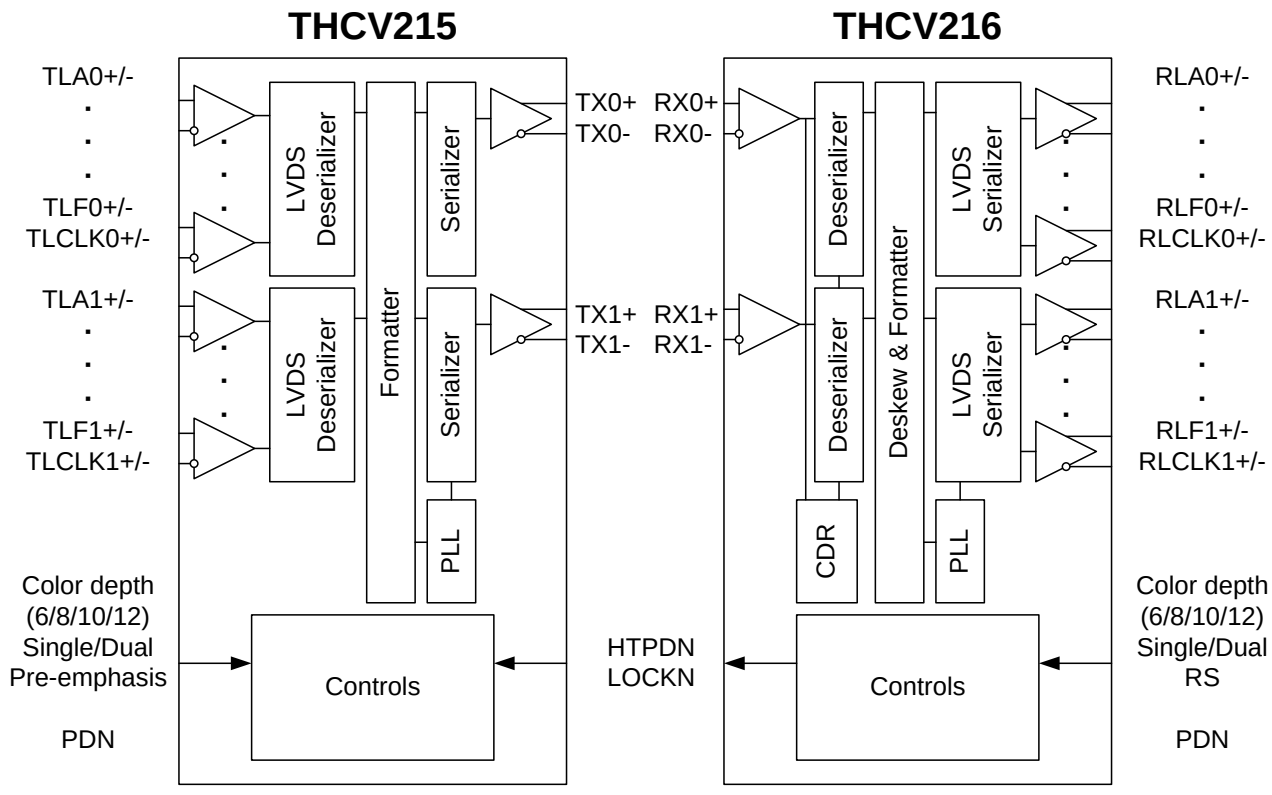
The chipset, which has two high-speed data lanes, can transmit the video data up to 1080p/10b/60Hz, 1080p/12b/60Hz. The maximum serial data rate is 3.75Gbps/lane.

Color Depth	Link	LVDS Clock Frequency
6bit	Single/Dual	20MHz to 100MHz
8bit	Single/Dual	20MHz to 100MHz
10bit	Single/Dual	20MHz to 85MHz
12bit	Single/Dual	20MHz to 75MHz

Features

- Color depth selectable: 6/8/10/12 bit
- Single/Dual Link selectable
- AC coupling
- LVDS Input internal termination
- CORE 1.8V, LVDS 3.3V
- Package: 64 pin TSSOP
- Wide frequency range
- CDR requires no external frequency reference
- Supports Spread Spectrum Clocking: Up to 30kHz/±0.5%(center spread)
- V-by-One® HS standard Version1.4 compliant

Block Diagram



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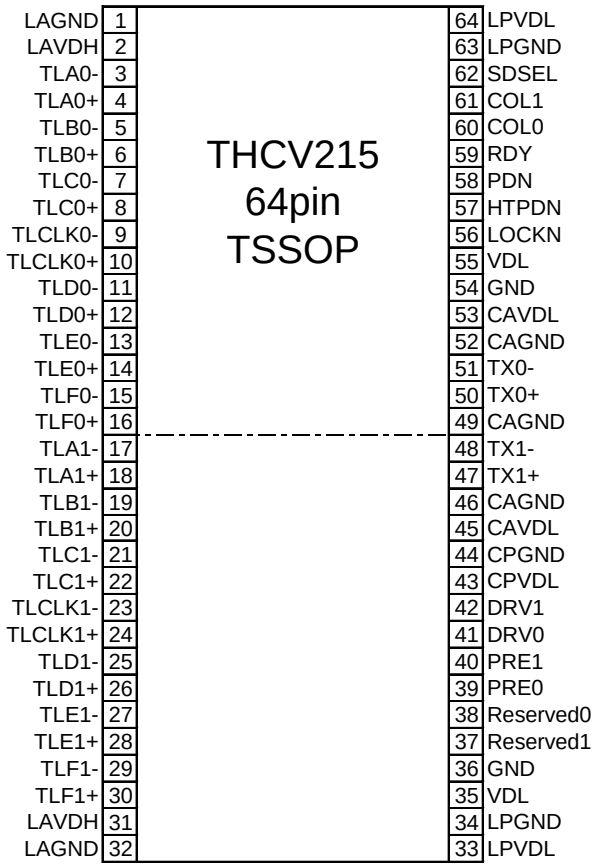
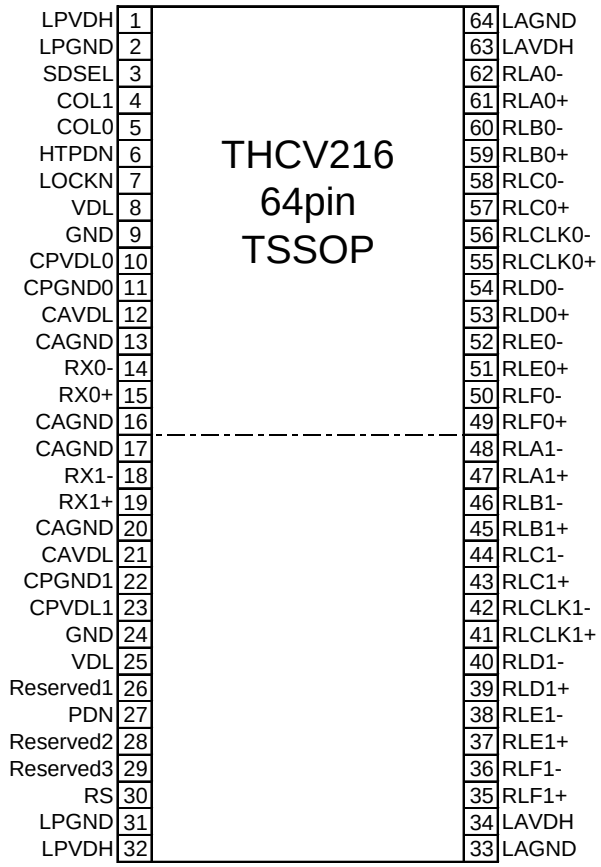
Pin Diagram





Pin Description

THCV215

Pin Name	Pin #	Type*	Description
TX0 +/-	50,51	CO	
TX1 +/-	47,48	CO	CML Data Output
TLA0+/-	4,3	LI	
TLB0+/-	6,5	LI	
TLC0+/-	8,7	LI	
TLCLK0+/-	10,9	LI	
TLD0+/-	12,11	LI	
TLE0+/-	14,13	LI	
TLF0+/-	16,15	LI	
TLA1+/-	18,17	LI	
TLB1+/-	20,19	LI	
TLC1+/-	22,21	LI	
TLCLK1+/-	24,23	LI	
TLD1+/-	26,25	LI	
TLE1+/-	28,27	LI	
TLF1+/-	30,29	LI	LVDS Data Input
LOCKN	56	I	Lock detect input
HTPDN	57	I	Hot plug detect input
PDN	58	I	Power down input H: Normal Operation L: Power down (CML output High Fix, other High-Z)
COL1, COL0	61,60	I	Color depth select input L,L: 6bit L,H: 8bit H,L: 10bit H,H: 12bit
SDSEL	62	I	Single/Dual select input L: Channel0 enable, Channel1 disable H: Channel0, Channel1 enable
DRV1	42	I	Must be tied to GND
DRV0	41	I	Must be tied to VDL
PRE1, PRE0	40,39	I	Pre-emphasis level select input L,L: 0% H,L: 100% L,H: not available H,H: not available
RDY	59	O	Link status ready output L: not ready H: ready
Reserved1	37	I	Field BET mode enable input L: Normal operation (default) H: Field BET mode enabled
Reserved0	38	I	Must be tied to GND
VDL	35,55	P	1.8V power supply pin for digital circuitry
GND	36,54	P	Ground pin for digital circuitry
CAVDL	45,53	P	1.8V power supply pin for CML output
CAGND	46,49,52	P	Ground pin for CML output
CPVDL	43	P	1.8V power supply pin for PLL circuitry
CPGND	44	P	Ground pin for PLL circuitry
LPVDL	33,64	P	1.8V power supply pin for LVDS PLL
LPGND	34,63	P	Ground pin for LVDS PLL circuitry
LAVDH	2,31	P	3.3V power supply pin for LVDS input
LAGND	1,32	P	Ground pin for LVDS input

Note) All CMOS inputs are 1.8V-inputs except for THCV216's RS

THCV216

Pin Name	Pin #	Type*	Description
RX0 +/-	15,14	CI	
RX1 +/-	19,18	CI	CML Data Input
RLA0+/-	61,62	LO	
RLB0+/-	59,60	LO	
RLC0+/-	57,58	LO	
RLCLK0+/	55,56	LO	
RLD0+/-	53,54	LO	
RLE0+/-	51,52	LO	
RLF0+/-	49,50	LO	
RLA1+/-	47,48	LO	
RLB1+/-	45,46	LO	
RLC1+/-	43,44	LO	
RLCLK1+/	41,42	LO	
RLD1+/-	39,40	LO	
RLE1+/-	37,38	LO	
RLF1+/-	35,36	LO	LVDS Data Output
LOCKN	7	O	Lock detect output (open drain)
HTPDN	6	O	Hot plug detect output (open drain)
PDN	27	I	Power down input H: Normal Operation L: Power down (High-Z)
COL1, COL0	4,5	I	Color depth select input L,L: 6bit L,H: 8bit H,L: 10bit H,H: 12bit
SDSEL	3	I	Single/Dual select input L: Channel0 enable, Channel1 disable H: Channel0, Channel1 enable
RS	30	IO3	Direction of RS pin depends on Reserved3. LVDS swing range select input when Reserved3=L H: Normal swing (350mV typ.) L: Reduced swing (200mV typ.) Field BET output when Reserved3=H. Goes LOW when errors detected.
Reserved 1,2	26,28	I	Must be tied to GND
Reserved3	29	I	Field BET mode enable input L: Normal operation (default) H: Field BET mode enabled
VDL	8,25	P	1.8V power supply pin for digital circuitry
GND	9,24	P	Ground pin for digital circuitry
CAVDL	12,21	P	1.8V power supply pin for CML input
CAGND	13,16, 17,20	P	Ground pin for CML input
CPVDL0	10	P	1.8V power supply pin for PLL circuitry
CPGND0	11	P	Ground pin for PLL circuitry
CPVDL1	23	P	1.8V power supply pin for PLL circuitry
CPGND1	22	P	Ground pin for PLL circuitry
LPVDH	1,32	P	3.3V power supply pin for LVDS PLL
LPGND	2,31	P	Ground pin for LVDS PLL circuitry
LAVDH	34,63	P	3.3V power supply pin for LVDS output
LAGND	33,64	P	Ground pin for LVDS output

*type symbol
I=1.8V CMOS Input, O=1.8V CMOS Output, IO3=3.3V CMOS I/O
LI=LVDS Input, LO= LVDS Output
CI=CML Input, CO=CML Output
P=Power

Functional Description

Functional Overview

With V-by-One®HS's proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV215 and THCV216 enable transmission of 18/24/30/36bits per pixel video data (Rn/Gn/Bn/CONTn), Hsync (HSYNCn), Vsync (VSYNCn) data and Data Enable (DE) by single/dual differential pair cable with minimal external components.

THCV215, the transmitter, inputs LVDS data (including video data, Hsync, Vsync and DE) and serializes video data and Hsync, Vsync data separately, depending on the polarity of DE. DE is a signal which indicates whether video or Hsync, Vsync data are active. When DE is high, it serializes video data inputs into a single differential data stream. And it transmits serialized Hsync, Vsync data when DE is low.

THCV216, the receiver, automatically extracts the clock from the incoming data stream and converts the serial data into video data with DE being high or Hsync, Vsync data with DE being low, recognizing which type of serial data is being sent by the transmitter. And it outputs the recovered data in the form of LVDS data.

THCV216 can seamlessly operate for a wide range of a serial bit rate from 600Mbps to 3.75Gbps/channel, detecting the frequency of an incoming data stream, and recovering both the clock and data by itself.

It does not need any external frequency reference, such as a crystal oscillator.

Data Enable Requirement (DE)

There are some requirements for DE as described in Figure 2, Figure 3 and Table 15.

Dual LVDS input to THCV215 should be synchronized in terms of DE transition. See Figure 2.

If DE=Low, Hsync and Vsync data of same cycle are transmitted. Otherwise video data of that are transmitted (DE=High). SYNC data from receiver in DE=High period are previous data of DE transition. See Figure 3.

The length of DE being low and high is at least 2 clock cycles long as described in Table 15.

Data Enable must be toggled like High -> Low -> High at regular interval.

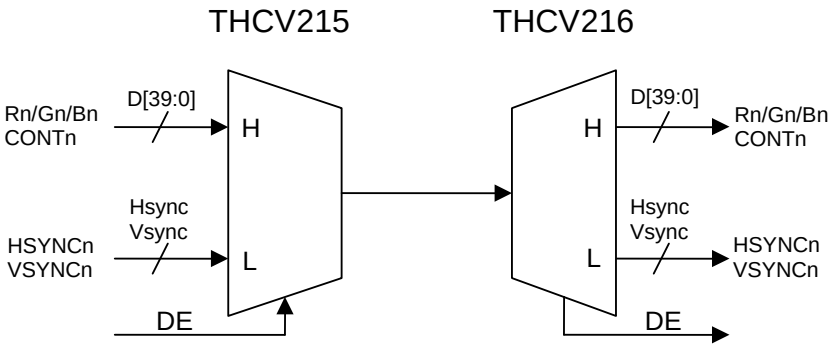


Figure 1. Conceptual diagram of the basic operation of the chipset

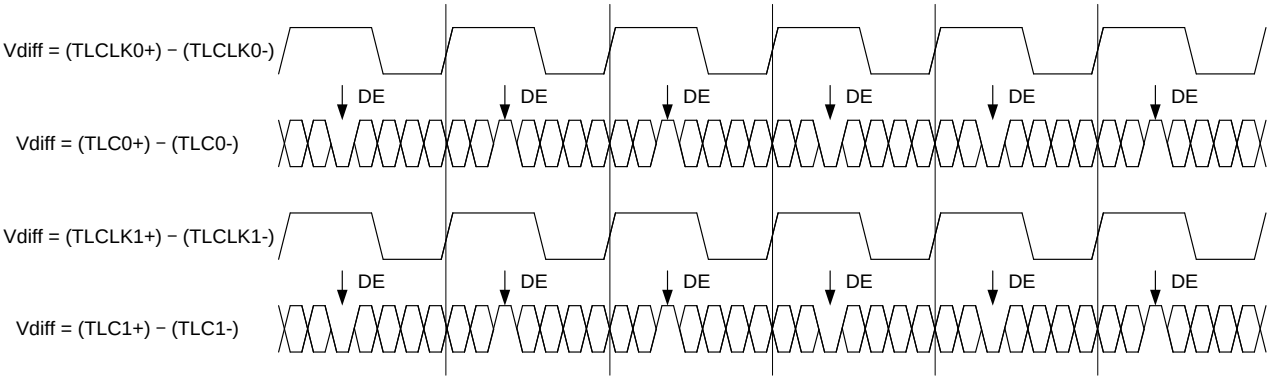


Figure 2. Service condition of DE input synchronization

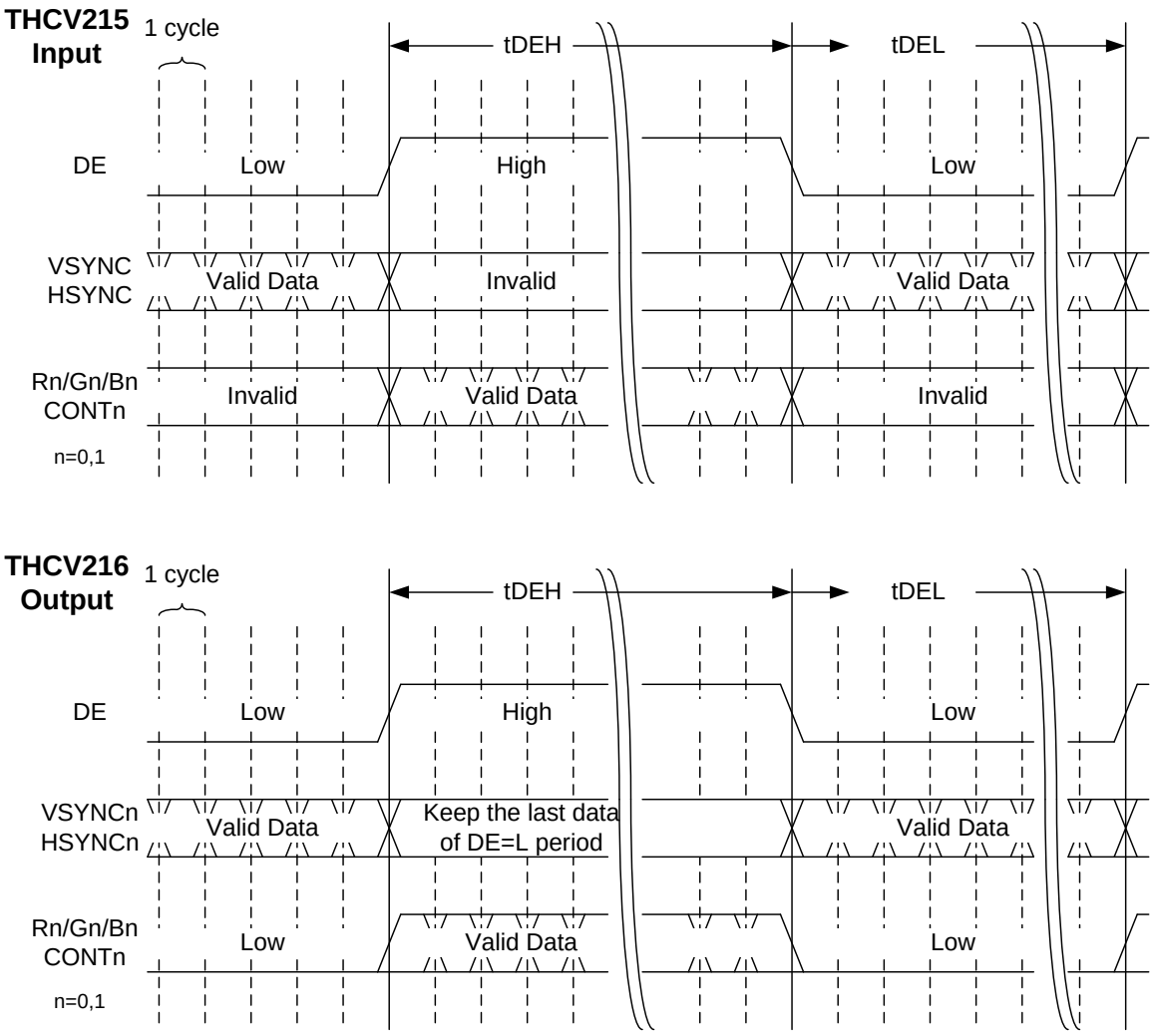


Figure 3. Video and sync data transmission timing diagram

Single/Dual Link mode function (SDSEL)

SDSEL	Mode	Function
H	Single	Channel 0 active and channel 1 power down
L	Dual	Both channel 0 and channel 1 active

Table 1. Single/Dual mode select

Color Depth mode function (COL [1:0])

COL[1:0]	Color Depth	LVDS Clock Frequency Range
L,L	6bit	20MHz to 100MHz
L,H	8bit	20MHz to 100MHz
H,L	10bit	20MHz to 85MHz
H,H	12bit	20MHz to 75MHz

Table 2. Color depth mode select

LVDS Mapping

LVDS data (video data, Hsync, Vsync, DE) are mapped as Figure 4. TLC0[6] is special bit for DE(data enable), and TLC0[5:4] are for Hsync, Vsync data bits and the other bits are for video data.

The number of LVDS channel depends on color depth mode(COL[1:0]).

If SDSEL=Low, only channel 0 (Figure 4, n=0) is active. If SDSEL=High, both channel 0/1(Figure 4, n=0/1) are active. (TLC1[6:4] are not available).

Depending on color mode, TLD1[6] and TLD0[6] are not available. See Table 3.

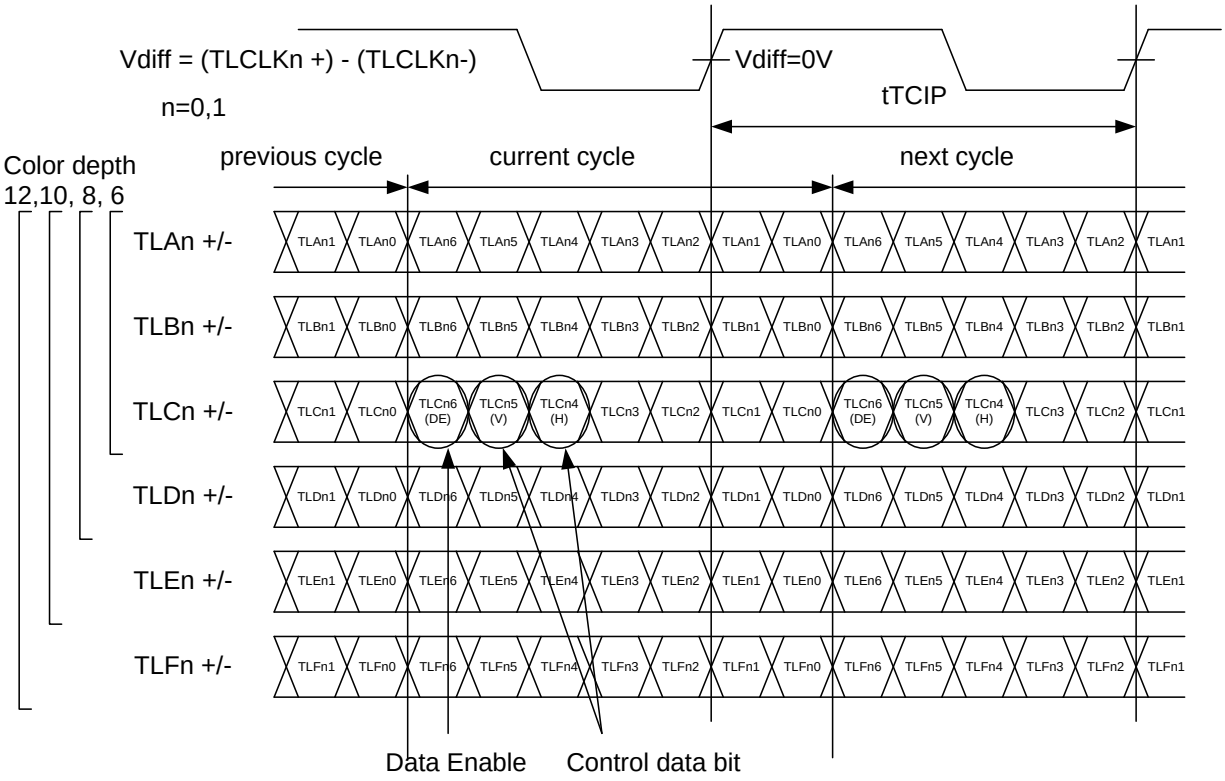


Figure 4. LVDS mapping timing diagram

THCV215 Input	THCV216 Output	Color depth (COL[1:0])				Symbol defined by V-by-One® HS
		L,L (6bit)	L,H (8bit)	H,L (10bit)	H,H (12bit)	
TLAn[0]	RLAn[0]	Rn[0]	Rn[2]	Rn[4]	Rn[6]	D2
TLAn[1]	RLAn[1]	Rn[1]	Rn[3]	Rn[5]	Rn[7]	D3
TLAn[2]	RLAn[2]	Rn[2]	Rn[4]	Rn[6]	Rn[8]	D4
TLAn[3]	RLAn[3]	Rn[3]	Rn[5]	Rn[7]	Rn[9]	D5
TLAn[4]	RLAn[4]	Rn[4]	Rn[6]	Rn[8]	Rn[10]	D6
TLAn[5]	RLAn[5]	Rn[5]	Rn[7]	Rn[9]	Rn[11]	D7
TLAn[6]	RLAn[6]	Gn[0]	Gn[2]	Gn[4]	Gn[6]	D10
TLBn[0]	RLBn[0]	Gn[1]	Gn[3]	Gn[5]	Gn[7]	D11
TLBn[1]	RLBn[1]	Gn[2]	Gn[4]	Gn[6]	Gn[8]	D12
TLBn[2]	RLBn[2]	Gn[3]	Gn[5]	Gn[7]	Gn[9]	D13
TLBn[3]	RLBn[3]	Gn[4]	Gn[6]	Gn[8]	Gn[10]	D14
TLBn[4]	RLBn[4]	Gn[5]	Gn[7]	Gn[9]	Gn[11]	D15
TLBn[5]	RLBn[5]	Bn[0]	Bn[2]	Bn[4]	Bn[6]	D18
TLBn[6]	RLBn[6]	Bn[1]	Bn[3]	Bn[5]	Bn[7]	D19
TLCn[0]	RLCn[0]	Bn[2]	Bn[4]	Bn[6]	Bn[8]	D20
TLCn[1]	RLCn[1]	Bn[3]	Bn[5]	Bn[7]	Bn[9]	D21
TLCn[2]	RLCn[2]	Bn[4]	Bn[6]	Bn[8]	Bn[10]	D22
TLCn[3]	RLCn[3]	Bn[5]	Bn[7]	Bn[9]	Bn[11]	D23
TLCn[4]	RLCn[4]	HSYNCn	HSYNCn	HSYNCn	HSYNCn	Hsync
TLCn[5]	RLCn[5]	VSYNCn	VSYNCn	VSYNCn	VSYNCn	Vsync
TLCn[6]	RLCn[6]	DEn(*2)	DEn(*2)	DEn(*2)	DEn(*2)	DE
TLDn[0]	RLDn[0]	Channel Power Down	Rn[0]	Rn[2]	Rn[4]	D0
TLDn[1]	RLDn[1]		Rn[1]	Rn[3]	Rn[5]	D1
TLDn[2]	RLDn[2]		Gn[0]	Gn[2]	Gn[4]	D8
TLDn[3]	RLDn[3]		Gn[1]	Gn[3]	Gn[5]	D9
TLDn[4]	RLDn[4]		Bn[0]	Bn[2]	Bn[4]	D16
TLDn[5]	RLDn[5]		Bn[1]	Bn[3]	Bn[5]	D17
TLDn[6]	RLDn[6]		N/A(*1)	CONTn[1]	CONTn[3]	D25(*3)
TLEn[0]	RLEn[0]	Channel Power Down	Channel Power Down	Rn[0]	Rn[2]	D30
TLEn[1]	RLEn[1]			Rn[1]	Rn[3]	D31
TLEn[2]	RLEn[2]			Gn[0]	Gn[2]	D28
TLEn[3]	RLEn[3]			Gn[1]	Gn[3]	D29
TLEn[4]	RLEn[4]			Bn[0]	Bn[2]	D26
TLEn[5]	RLEn[5]			Bn[1]	Bn[3]	D27
TLEn[6]	RLEn[6]			CONTn[2]	CONTn[4]	D24(*3)
TLFn[0]	RLFn[0]	Channel	Channel Power Down	Channel Power Down	Rn[0]	D38
TLFn[1]	RLFn[1]				Rn[1]	D39
TLFn[2]	RLFn[2]				Gn[0]	D36
TLFn[3]	RLFn[3]				Gn[1]	D37
TLFn[4]	RLFn[4]				Bn[0]	D34
TLFn[5]	RLFn[5]				Bn[1]	D35
TLFn[6]	RLFn[6]				CONTn[1]	D33

n=0,1 : if SDSEL=L, Channel 1(n=1) is power down

*1 N/A: Not available, THCV216 output RLDn[6]=Low.

*2 DE must be same polarity(TLC0[6] = TLC1[6]) when SDSEL=H

*3 3D information flags defined in the V-by-One® HS Standard are assigned to the following bit.

V-by-One® HS Standard Packer/Unpacker D[24](3DLR) <=> LVDS T/RLEn[6]

V-by-One® HS Standard Packer/Unpacker D[25](3DEN) <=> LVDS T/RLDn[6]

Table 3. LVDS mapping table

CML Buffer

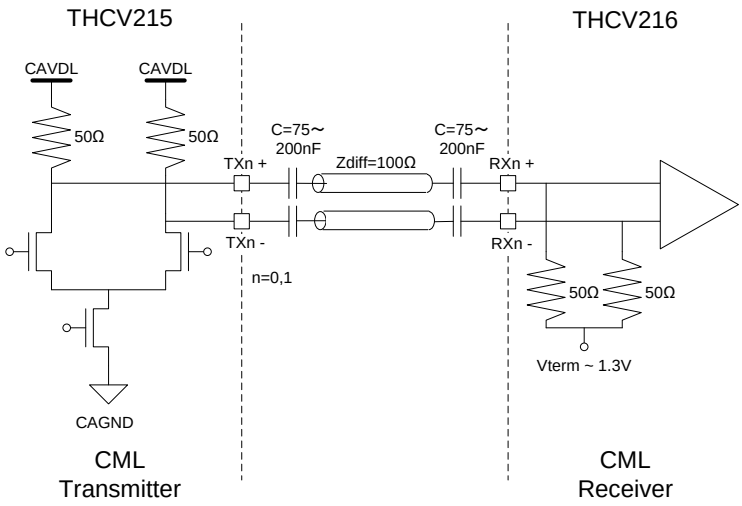


Figure 5. CML buffer scheme

Lock detect and Hot-plug function

LOCKN and HTPDN are both open drain output from THCV216. Pull-up resistors are needed at THCV215 side to VDL. See Figure 6.

If THCV216 is not active (power down mode (PDN=L) or powered off), HTPDN is open. Otherwise, HTPDN is pulled down by THCV216.

HTPDN of THCV215 side is High when THCV216 is not active or the receiver board is not connected. Then THCV215 enters into the power down mode. When HTPDN transits from High to Low, THCV215 starts up and transmits training pattern for link training.

LOCKN indicates whether THCV216 is in the lock state or not. If THCV216 is in the unlock state, LOCKN is open. Otherwise (in the lock state), it's pulled down by THCV216.

THCV215 keeps transmitting training pattern until LOCKN transits to Low. After training done, THCV216 sinks current and LOCKN is Low. Then THCV215 starts transmitting normal video pattern.

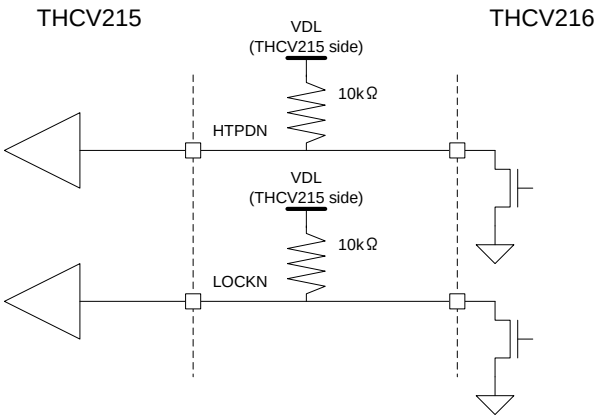


Figure 6. Hot-plug and Lock detect scheme

No HTPDN connection option

HTPDN connection between THCV215 and THCV216 can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken ad Low. See Figure 7.

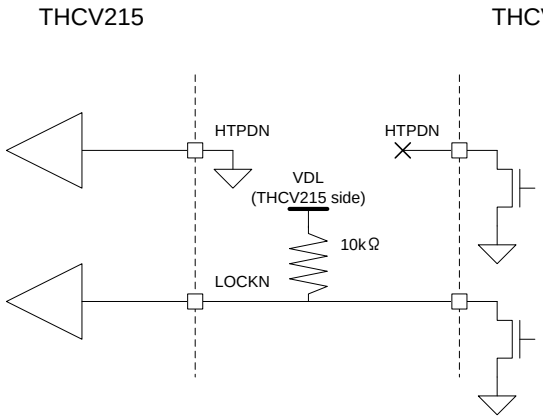


Figure 7. HTPDN is not connected scheme

THCV215 Pre-emphasis function (PRE [1:0])

Pre-emphasis can equalize severe signal degradation caused by long distance or high-speed transmission. Two pins, PRE1 and PRE0, select the strength of pre-emphasis. See Table 4.

PRE[1:0]	Description
L,L	w/o Pre-emphasis
H,L	w/ 100% Pre-emphasis
L,H / H,H	Not available

Table 4. Pre-emphasis function table

THCV215 Power Down function (PDN)

By setting the PDN pin to low, it results in the power down mode. All the internal circuitry turns off and the both TXn+/- (n=0, 1) outputs turn to VDL.

THCV216 Power Down function (PDN)

By setting the PDN pin to low, it results in the power down mode. All the internal circuitry turns off and the RLXn+/- (X=A, B, C, D, E, F, CLK, n=0, 1) outputs turn to High-Z.

THCV215 Link Ready function (RDY)

This is a CMOS output for indicating the link status. RDY=High if link is ready.

Field BET Operation

In order to help users to check the validity of high speed serial links (CML lines), THCV215/THCV216 have an operation mode in which they act as the bit error tester (BET). In this mode, THCV215 internally generates a test pattern, which is then serialized onto the CML high speed lines. THCV216 receives the data stream and checks the sampled data for bit errors.

This "Field BET" mode is activated by setting Reserved1= H on THCV215 and Reserved3= H on THCV216 (Refer to Table 5).

In the Field BET mode, the on-chip pattern generator on THCV215 is enabled and generates the test pattern as long as the LVDS clocks (TLCLK0+/-, TLCLK1+/-) are applied. Other LVDS data inputs may be left open or applied with any pattern. They are ignored by THCV215. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channels. As for THCV216, the internal test pattern check circuit gets enabled and the RS pin, which is normally an input, turns into an output for the pattern checker (LVDS output level is internally configured to be "Normal Swing"). The RS pin goes LOW whenever bit errors occur, and it stays HIGH when there is no bit error. Please Refer to Figure 8.

Product	THCV215	THCV216	
Pin Name	Reserved1	Reserved3	RS
Normal	L	L	3.3V INPUT H: Normal Swing, L: Reduced Swing
Field BET	H	H	3.3V OUTPUT Goes LOW when bit errors occur.

Table 5. Field BET Operation Pin Settings

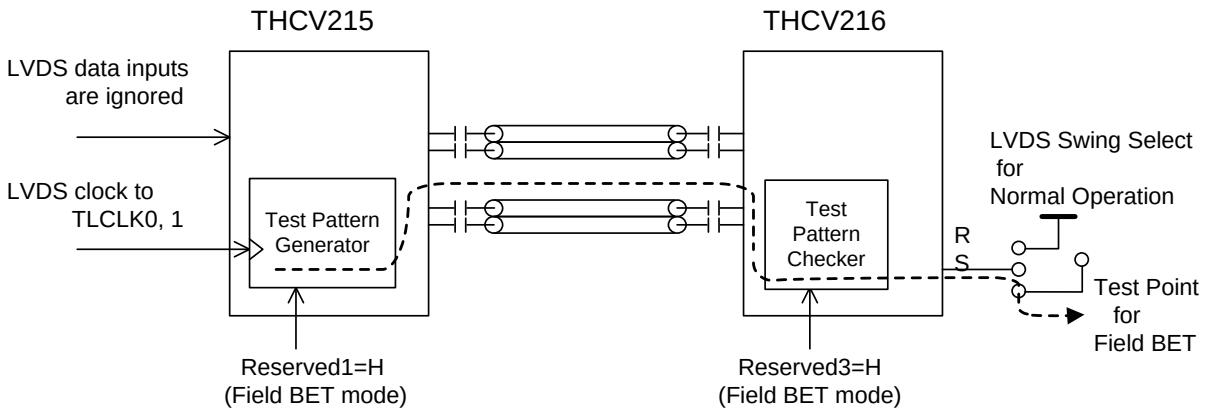


Figure 8. Field BET Configuration

Absolute Maximum Ratings*

Parameter	Min.	Typ.	Max.	Units
1.8V Supply Voltage（VDL,CAVDL,CPVDL,LPVDL）	-0.3	-	+2.1	V
3.3V Supply Voltage(LAVDH)	-0.3	-	+4.0	V
1.8V CMOS Input Voltage	-0.3	-	VDL+0.3	V
1.8V CMOS Output Voltage	-0.3	-	VDL+0.3	V
LVDS Receiver Input Voltage	-0.3	-	LAVDH+0.3	V
CML Transmitter Output Voltage	-0.3	-	CAVDL+0.3	V
Output Current	-50	-	50	mA
Storage Temperature	-55	-	+125	°C
Junction Temperature	-	-	+125	°C
Reflow Peak Temperature / Time	-	-	+260/10sec	°C

Table 6. THCV215 Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
1.8V Supply Voltage(VDL,CAVDL,CPVDL0,CPVDL1)	-0.3	-	+2.1	V
3.3V Supply Voltage(LPVDH,LAVDH)	-0.3	-	+4.0	V
1.8V CMOS Input Voltage	-0.3	-	VDL+0.3	V
3.3V CMOS Input Voltage	-0.3	-	LAVDH+0.3	
CMOS Output Voltage	-0.3	-	+2.1	V
CML Receiver Input Voltage	-0.3	-	CAVDL+0.3	V
LVDS Transmitter Output Voltage	-0.3	-	LAVDH+0.3	V
Output Current	-30	-	30	mA
Storage Temperature	-55	-	+125	°C
Junction Temperature	-	-	+125	°C
Reflow Peak Temperature / Time	-	-	+260/10sec	°C
Maximum Power Dissipation @+25℃	-	-	2	W
Lead Temperature (Soldering, 10sec)	-	-	+260	°C

Table 7. THCV216 Absolute Maximum Ratings

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
1.8V Supply Voltage（VDL,CAVDL,CPVDL,LPVDL）	1.62	1.80	1.98	V
3.3V Supply Voltage(LAVDH)	3.00	3.30	3.60	V
Operating Temperature	0	-	70	℃

Table 8. THCV215 Operating Conditions

Parameter	Min.	Typ.	Max.	Units
1.8V Supply Voltage(VDL,CAVDL,CPVDL0,CPVDL1) except for the 12 bit color depth mode	1.62	1.80	1.98	V
1.8V Supply Voltage(VDL,CAVDL,CPVDL0,CPVDL1) for the 12 bit color depth mode	1.71	1.80	1.89	V
3.3V Supply Voltage(LPVDH,LAVDH)	3.00	3.30	3.60	V
Operating Temperature	0	-	70	℃

Table 9. THCV216 Operating Conditions

* "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Electrical Specifications

1.8V & 3.3V CMOS DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High Level Input Voltage		0.65 × VDL	-	VDL	V
VIL	Low Level Input Voltage		0	-	0.35 × VDL	V
VOH	High Level Output Voltage	IOH=-2mA	VDL-0.45	-	-	V
VOL	Low Level Output Voltage	IOL=2mA	-	-	0.2	V
IIH	Input Leak Current High	VIN=VDL	-	-	±10	uA
IIL	Input Leak Current Low	VIN=0V	-	-	±10	uA
VIH3	High Level Input Voltage (3.3V inputs)		2.1	-	LAVDH	V
VIL3	Low Level Input Voltage (3.3V inputs)		0	-	0.8	V
VOH3	High Level Output Voltage (3.3V outputs)	IOH=-4mA	2.4	-	-	V
VOL3	Low Level Output Voltage (3.3V outputs)	IOL=4mA	-	-	0.4	V
IIH3	Input Leak Current High (3.3V inputs)	VIN=LAVDH	-	-	±10	uA
IIL3	Input Leak Current Low (3.3V inputs)	VIN=0V	-	-	±10	uA

Table 10. THCV215 and THCV216 1.8V & 3.3V CMOS DC Specifications

CML & LVDS DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VTTH	LVDS Differential Input High Threshold		-	-	100	mV
VTTL	LVDS Differential Input Low Threshold		-100	-	-	mV
ITIH	LVDS Input Leak Current High	PDN=L, TLxn+/-=LAVDH	-	-	±10	uA
ITIL	LVDS Input Leak Current Low	TLxn+/-=0V,PDN=L	-	-	±10	uA
RTIN	LVDS Differential Input Resistance	PDN=L	80	100	120	Ω
VTOD	CML Differential Mode Output Voltage	DRV[1:0]=L,H PRE[1:0]=L,L	200	300	400	mV
PRE	CML Pre-emphasis Level	PRE[1:0]=L,L	-	0	-	%
		PRE[1:0]=H,L	80	100	120	%
VTOC	CML Common Mode Output Voltage	PRE[1:0]=L,L	CAVDL-VTOD			mV
		PRE[1:0]=H,L	CAVDL-2 × VTOD			mV
ITOH	CML Output Leak Current High	PDN=L		-	±10	uA
ITOS	CML Output Short Circuit Current	CAVDL=1.8V	-90	-	-	mA

Table 11. THCV215 CML & LVDS DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VRTH	CML Differential Input High Threshold		-	-	50	mV
VRTL	CML Differential Input Low Threshold		-50	-		mV
IRIH	CML Input Leak Current High	PDN=L, RXn+/-=CAVDL	-	-	±10	uA
IRIL	CML Input Leak Current Low	PDN=L,RXn+/-=0V	-	-	±10	uA
IRRIH	CML Input Current High	RXn+/-=CAVDL	-	-	2	mA
IRRIL	CML Input Current Low	RXn+/-=0V	-6	-	-	mA
RRIN	CML Differential Input Resistance		80	100	120	Ω
VROD	LVDS Differential Mode Output Voltage (Normal Swing)	RL=100Ω, RS=H	250	350	450	mV
	LVDS Differential Mode Output Voltage (Reduced Swing)	RL=100Ω, RS=L	100	200	300	mV
ΔVROD	Change in VROD between Complementary Output States	RL=100Ω	-	-	35	mV
VROC	LVDS Common Mode Output Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVROC	Change in VROC between Complementary Output States	RL=100Ω	-	-	35	mV
IROS	LVDS Output Short Circuit Current	RLxn+/-=0V	-24	-	-	mA
IROZ	LVDS Output TRI-STATE Current	PDN=L, RLxn+/-=0V / LAVDH x=A~F,CLK, n=0, 1	-	-	±10	uA

Table 12. THCV216 CML & LVDS DC Specifications

Supply Currents

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ITCCW	Supply Current for 1.8V Power Supply (Worst Case Pattern)	COL[1:0]=H,H PRE[1:0]=H,L SDSEL=H	-	-	210	mA
ITCCW33	Supply Current for 3.3V Power Supply (Worst Case Pattern)	COL[1:0]=H,H PRE[1:0]=H,L SDSEL=H	-	-	90	mA
ITCCS	Power Down Supply Current	PDN=L All Inputs =Fixed L or H	-	-	200	uA

Table 13. THCV215 Supply Currents

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IRCCW	Supply Current for 1.8V Power Supply (Worst Case Pattern)	COL[1:0]=H,H SDSEL=H RS=H	-	-	160	mA
IRCCW33	Supply Current for 3.3V Power Supply (Worst Case Pattern)	COL[1:0]=H,H SDSEL=H RS=H	-	-	190	mA
IRCCS	Power Down Supply Current	PDN=L All Inputs =Fixed L or H	-	-	200	uA

Table 14. THCV216 Supply Currents

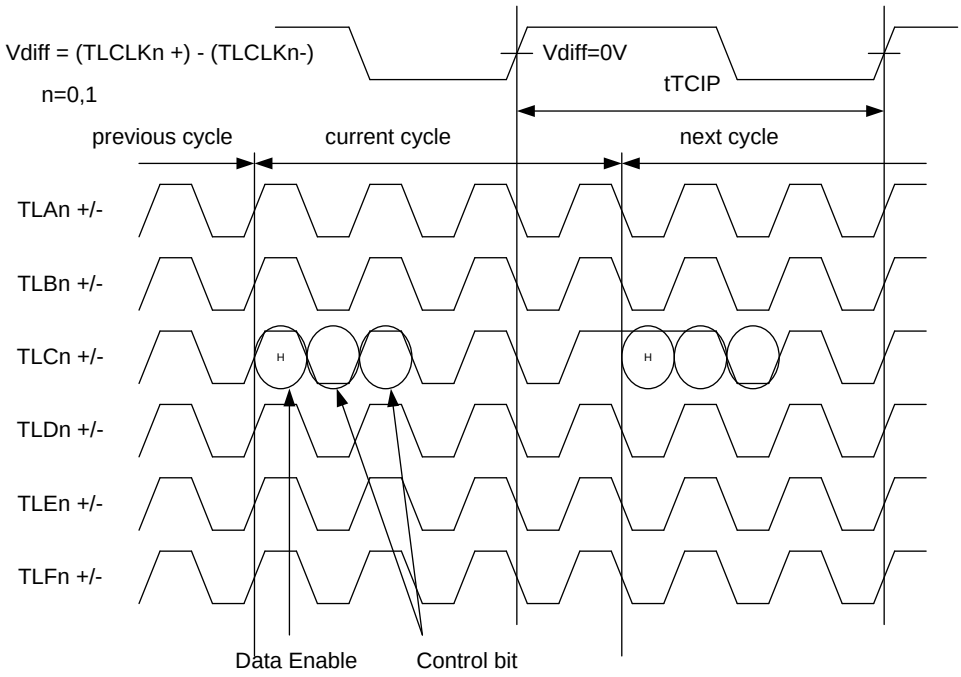


Figure 9. Worst Case Pattern

Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tDEH	DE=High Duration		2tTCIP	-	-	sec
tDEL	DE=Low Duration		2tTCIP	-	-	sec

Table 15. DE requirement

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
		COL[1:0]=L,L | L,H	10	-	50	ns
		COL[1:0]=H,L	11.76	-	50	ns
tTCIP	TLCLK Period	COL[1:0]=H,H	13.3	-	50	ns
tTCIH	LVDS Differential Clock High Time		2×tTCIP/7	-	5×tTCIP/7	ns
tTCIL	LVDS Differential Clock Low Time		2×tTCIP/7	-	5×tTCIP/7	ns
		tTCIP=75MHz	-440	-	440	ps
		tTCIP=85MHz	-390	-	390	ps
tSK	LVDS Receiver Skew Margin	tTCIP=100MHz	-330	-	330	ps
tTIP1	LVDS Input Data Position0		-tSK	0	+tSK	ns
tTIP0	LVDS Input Data Position1		tTCIP/7-tSK	tTCIP/7	tTCIP/7+tSK	ns
tTIP6	LVDS Input Data Position2		2×tTCIP/7-tSK	2×tTCIP/7	2×tTCIP/7+tSK	ns
tTIP5	LVDS Input Data Position3		3×tTCIP/7-tSK	3×tTCIP/7	3×tTCIP/7+tSK	ns
tTIP4	LVDS Input Data Position4		4×tTCIP/7-tSK	4×tTCIP/7	4×tTCIP/7+tSK	ns
tTIP3	LVDS Input Data Position5		5×tTCIP/7-tSK	5×tTCIP/7	5×tTCIP/7+tSK	ns
tTIP2	LVDS Input Data Position6		6×tTCIP/7-tSK	6×tTCIP/7	6×tTCIP/7+tSK	ns
tTISK	Lane0/1 LVDS Input Clock Skew		-0.3×tTCIP	-	0.3×tTCIP	ns
tTRF	CML Output Rise and Fall Time(20%-80%)		50	-	150	ps
tTOSK	CML Lane0/1 Output Inter Pair Skew		-2	-	2	UI
tTCD	Input Clock to Output Data Delay		(56/(5×n)+6.1) ×tTCIP-5 (1)	-	(56/(5×n)+6.1) ×tTCIP+5 (1)	ns
tTPD	Power On to PDN High Delay		0	-	-	ns
tTPLL0	PDN High to CML Output Delay		-	-	10	ms
tTPLL1	PDN Low to CML Output High Fix Delay		-	-	20	ns
tTNP0	LOCKN High to Training Pattern Output Delay		-	-	10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay		-	-	10	ms

(1) n =3, 4, and 5 for 6/8bit, 10bit, and 12bit mode, respectively.

Table 16. THCV215 Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
		COL[1:0]=L,L | L,H	333	tTCIP/30	1667	ps
		COL[1:0]=H,L	294	tTCIP/40	1250	ps
tRBIT	Unit Interval	COL[1:0]=H,H	266	tTCIP/50	1000	ps
tRISK	CML Lane0/1 Input Inter Pair Skew Margin		-	-	15	UI
tRLVT	LVDS Differential Output Transition Time		-	0.6	1.5	ns
tROP1	LVDS Output Data Position0		-0.25	0	0.25	ns
tROP0	LVDS Output Data Position1		tTCIP/7-0.25	tTCIP/7	tTCIP/7+0.25	ns
tROP6	LVDS Output Data Position2		2×tTCIP/7-0.25	2×tTCIP/7	2×tTCIP/7+0.25	ns
tROP5	LVDS Output Data Position3		3×tTCIP/7-0.25	3×tTCIP/7	3×tTCIP/7+0.25	ns
tROP4	LVDS Output Data Position4		4×tTCIP/7-0.25	4×tTCIP/7	4×tTCIP/7+0.25	ns
tROP3	LVDS Output Data Position5		5×tTCIP/7-0.25	5×tTCIP/7	5×tTCIP/7+0.25	ns
tROP2	LVDS Output Data Position6		6×tTCIP/7-0.25	6×tTCIP/7	6×tTCIP/7+0.25	ns
tROSK	Lane0/1 LVDS Output Clock Skew		-	-	50	ps
tRDC	Input Data to Output Clock Delay		(178+68×n) ×tRBIT-5 (1)	-	(178+68×n) ×tRBIT+5 (1)	ns
tRPD	Power On to PDN High Delay		0	-	-	ns
tRHPD0	PDN High to HTPDN Low Delay		-	-	1	us
tRHPD1	PDN Low to HTPDN High Delay		-	-	1	us
tRPLL0	Training Pattern Input to LOCKN Low Delay		-	-	10	ms
tRPLL1	PDN Low to LOCKN High Delay		-	-	10	us
tRLCK0	LOCKN Low to LVDS Output Delay		-	-	1	ms
tRLCK1	LOCKN High to LVDS High-Z Delay		-	-	0	ns

(1) n =3, 4, and 5 for 6/8bit, 10bit, and 12bit mode, respectively.

Table 17. THCV216 Switching Characteristics

AC Timing Diagrams and Test Circuits

THCV215 LVDS Input Switching Characteristics

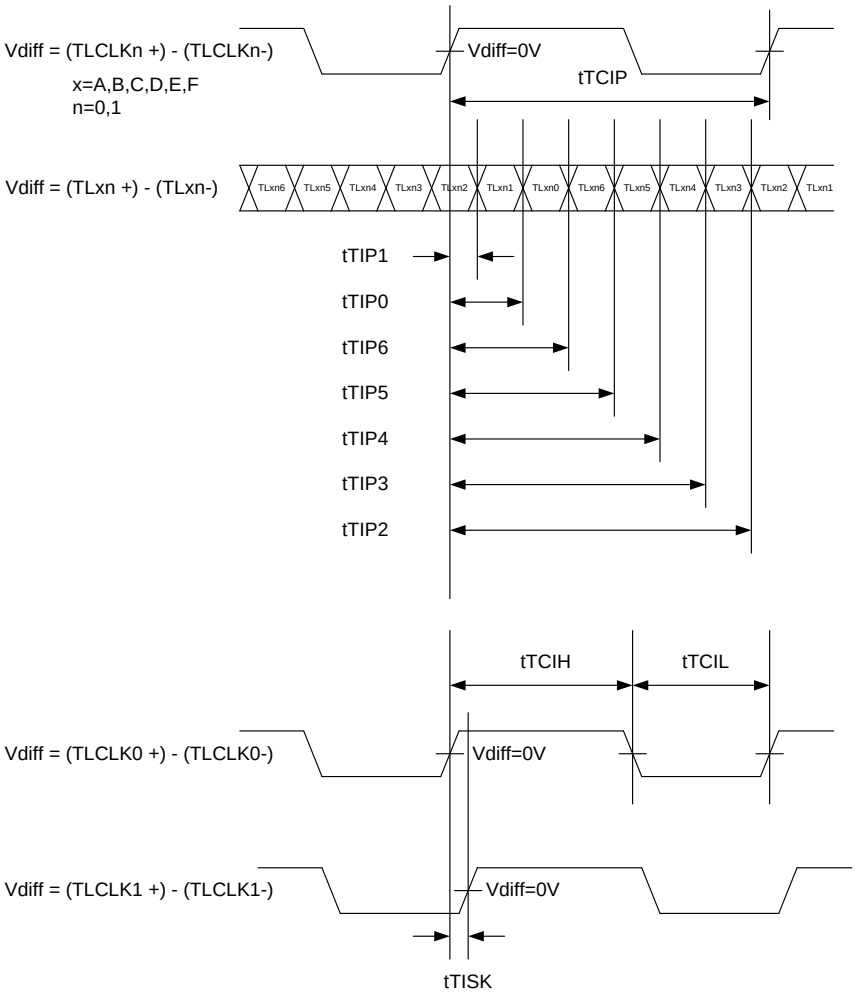


Figure 10. THCV215 LVDS Input Switching Timing Diagrams

THCV216 LVDS Output Switching Characteristics

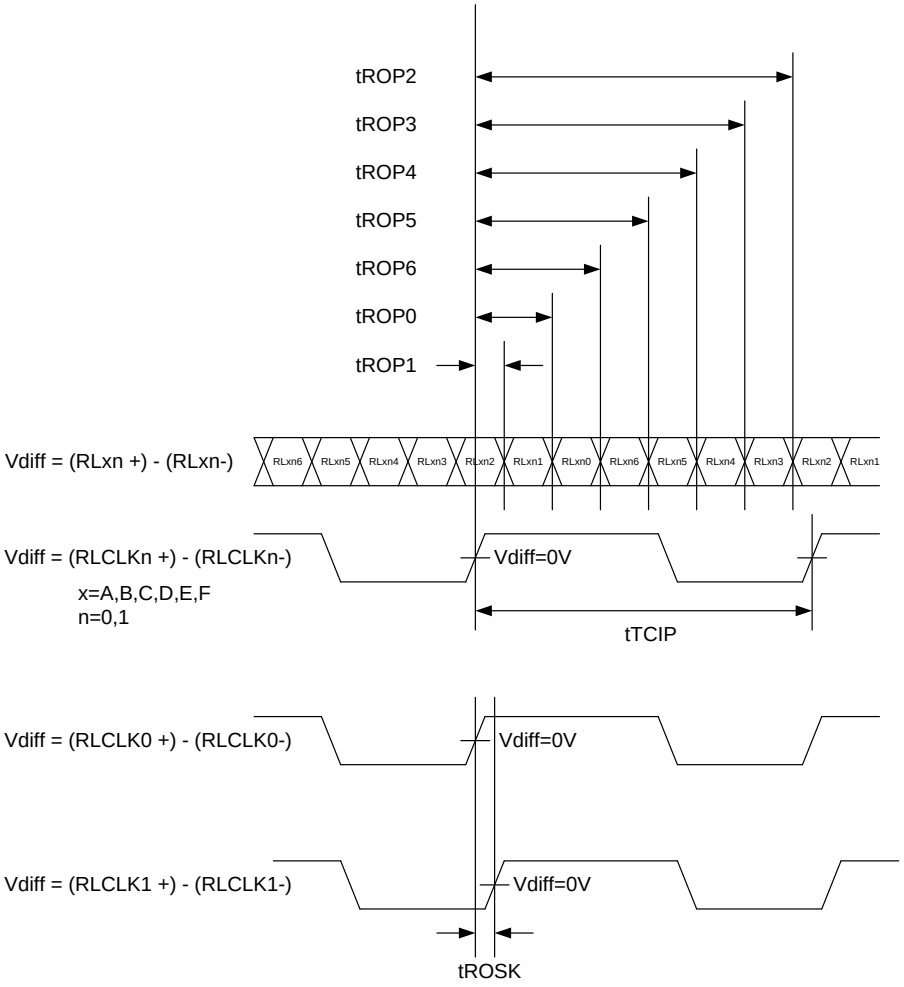


Figure 11. THCV216 LVDS Output Switching Timing Diagrams

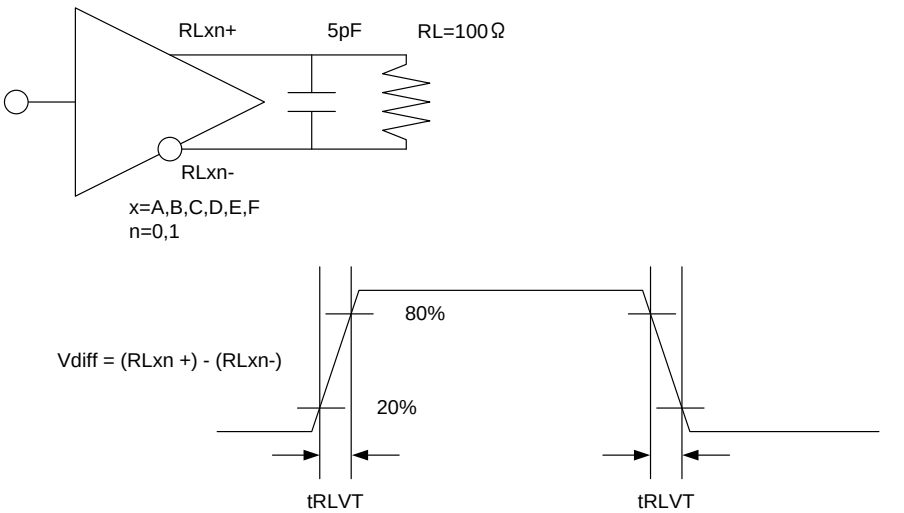


Figure 12. THCV216 LVDS Output Switching Timing Diagram and Test Circuit.

THCV215 CML Output Switching Characteristics

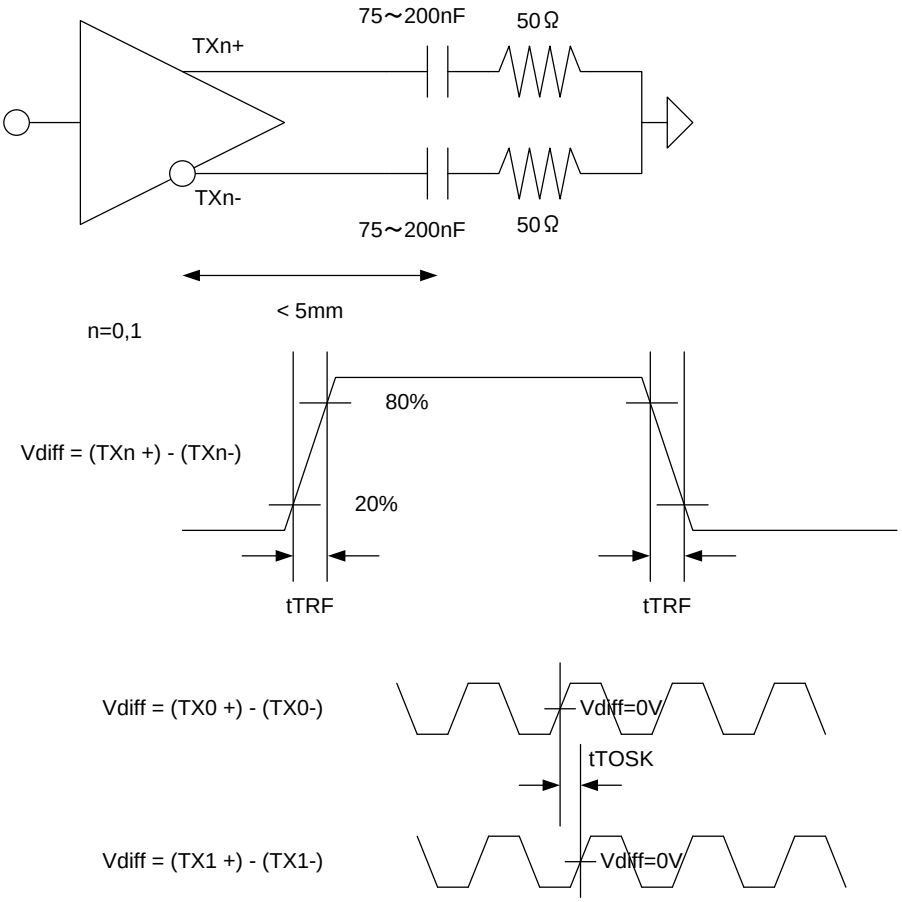


Figure 13. THCV215 CML Output Switching Timing Diagrams and Test Circuit

THCV216 CML Input Switching Characteristics

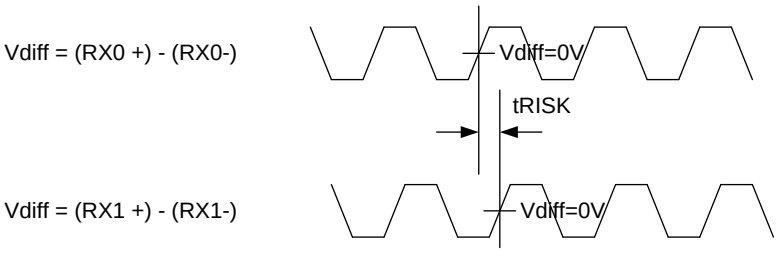


Figure 14. THCV216 CML Input Timing Diagrams

DE period requirement

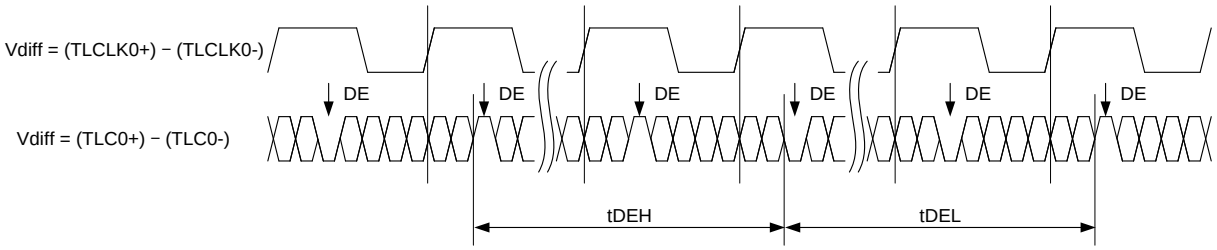


Figure 15. DE period requirement

Latency Characteristics

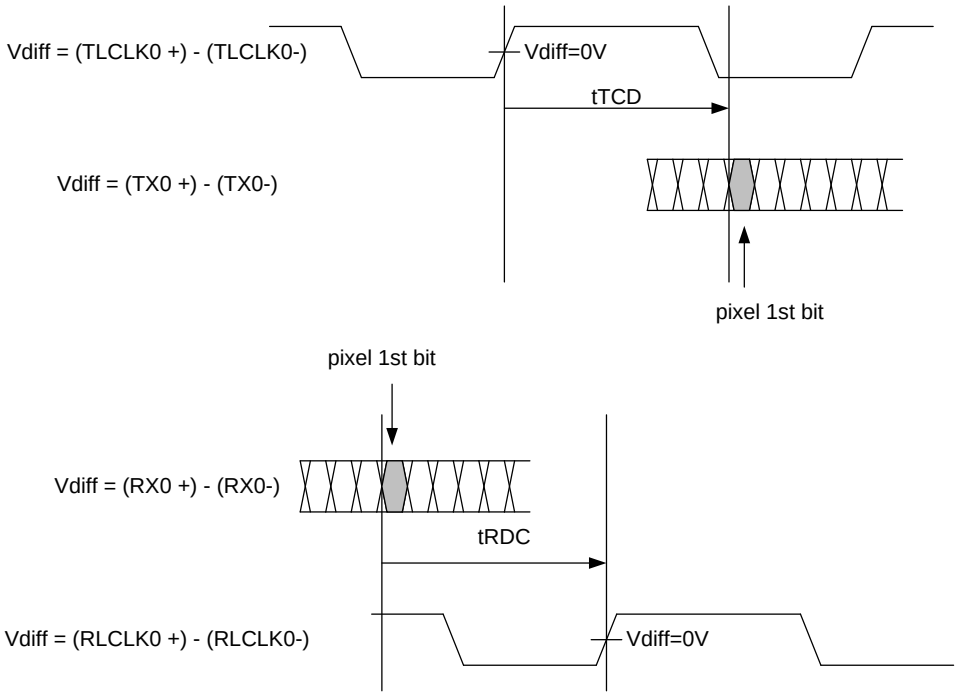


Figure 16. THCV215 and THCV216 Latency

Lock and Unlock Sequence

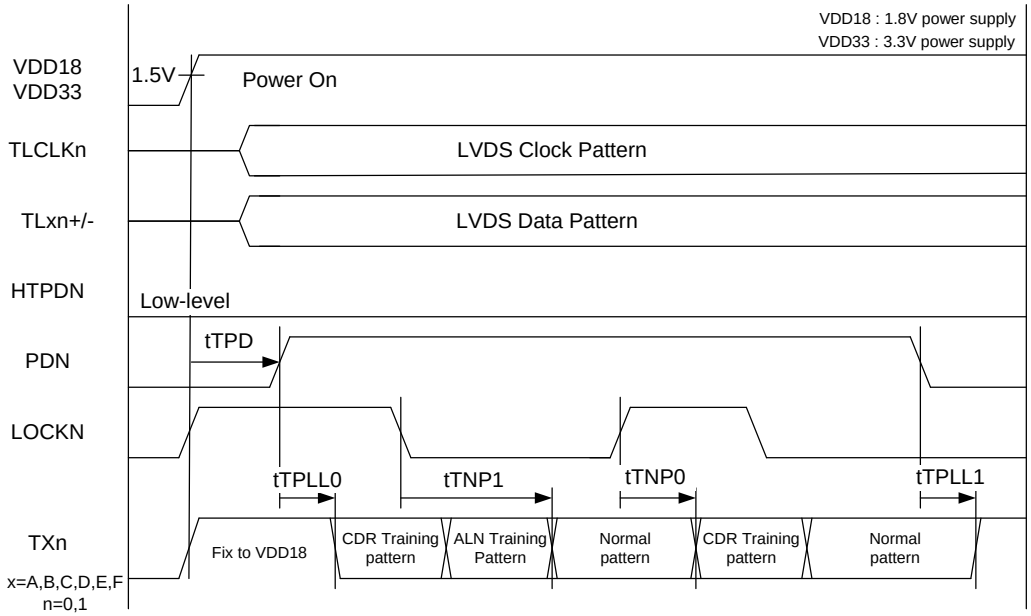


Figure 17. THCV215 Lock/Unlock Sequence

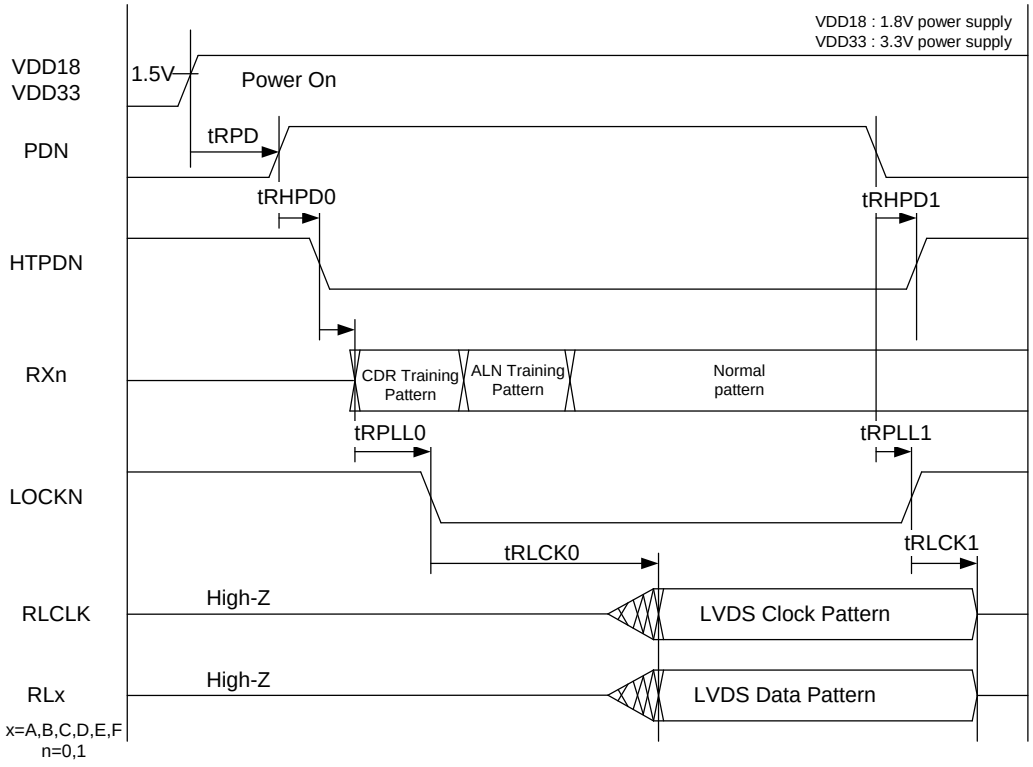


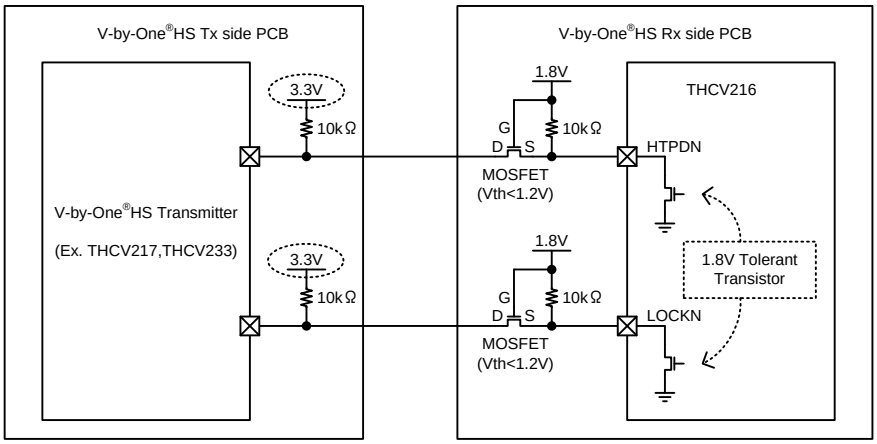
Figure 18. THCV216 Lock/Unlock Sequence

tTPD and tRPD minimum is 0sec; therefore, PDN can be applied at the same time as VDD18 and VDD33.
tTPLL0 is the time from “both PDN=High and HTPDN=Low“ moment to Training pattern ignition.
HTPDN could transit from High to Low under PDN=High condition at THCV215, which is different from what Figure 17 indicates but is natural situation.

Note

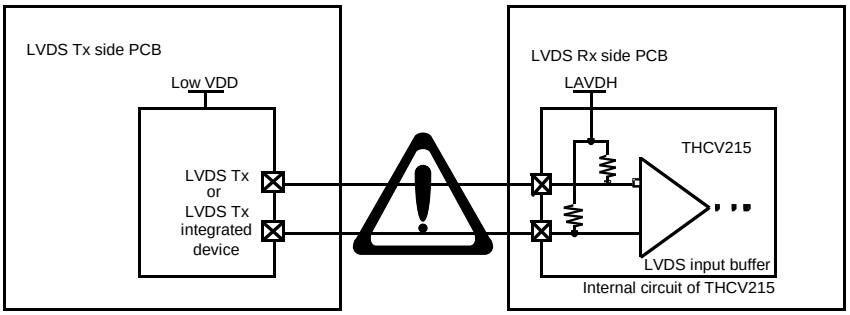
1)HTPDN/LOCKN connection between high VDD V-by-One® HS transmitter and THCV216

When using THCV216 with high VDD V-by-One® HS transmitter, user have to take care of HTPDN/LOCKN connection because THCV216 HTPDN/LOCKN output pins absolute maximum ratings are VDL+0.3V; therefore high VDD pull-up at transmitter side can cause violation of usage. Users are supposed to connect those HTPDN/LOCKN line between two devices with appropriate level-shifter configuration.



2)LVDS input pin connection

When LVDS line is not drove from the previous device, the line is pulled up to 3.3V internally in THCV215.This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THCV215. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.



3)Power On Sequence

Don't input TCLK#+/- before power supply to THCV215 is on in order to keep absolute maximum ratings.

4)Unused LVDS input pins

First, select appropriate color depth with COL0,COL1 pins. If there are inevitably remained LVDS no input pins which are originally active, tie them to GND.

Second, avoid the situation that LVDS input pins in use are open. You can use PDN=L control during no LVDS input period to cut off pulled-up resistors.

5)Cable Connection and Disconnection

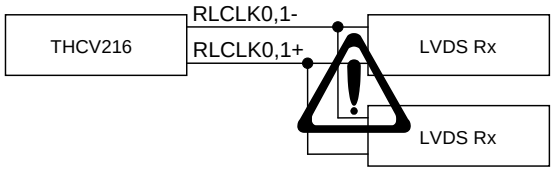
Don't connect and disconnect CML and LVDS cables, when the power is supplied to the system.

6)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THCV215 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

7)Multi Drop Connection

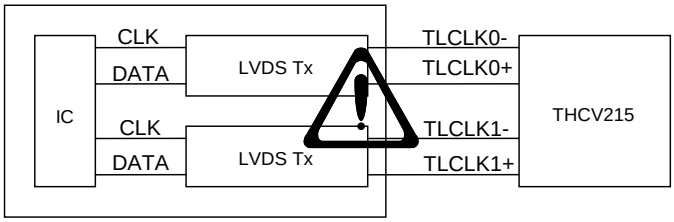
Multi drop connection is not recommended.



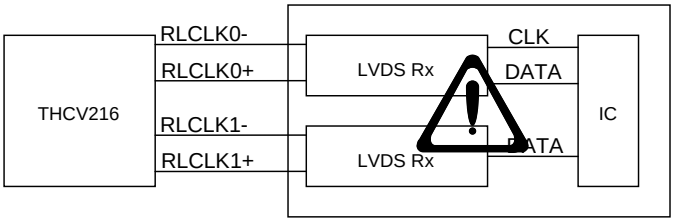
8)Multiple counterpart use

Multiple counterpart use such as following system is not recommended.

p.15 tTISK spec should be kept.



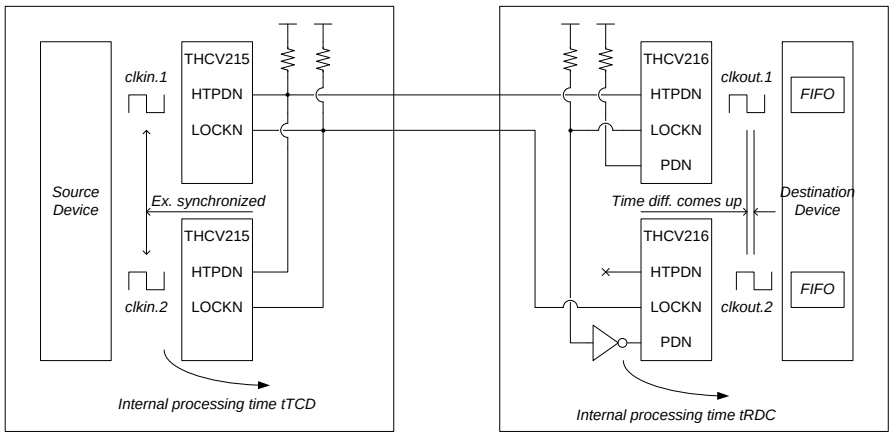
Asynchronous use such as following system is not recommended.



9)Multiple device connection

HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure.
HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx.
LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data.
LOCKN of Tx side can be simply split to multiple Tx.
There can be other applicable circuits like 'OR gate of LOCKN', 'npn transistor with resistors as inverter', etc.

Also possible time difference of internal processing time (p.15 THCV215 tTCD and THCV216 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV216, which may have internal FIFO.



Package

64 Lead Molded Thin Shrink Small Outline Package, JEDEC

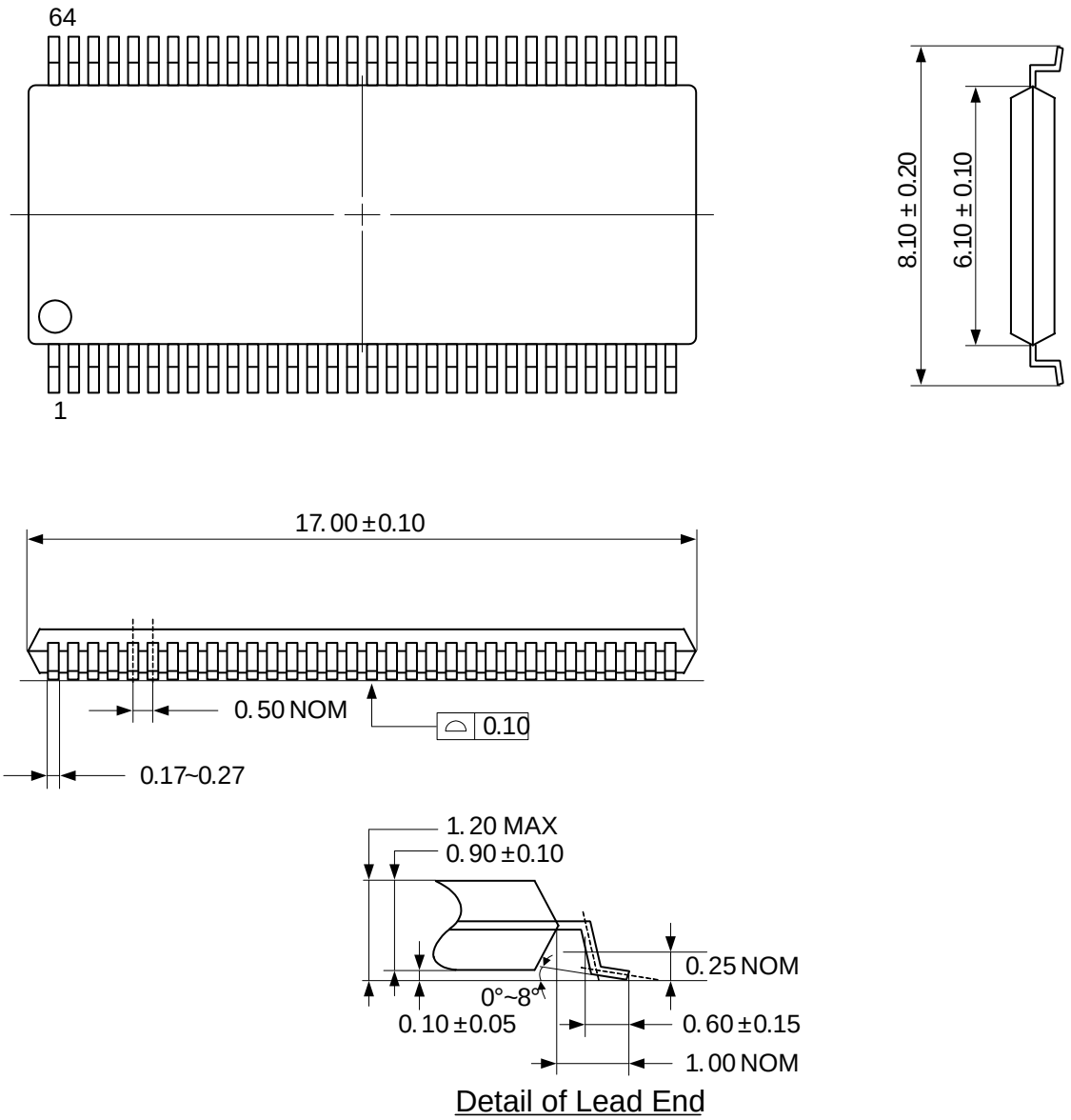


Figure 19. 64 pin TSSOP package physical dimension

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.

4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.

5. Product Application
   5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
   5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. (“THine”) accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
   5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.

6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. Please note that this product is not designed to be radiation-proof.

8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user’s request, testing of all functions and performance of the product is not necessarily performed.

9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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