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# THCV217/THCV218 Application Note

## System Diagram and PCB Design Guideline

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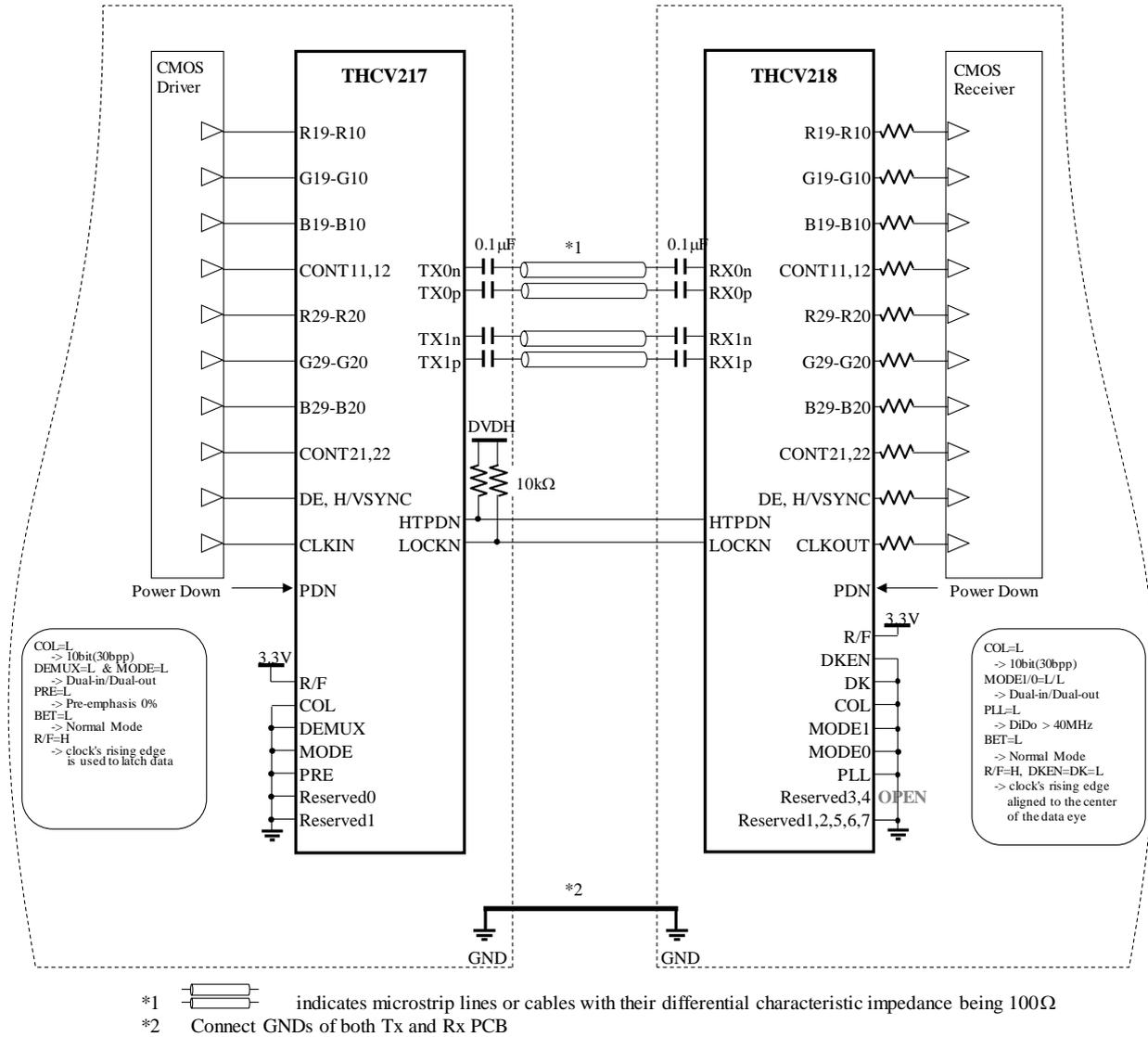
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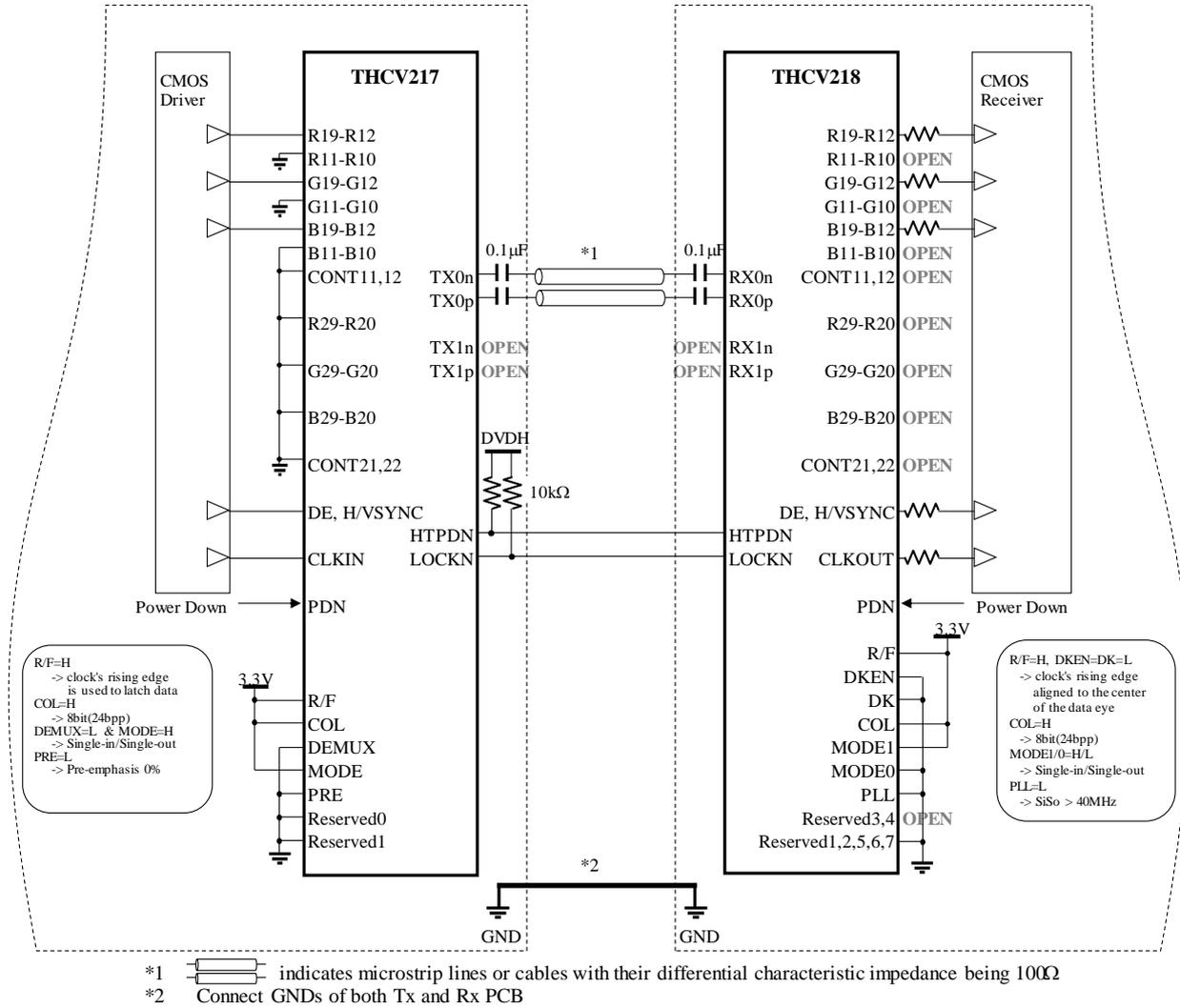
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### Application Diagrams

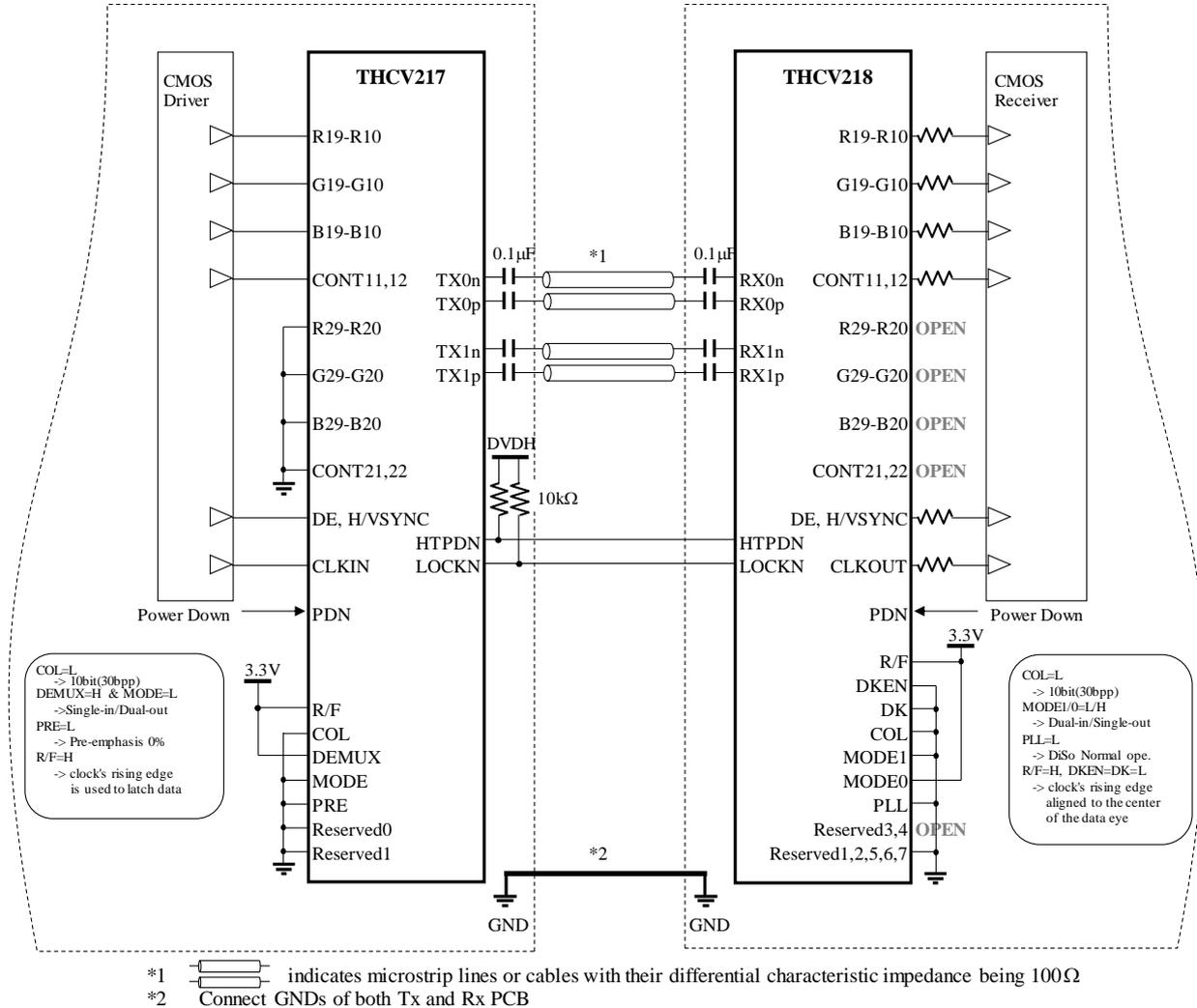
#### Dual-in/Dual-out, 10bit (30bit per pixel) without Pre-emphasis



**Single-in/Single-out, 8bit (24bit per pixel) without Pre-emphasis**



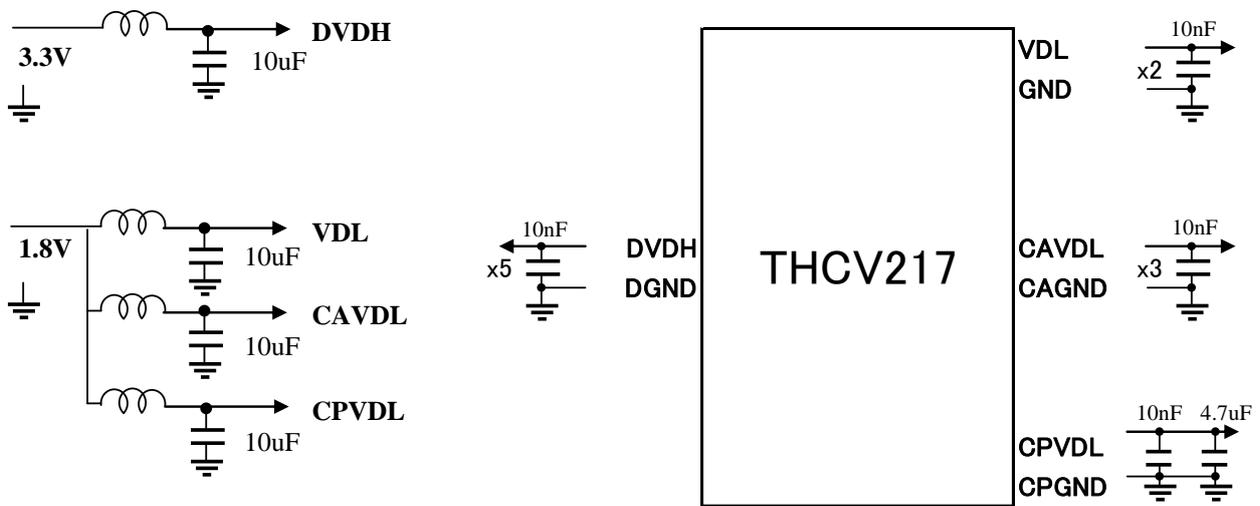
Single-in/Dual-out to Dual-in/Single-out, 10bit (30bit per pixel) without Pre-emphasis



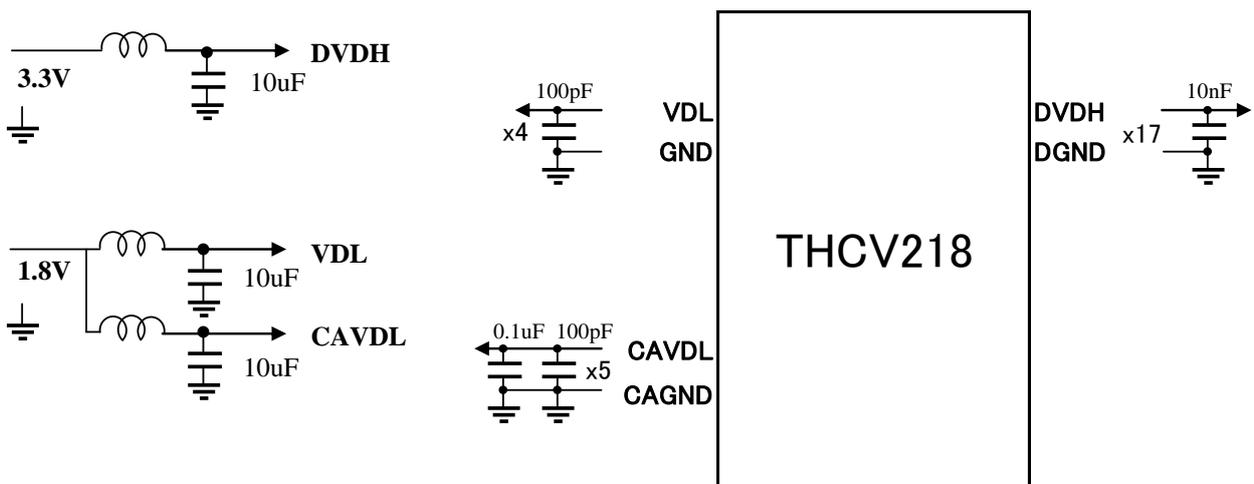
**Recommendations for Power Supply**

- Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains.
- Use high frequency ceramic capacitors of 100pF or 10nF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. 100pF capacitors, along with 0.1uF capacitors, are recommended for 218's CAVDL.
- Adding 4.7uF capacitors to PLL's power pins, along with the smaller bypass capacitors, is recommended.
- Use the same ground plane for all ground pins.

**Recommended Power Supply for THCV217**



**Recommended Power Supply for THCV218**



**Note**

**1)Cable Connection and Disconnection**

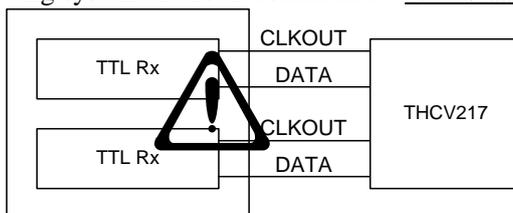
Don't connect and disconnect the LVDS and CML cable, when the power is supplied to the system.

**2)GND Connection**

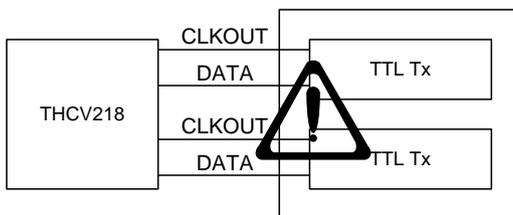
Connect the each GND of the PCB which Transmitter, Receiver and THCV217 on it. It is better for EMI reduction to place GND cable as close to LVDS and CML cable as possible.

**3)Asynchronous use**

Asynchronous use such as following system are not recommended. Data sheet p.18 tRS/tRH should be kept.



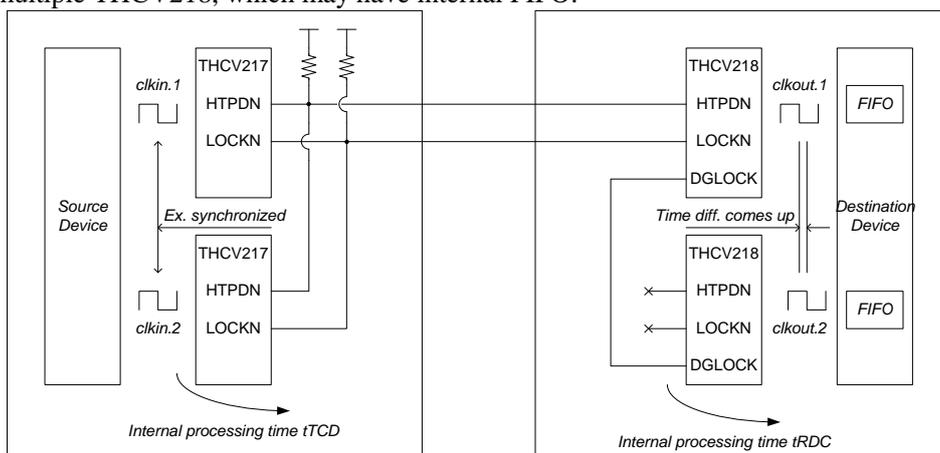
Asynchronous use such as following system are not recommended.



**4)Multiple device connection**

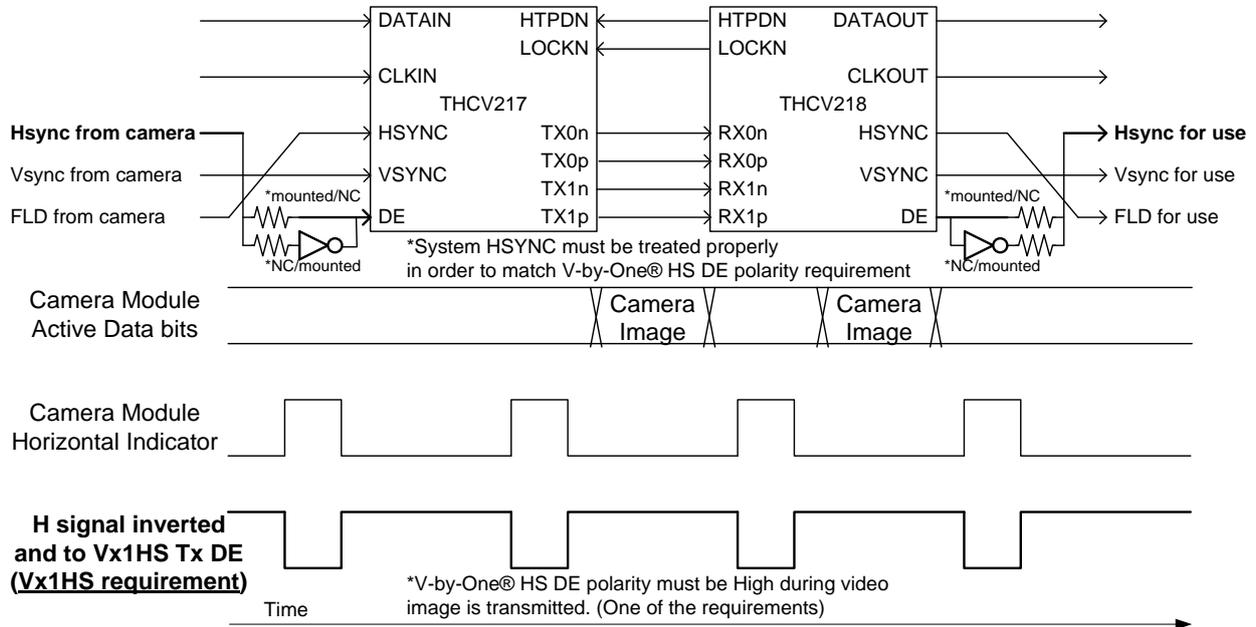
HTPDN and LOCKN signals are supposed to be connected proper for their purpose like the following figure. HTPDN should be from just one Rx to multiple Tx because its purpose is only ignition of all Tx. LOCKN should be connected so as to indicate that all Rx CDR become ready to receive normal operation data. LOCKN of Tx side can be simply split to multiple Tx. THCV218 DGLOCK is appropriate for multiple Rx use.

Also possible time difference of internal processing time (Data sheet p.19 THCV217 tTCD and THCV218 tRDC) on multiple data stream must be accommodated and compensated by the following destination device connected to multiple THCV218, which may have internal FIFO.

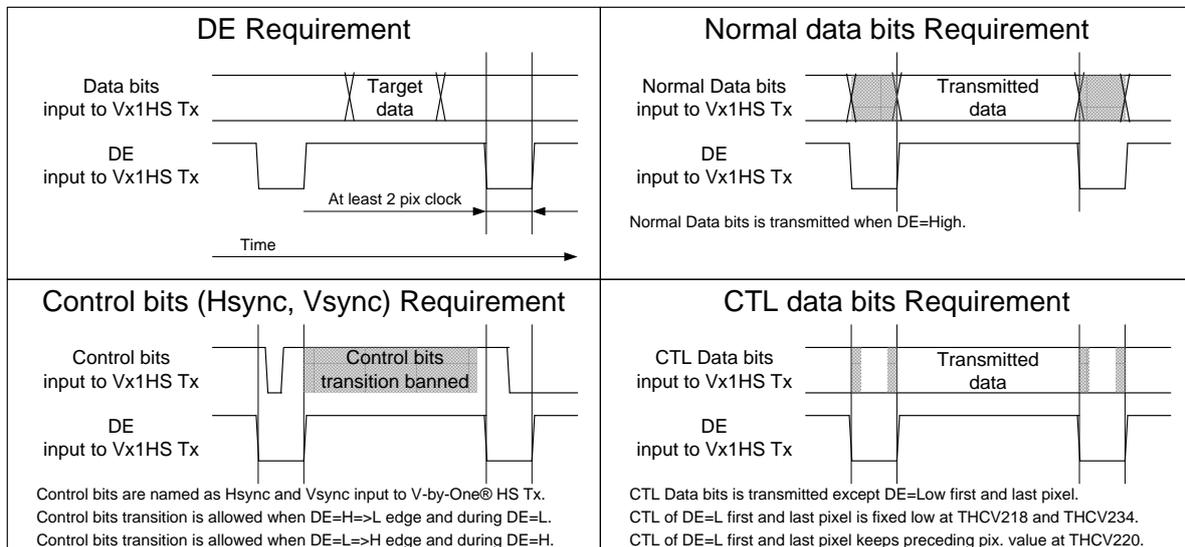


**5) In case of No DE in video signal stream**

V-by-One® HS transmission always requires DE, while some system has only HSync and VSync. Sometimes Hsync should be connected to DE and other treatment is at the same time required. DE polarity on active data transmission period must be High, which sometimes needs external inverter.



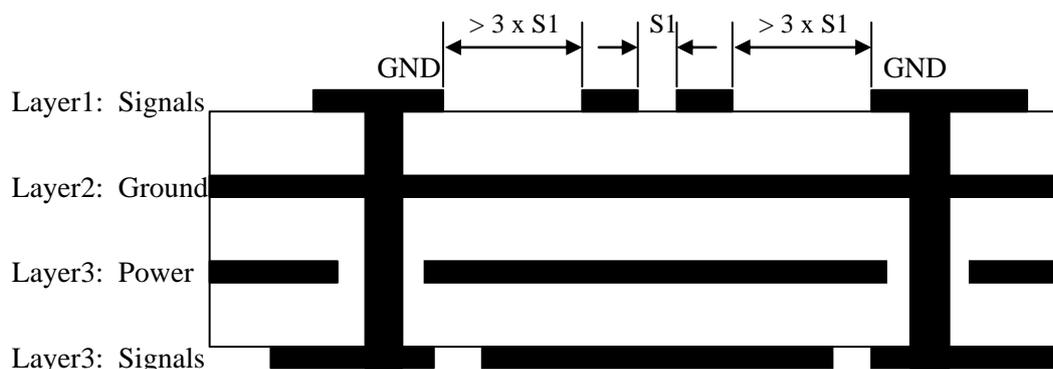
Below are consideration points if there is no DE signal on original data format.



### PCB Layout Considerations

- Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- PCB traces for high-speed signals must be single-ended microstrip lines or coupled microstrip lines whose differential characteristic impedance is  $100\Omega$ .
- Minimize the distance between traces of a differential pair ( $S1$ ) to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Route differential signal traces symmetrically.
- Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity. Mismatch among impedances of PCB traces, connectors, or cables also causes reflection, limiting the bandwidth of the high-speed channels.

### PCB Cross-sectional View for Microstrip Lines



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